SONY

Semiconductor IC

Data Book 1992

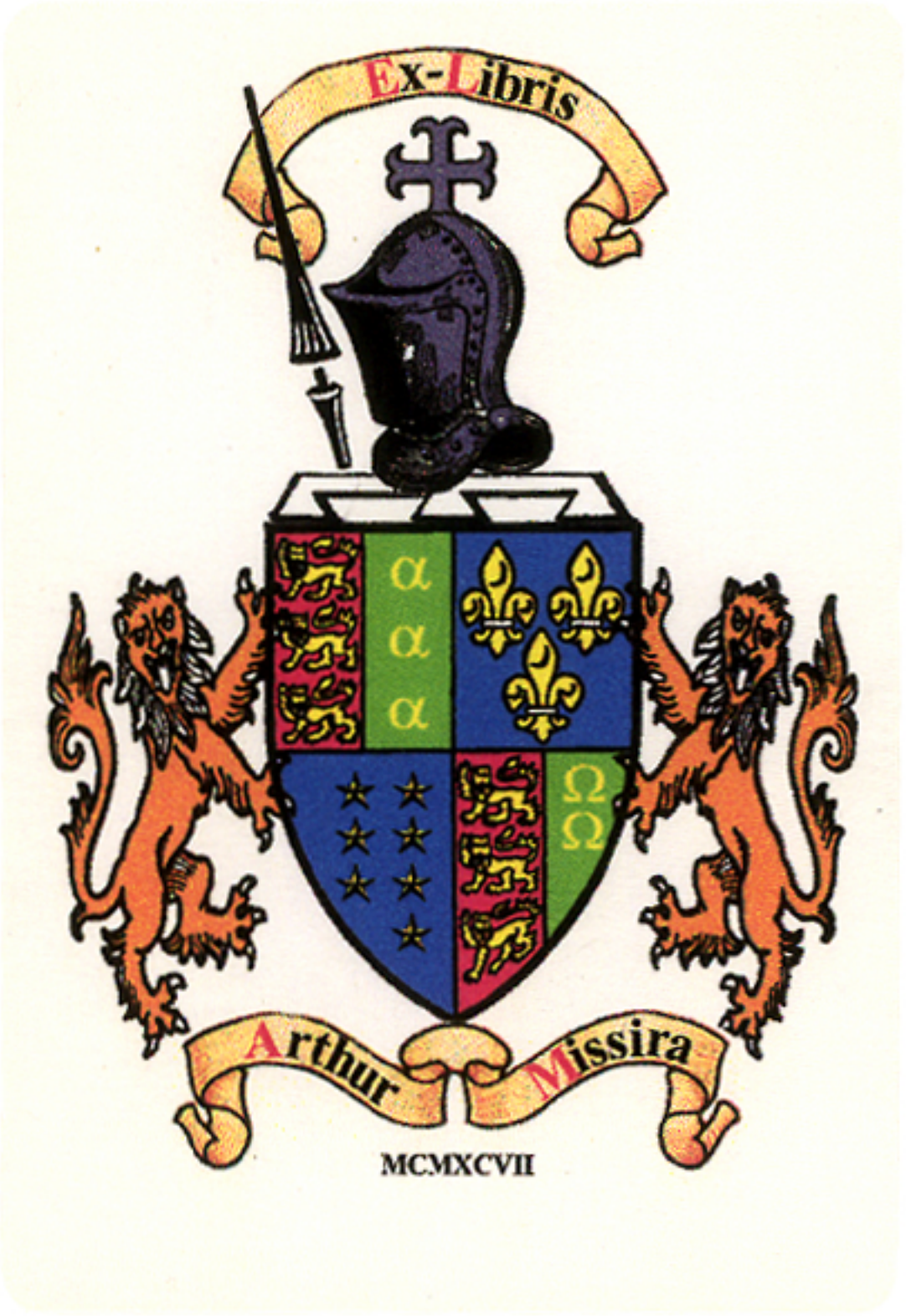
CCD Cameras & Peripherals

SONY®

Semiconductor Integrated Circuit Data Book 1992

Semiconductor Integrated Circuit Data Book

1992



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PREFACE

This is the 1992 version of the Sony semiconductor IC data book. This book covers all the semiconductor products manufactured and marketed by Sony.

In preparation of this data book, as much characteristic and application data as possible have been collected and added with a view of making this book a convenient reference for users of Sony products. If, however, you are dissatisfied with this book in any way, please write; we welcome suggestions and comments.

Sony Semiconductor Data Books

The following data books are available for the respective products applications.

1. TV Devices
2. Video Recorder ICs
3. CCD Image Sensors & Peripheral ICs
4. Compact Discplayer ICs
5. Digital Audio ICs
6. Analog Audio ICs
7. Floppy Disk/Hard Disk Drive ICs
8. Radio Communication System ICs
9. A/D, D/A Converters
10. ECL Logic/ASSP ICs
11. Microcomputers
12. Memories
13. Discrete Semiconductors
14. Laser Diodes

In addition, a List of Semiconductor Products covering all manufacutured device on the market, is issued twice a year.

Data books offer information pertaining to the listed products.

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1. List of Model Names

Type	Page	Type	Page	Type	Page
CX20095A CX20186	479	CXD1217Q	339	CXL5508M/P	829
CXA1065M	454	CXD1250M	469	CXL5509M/P	838
CXA1072Q-Z/R	627	CXD1251Q	446	ICX022BL-3	165
CXA1270N	496	CXD1252AR/AQ	390	ICX022BN-3	31
CXA1310AQ	501	CXD1253AR/AQ	409	ICX024BL-3	179
CXA1337Q-Z/R	518	CXD1255Q	428	ICX024BN-3	48
CXA1338Q-Z/R	554	CXL1008P/M	855	ICX026BKA	65
CXA1339Q-Z/R	608	CXL1009P	846	ICX026BLA	193
CXA1390AQ/AR	537	CXL1501M	867	ICX026CKA	80
CXA1391Q/R	575	CXL1502M	878	ICX027BKA	95
CXA1392Q/R	651	CXL1503M CXL1505M	721	ICX027BLA	222
CXA1393AN/AM	697	CXL1504M	743	ICX027CKA	110
CXA1439M	713	CXL1506M	890	ICX038ALA	206
CXA1516M/Q	486	CXL1517M CXL1518M	729	ICX039ALA	235
CXA1592Q/R	674	CXL1517N CXL1518N	736	ICX044ALA	251
CXB0026AM	451	CXL5001P/M	765	ICX044BKA	125
CXD1030M	297	CXL5002P/M	772	ICX045ALA	267
CXD1035BQ-Z	351	CXL5003P/M	778	ICX045BKA	142
CXD1141M	442	CXL5005P/M	785	ILX501	903
CXD1149Q/R	363	CXL5502M/P	791	ILX503	913
CXD1156Q/R	377	CXL5504M/P	751	ILX505	923
CXD1158M	307	CXL5505M/P	802	IS026BK IS027BK	285
CXD1159Q	317	CXL5506M/P	811	IU022AK-30A/40A IU024AK-30A/40A	159
CXD1217M	327	CXL5507M/P	820		

2. Index by Usage

1) CCD Image Sensor (Color)

Type	Functions				Page
	Optical size	TV System	Effective pixels	Features	
ICX022BN-3	2/3 inches	NTSC	768H×493V	Complementary mosaic filter, Variable speed electronic shutter equipped	31
ICX024BN-3	2/3 inches	PAL	756H×581V	Complementary mosaic filter, Variable speed electronic shutter equipped	48
ICX026BKA	1/2 inch	NTSC	510H×492V	Complementary mosaic filter, Variable speed electronic shutter equipped	65
ICX026CKA					80
ICX027BKA	1/2 inch	PAL	500H×582V	Complementary mosaic filter, Variable speed electronic shutter equipped	95
ICX027CKA					110
ICX044BKA	1/3 inch	NTSC	510H×492V	Complementary mosaic filter, Variable speed electronic shutter equipped	125
ICX045BKA		PAL	500H×582V		142
IU022AK-30A/40A IU024AK-30A/40A	2/3 inches	NTSC	768H×493V	• Integration of CCD image sensor, quartz low pass filter, and infrared rays cut filter • Unnecessary for optical positioning	159
		PAL	756H×581V		

2) CCD Image Sensor (Black/White)

Type	Functions				Page
	Optical size	TV System	Effective pixels	Features	
ICX022BL-3	2/3 inches	EIA	768H×493V	Variable speed electronic shutter equipped	165
ICX024BL-3		CCIR	756H×581V		179
ICX026BLA	1/2 inch	EIA	510H×492V	Variable speed electronic shutter equipped	193
ICX038ALA			768H×494V		206
ICX027BLA	1/2 inch	CCIR	500H×582V	Variable speed electronic shutter equipped	222
ICX039ALA			752H×582V		235
ICX044ALA	1/3 inch	EIA	510H×492V	Variable speed electronic shutter equipped	251
ICX045ALA		CCIR	500H×582V		267

3) CCD Image Sensor System

Type	Functions				Page
	Classification		Image sensor	Features	
IS026BK IS027BK	Color	NTSC	ICX026BK	• Variable electronic shutter equipped • Extemal synchronization possible • High senstivity • High density mounting adopting small packages	285
		PAL	ICX027BK		

4) Scanning System IC for Video Camera

Type	Applications	Functions	Page
CXD1030M	Sync signal generator	14MHz (18MHz) demultiplier, for NTSC, PAL	297
CXD1158M		14MHz (18MHz) demultiplier, for NTSC, PAL, Sub carrier output×3	307
CXD1159Q		14MHz (18MHz) demultiplier, for NTSC, PAL, Sub Window pulse output	317
CXD1217M		For NTSC, PAL, PALM, SECAM, Color framing in NTSC, PAL, PALM	327
CXD1217Q			339
CXD1035BQ-Z	Timing pulse generator for scanning system	CCD drive timing pulse generation, Signal processing pules generation, for ICX022BL, ICX024BL	351
CXD1149Q/R		CCD drive timing pulse generation, Signal processing pules generation, for ICX022BN/ICX024BN, Variable speed electronic shutter timing generation (1/60 to 1/10000s.)	363
CXD1156Q/R		CCD drive timing pulse generation, Variable speed electronic shutter timing generation (1/60 to 1/10000s.) for ICX026BKA/BLA, ICX027BKA/BLA	377
CXD1252AR/AQ		CCD drive timing pulse generation, Signal processing pulse generation, Variable speed electronic shutter timing generation (built-in slow shutter) for ICX038BNA/ICX039BNA	390
CXD1253AR/AQ		CCD drive timing pulse generation, Signal processing pulse generation, Variable speed electronic shutter timing generation (built-in slow shutter) for ICX026CKA/ICX027CKA, ICX044BKA/ICX045BKA	409
CXD1255Q		CCD drive timing pulse generation, Signal processing pulse generation, Variable speed electronic shutter timing generation (1/60 to 1/10000s.) for ICX038ALA/ICX039ALA	428
CXD1141M	Variable speed electronic shutter timing generator	Variable speed electronic shutter timing generation (1/60 to 1/10000s.) for ICX022BL/ICX024BL	442
CXD1251Q	Blemish compensation timing generator	Blemish compensation timing generation	446
CXB0026AM	Vertical/horizontal clock driver	CCD image sensor driver×2, Compatible with high frequency operation	451
CXA1065M	Vertical clock driver	CCD image sensor driver×4, Lead-out pulse generation inverter, Negative voltage generation inverter	454
CXD1250M		CCD image sensor driver×4, Lead-out pulse generation inverter, Shutter pulse driver	469

5) Signal Processing IC for Video Camera

Type	Applications	Functions	Page
CX20095A CX20186	Video output	6dB amplifier, Video driver, Bidirectional video driver	479
CXA1516M/Q	Auto Focus detector for camcoder	Built-in 3-channel Built-in gain control (6 to 33dB)	486
CXA1270N	Vertical aperture correction	Vertical aperture correction signal generation	496
CXA1310AQ	CCD B/W camera processing	Signal processing, Built-in AGC loop operationnal amplifier	504
CXA1337Q-Z/R	CCD color camera sample and hold, color separation	CDS, AGC, color separation S/H, Chroma suppression	518
CXA1390AQ/AR		CDS, AGC,color separation	537
CXA1338Q-Z/R	CCD color camera matrix	From color complementary (Mg, G, Cy, Ye) mosaic coding, R, G, B, synthetic and Y signal processing	554
CXA1391Q/R	CCD color camera processing	Original color separation, White balance, γ correction, Sharpness control	575
CXA1339Q-Z/R		Matrix, White balance, γ correction, Negative/positive inversion	608
CXA1072Q-Z/R	CCD color camera encoder	Aperture, Auto-carrier balance, Negative-positive inversion, Fader, Chroma suppression, BLK cleaning	627
CXA1392Q/R		Aperture correction, Y/C separation output	651
CXA1592Q/R	CCD color camera processing	Aperture correction, Y/C separation output Chang version of CXA1392 (ratio and level)	674
CXA1393AN/AM	Title addition	Title insertion for video camera	697
CXA1439M	For CCD camera, CDS	CDS, 6dB amplifier, 9.5dB amplifier	713
CXL1503M CXL1505M	Chroma signal 1H delay line	In-phase for color signal delay (1H×4) CMOS-CCD delay line	721
CXL1517M CXL1518M	Chroma signal 1H delay line	1H×3 CMOS-CCD delay line	729
CXL1517N CXL1518N	Chroma signal 1H delay line	1H×3 CMOS-CCD delay line	736
CXL1504M	Luminance signal 1H delay line	NTSC 1H CMOS-CCD delay line	743
CXL5504M/P			751

6) CCD Delay Line

Type	Applications	Functions	Page
CXL5001P/M	General purpose	3fsc, NTSC, 1H	765
CXL5002P/M		3fsc, NTSC, 1/2H	772
CXL5003P/M		3fsc, PAL, 1H	778
CXL5005P/M		3fsc, NTSC, 1H, 3 pole wiht PLL	785
CXL5502M/P		4fsc, NTSC, 1H, 4 pole with PLL	791
CXL5504M/P		4fsc, NTSC, 1H	751
CXL5505M/P		4fsc, PAL, 1H, 4 pole with PLL	802
CXL5506M/P		4fsc, PAL, 1H	811
CXL5507M/P		2fsc, NTSC, 1H	820
CXL5508M/P		2fsc, PAL, 1H	829
CXL5509M/P	1H, 2H CCD delay line for NTSC	1 input and 2 outputs (1H delay, 2H delays). Built-in quadrupre progression PLL circuit	838
CXL1009P	Video disk	TBC, 15.2 to 27.2MHz drive, 680-bit×2	846
CXL1008P/M	8mm VCR	Skew correction (3fsc, 1/2H), 359-bit, 20-bit	855
CXL1501M		4fsc, NTSC comb filter	867
CXL1502M		3fsc, PAL comb filter	878
CXL1506M		3fsc, PAL 1H/2H output, with PLL	890
CXL1503M CXL1505M	8mm VCR	301.5-bit×4 (4/3fsc, 1H) 453.5-bit×4 (2fsc, 1H)	721
CXL1504M	8mm VCR	905.5-bit (4fsc, 1H)	743
CXL1517M CXL1518M	Color video camera	452.5-bit×2, 453.5-bit×1 (2fsc, 1H)/ 300.5-bit×2, 301.5-bit×1 (4/3fsc, 1H)	729
CXL1517N CXL1518N	Color video camera		736

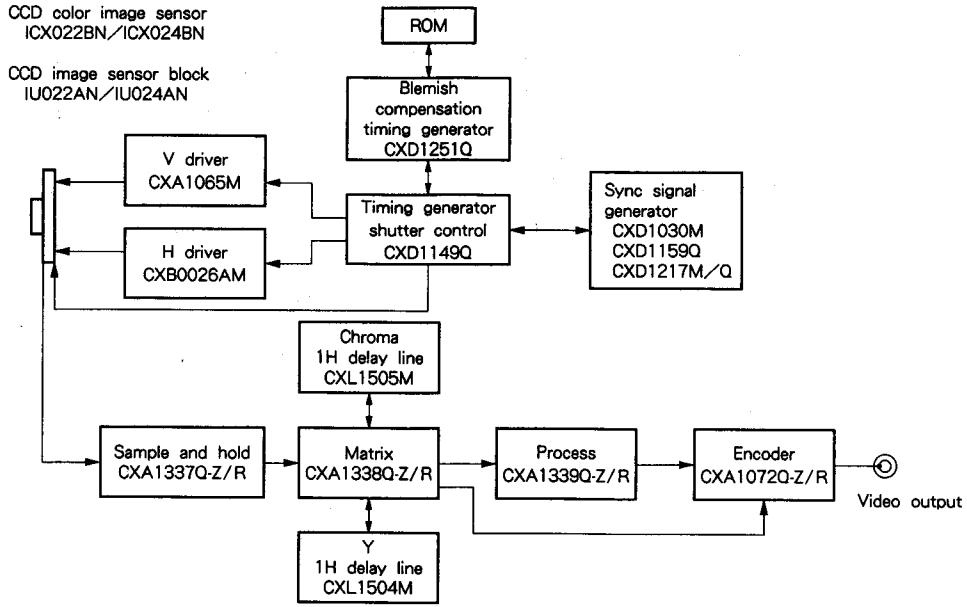
7) CCD Linear Sensor

Type	Applications	Functions	Page
ILX501	Facsimile, Copy machine	5000-pixel, B/W linear sensor	903
ILX503	Facsimile, Image scanner	2048-Pixel, B/W linear sensor	913
ILX505		2592-Pixel, B/W linear sensor	923

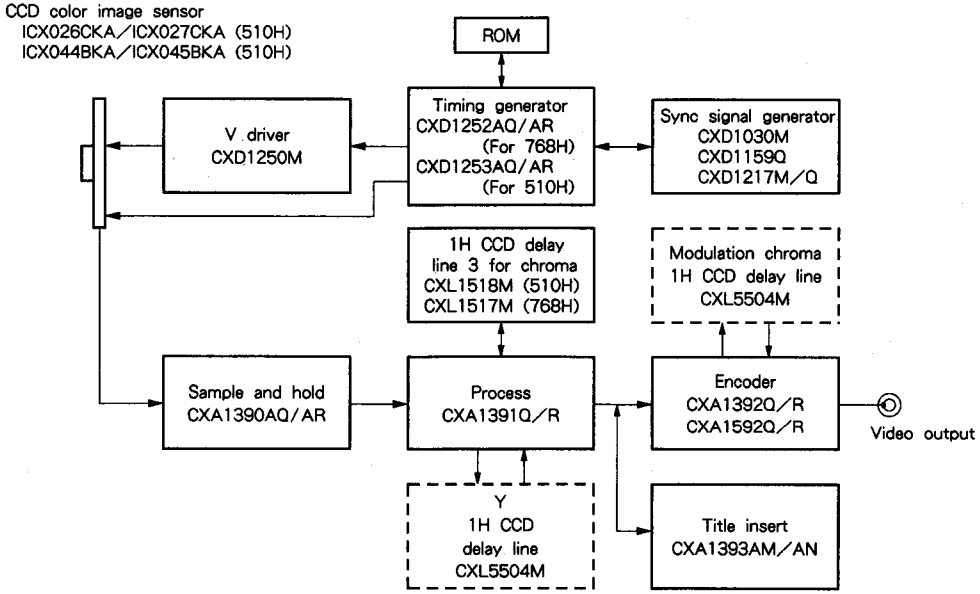
● CCD IMAGE SENSOR AND CAMERA SIGNAL PROCESSING IC

	classification	Color				B/W			
CCD image sensor	System	ICX022BN ICX024BN	ICX026CKA ICX027CKA	ICX038BNA ICX039BNA	ICX044BKA ICX045BKA	ICX022BL ICX024BL	ICX026BLA ICX027BLA	ICX038ALA ICX039ALA	ICX044ALA ICX045ALA
	Optical size (inch)	2/3	1/2		1/3	2/3	1/2		1/3
	Effective pixels (H×V)	768×493 756×581	510×492 500×582	768×494 752×582	510×492 500×582	768×493 756×581	510×492 500×582	768×494 752×582	510×492 500×582
Timing/Driver system	Timing generation	CXD1149Q/R	CXD1253AQ/AR	CXD1252AQ/AR	CXD1253Q/R	CXD1035BQ-Z	CXD1156Q/R	CXD1255Q	CXD1156Q/R
	Vertical driver	CXA1065M	CXD1250M			CXA1065M	CXD1250M		
	Horizontal driver	CXB0026AM	Built into timing generator			CXB0026AM	Built into timing generator	74AC04	Built into timing generator
	Sync signal generator	CXD1030M, CXD1159Q, CXD1217M/Q							
	Blemish compensation timing generator	CXAD1251Q	Built into timing generator				CXD1251Q		Built into timing generator
	Variable electronic shutter timing generator	Built into timing generator				CXD1141M	Built into timing generator		
Signal processing system	Sample and hold AGC	CXA1337Q-Z/R	CXA1390AQ/AR			CXA1310AQ			
	Matrix	CXA1338Q-Z/R	CXA1391Q/R						
	Process	CXA1339Q-Z/R							
	Encoder	CXA1072Q-Z/R	CXA1392Q/R, CXA1592Q/R						
	CCD delay line for chroma	CXL1505M	CXL1518M CXL1518N	CXL1517M CXL1517N	CXL1518M CXL1518N				
	CCD delay line for Y	CXL1504M	CXL5504M						
	Title insert	CXA1157M	CXA1393AM/AN						

■ CCD COLOR CAMERA BLOCK DIAGRAM FOR 2/3" OPTICAL SIZE



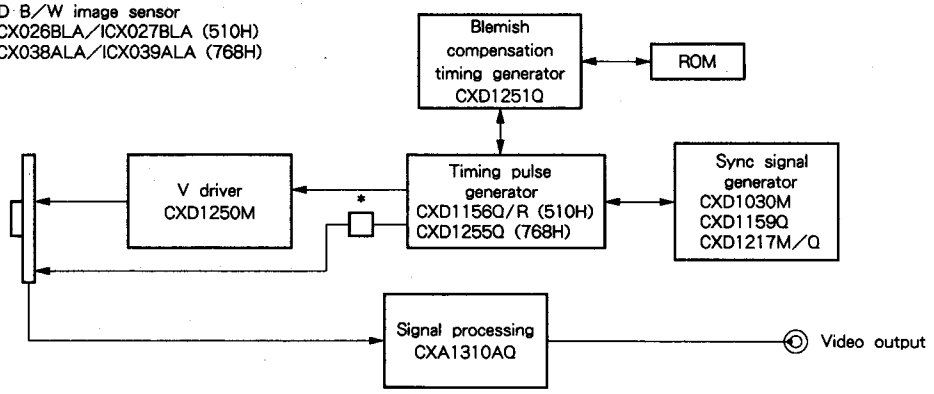
■ CCD COLOR CAMERA BLOCK DIAGRAM FOR 1/2", 1/3" OPTICAL SIZE



* The system without CCD delay line of [ ] can be configurated.

■ CCD B/W CAMERA BLOCK DIAGRAM FOR 1/2" OPTICAL SIZE

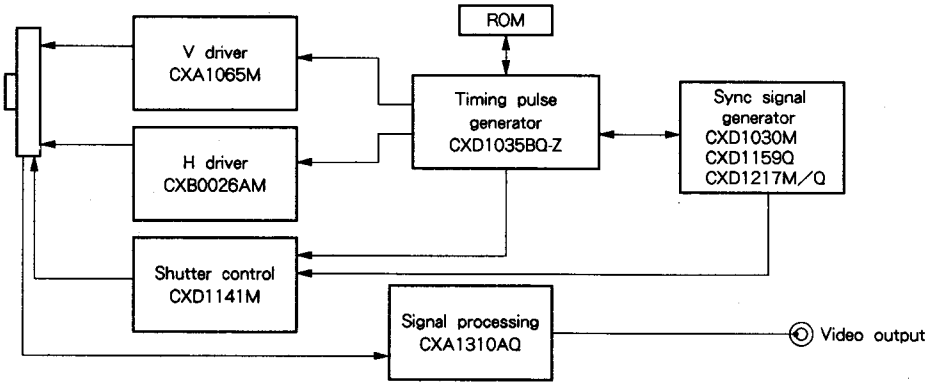
CCD B/W image sensor
ICX026BLA/ICX027BLA (510H)
ICX038ALA/ICX039ALA (768H)



* On ICX038ALA/ICX039ALA, CMOS standard logic ICs (74AC04 etc.) are needed as horizontal driver.

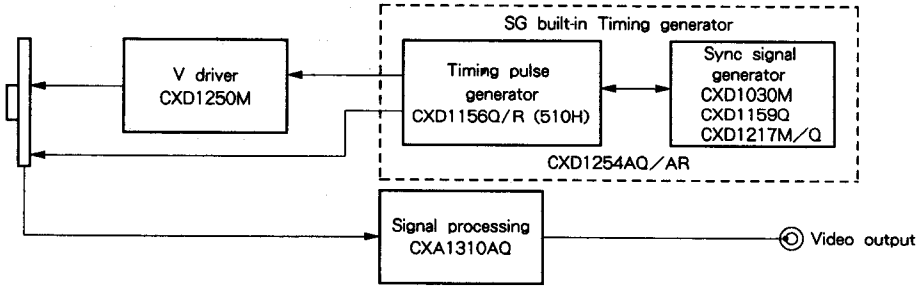
■ CCD B/W CAMERA BLOCK DIAGRAM FOR 2/3" OPTICAL SIZE

CCD B/W Image sensor
ICX022BL/ICX024BL



■ CCD B/W CAMERA BLOCK DIAGRAM FOR 1/3" LENS SYSTEM

CCD B/W image sensor
ICX044ALA/ICX045ALA



3. IC Nomenclature

1) Nomenclature of IC product name

Currently, both the conventional and new nomenclature systems are mixed in naming IC products.

a) Conventional nomenclature system

[Example] CX20011A

- A — Improvement mark
  - "A" is affixed when specifications are partially improved.
- 11 — Product number
  - Identifies individual product.
- 20 — Category number
  - Indicates the product category in one or two digits.
  - Bipolar IC: 0, 1, 8, 10, 20, 22
  - MOS IC: 5, 7, 23, 79
- CX — Sony IC mark

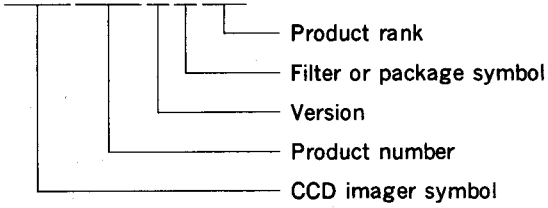
b) New nomenclature

[Example] CXA1001AP

- P — Package mark
  - P: Plastic Dual In-line Package
  - D: Ceramic Dual In-line Package
  - M: Small Outline L-Leaded Package
  - L: Single In-line Package
  - Q: Quad Flat L-Leaded Package
  - S: Shrink Dual In-line Package
  - N: Very Small Outline Package (SSOP)
  - R: Very Small Quad Flat Package
- A — Improvement mark
  - "A" is affixed when specifications are improved.
- 1001 — Product number
  - Identifies the individual product.
- A — Product category mark
  - A: Bipolar IC
  - B: Bipolar digital IC
  - D: MOS logic IC
  - K: Memory, Mask ROM
  - P, Q: Microcomputer, Microprocessor
  - L: CCD signal processor
- CX — Sony IC mark

2) Nomenclature of CCD Imager

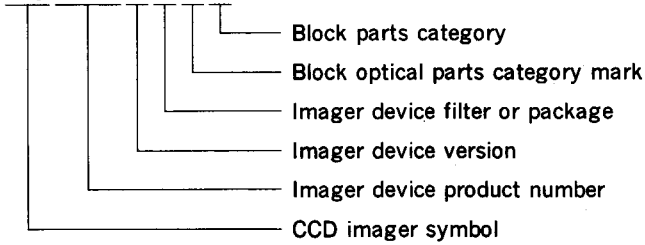
(Example) ICX026AK-3



3) Nomenclature of CCD Imager Block

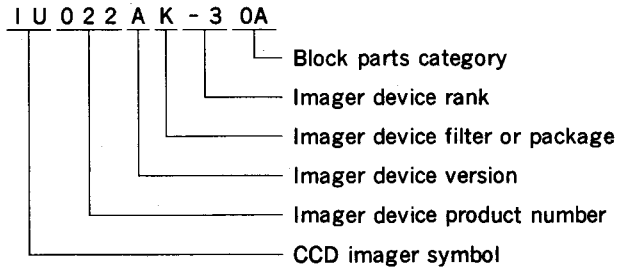
a) Conventional nomenclature system

(Example) IU018CKAA



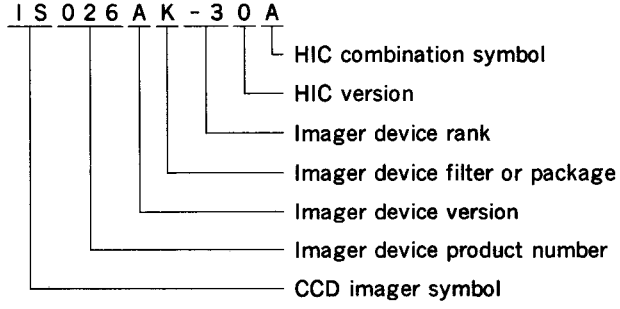
b) New Nomenclature

(Example) IU022AK-30A



4) Nomenclature of CCD Imager System

(Example) IS026AK-30A



4. Precautions for IC Application

1) Absolute maximum ratings

The maximum ratings for semiconductor devices are normally specified by "absolute maximum ratings". The values shown in the maximum ratings table must never be exceeded even for a moment.

If the maximum rating is ever exceeded, device deterioration or damage will occur immediately. Then, even if the affected device can operate, the life will be considerably shortened.

IC maximum ratings

The following maximum ratings are used for ICs.

(1) Maximum power supply voltage Vcc (V_{DD})

The maximum voltage that can be applied between the power supply pin and ground pin.

This power supply voltage rating is directly related to the dielectric voltage of transistors in the internal circuit. The transistors may be destroyed if this voltage is exceeded.

(2) Allowable power dissipation P_D

The maximum power consumption allowed in IC.

Usage beyond the Allowable power dissipation will cause ultimate destruction through the IC's heat generation.

(3) Operating ambient temperature Topr

The temperature range within which IC can operate satisfactorily.

Even if this temperature range is exceeded and some deterioration in operating characteristics is noted, the IC is not always damaged.

For some ICs, the electrical characteristics at Ta=25°C are not guaranteed even in this temperature range.

(4) Storage temperature Tstg

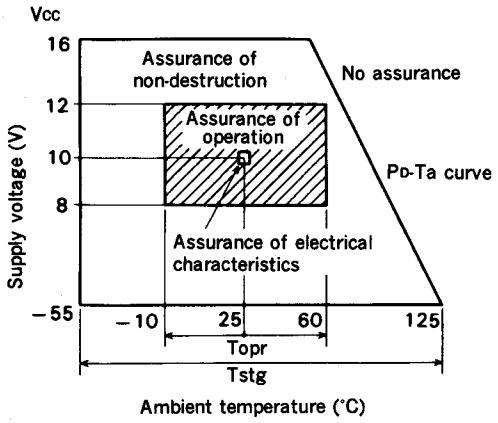
The temperature range for storing the IC which is not operating.

This temperature is restricted by the package material, and the intrinsic properties of the semiconductor.

(5) Other values

The input voltage Vin, output voltage Vout, input current Iin, output current Iout and other values may be specified in some IC's.

A general example on the relation with Absolute Maxium Ratings.



Main points on Circuit design.

In the circuit design the absolute maximum ratings must not be exceeded, and it must be designed only after considering the worst situations among the following:

- Fluctuation in source voltage
- Scattering in the electrical characteristics of electrical parts (transistors, resistors, capacitors, etc.)
- Power dissipation in circuit adjustment
- Ambient temperature
- Fluctuation in input signal
- Abnormal pulses

If this allowable power dissipation is exceeded, electrical and thermal damage may result.

This value varies with amount of IC integration in package types.

2) Protection against electrostatic breakdown

There have been problems concerning electrostatic destruction of electronic devices since the 2nd World War. Those are closely related to the advancement made in the field of semiconductor devices; this is, with the development of semiconductor technology, new problems in electrostatic destruction have arisen. This situation, perhaps, can be understood by recalling the case of MOS FET.

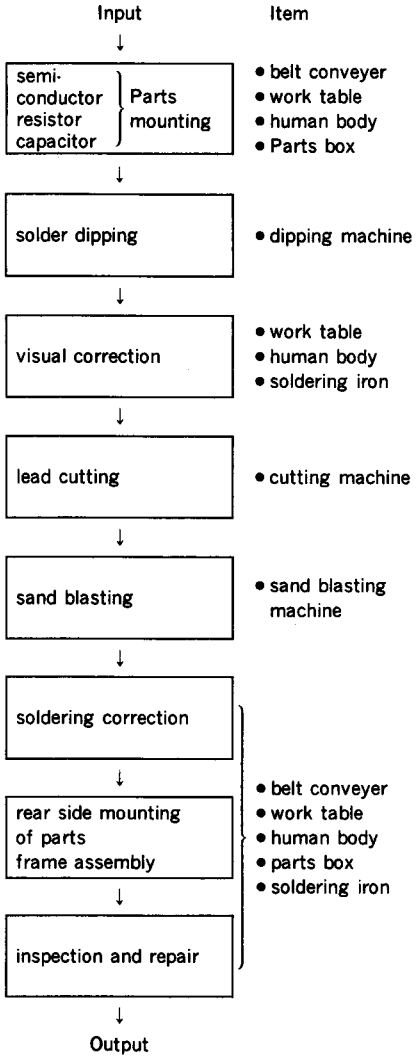
Electrostatic destruction is again drawing people's attention as we are entering the era of LSI, VLSI, and ULSI. Here are our suggestions for preventing such destruction in the device fabrication process.

Factors causing electrostatic generation in manufacture process

A number of dielectric materials are used in manufacture process. Friction of these materials with the substrate can generate static electricity which may destroy the semiconductor device.

Factors that can cause electrostatic destruction in the manufacture process are shown below:

Causes of electrostatic destruction of semiconductor parts in manufacture process



Handling precautions for the prevention of electrostatic destruction

Explained below are procedures that must be taken in fabrication to prevent the electrostatic destruction of semiconductor devices.

The following basic rules must be obeyed.

①Equalize potentials of terminals when transporting or storing.

②Equalize the potentials of the electric device, work bench, and operator's body that may come in contact with the semiconductor device.

③Prepare an environment that does not generate static electricity.

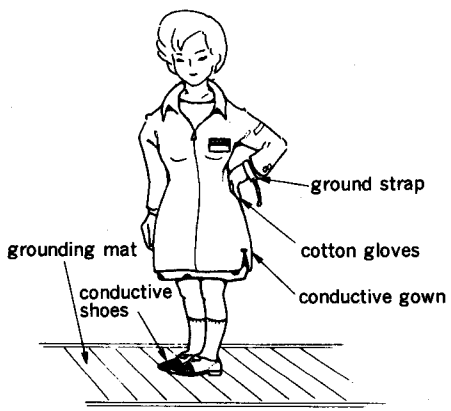
One method is keeping relative humidity in the work room to about 50%.

Operator

(1) Clothes

Do not use nylon, rubber and other materials which easily generate static electricity. For clothes, use cotton, or antistatic-treated materials. Wear gloves during operation.

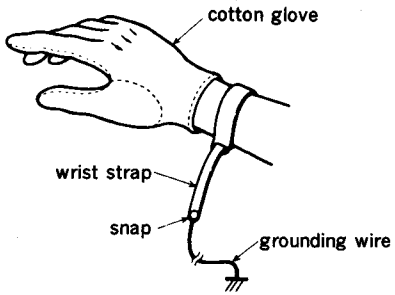
protective clothing for static electricity



(2) Grounding of operator's body

The operator should connect the specified wrist strap to his arm.

example of grounding band



When using a copper wire for grounding, connect a 1MΩ resistance in series near the hand for safety.

(3) Handling of semiconductor device

Do not touch the lead. Touch the body of the semiconductor device when holding. Limit the number of handling times to a minimum. Do not take the device out of the magazine or package box unless it is absolutely necessary.

holding of semiconductor device

Equipment and tools

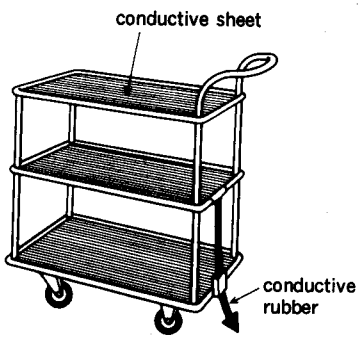
(1) Grounding of equipment and tools

Ground the equipments and tools that are to be used. Check insulation beforehand to prevent leakage.

[Check point]

- measuring instrument
- conveyer
- electric deburr brush
- carrier
- solder dipping tank
- lead cutter
- shelves and racks

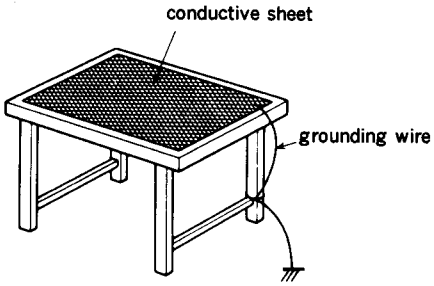
grounding of carrier



(2) Grounding of work table

Ground the work table as illustrated. Do not put anything which can easily generate static electricity, such as foam styrol, on the work table.

grounding of work table



(3) Semiconductor device case

Use a conductive case.

(4) Insertion of semiconductor device

Insert the semiconductor device during the mounting process or on the belt conveyer. The insertion should be done on a conductive sheet.

(5) Other points of caution

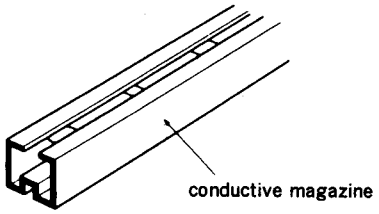
Take note of the kind of brush material used for removing lead chips. Use metal or antistatic-treated plastic brushes.

Transporting, storing and packaging methods

(1) Magazine

Use conductive, or antistatic-treated plastic IC magazines.

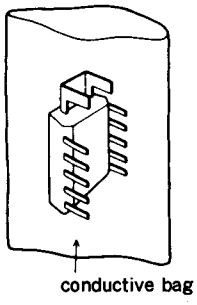
magazine



(2) Bag

Use a conductive bag to store ICs.

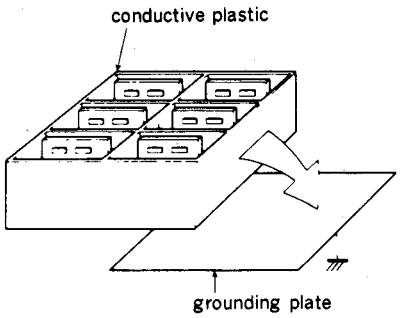
bag



(3) Handling of delivery box

The delivery box used for carrying substrates must be made of conductive plastic. Do not use a vinyl chloride or acrylic delivery box, otherwise static electricity will be generated.

handling of delivery box



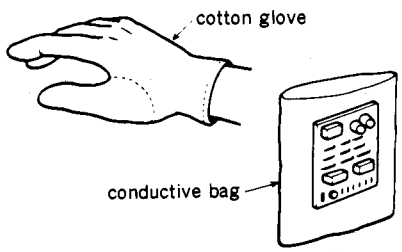
(4) Treatment after vehicle transport

After truck transport, place the magazine, package box or delivery box on the grounded rack, work table for discharging.

(5) Handling of mounted substrates

Wear cotton gloves when handling. As far as possible, avoid touching soldered faces. When handling mounted substrates individually, be sure to use a conductive bag. Do not use a polyethylene bag.

handling of mounted substrate

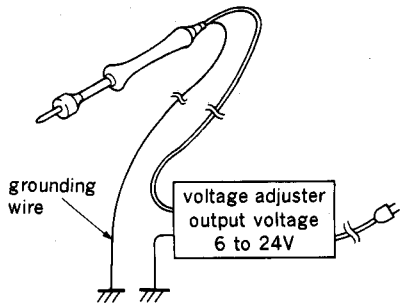


Soldering operation

(1) Soldering iron

Use a soldering iron with a grounding wire and an insulation resistance greater than 10MΩ (DC 500V) after five minutes from energizing.

example of solder iron tip grounding



(2) Operation

After inserting the semiconductor device into the substrate, solder it as quickly as possible. Do not carry the substrate with the inserted semiconductor device by car.

(3) Correction

When correcting parts (semiconductor device and CR parts) after solder-dipping, be sure to wear cotton gloves.

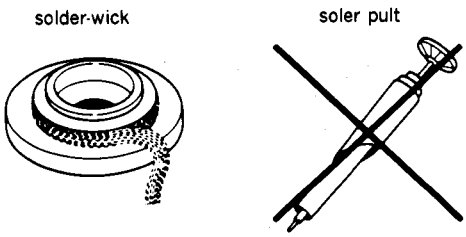
(4) Manual soldering

Solder with wrist strap connected to the hand.

(5) Removing semiconductor device

Do not use the Solder-Pult when removing the semiconductor device. Use a Solder-wick or equivalent.

solder remover



3) Mounting method

Soldering and solderability

(1) Solderability by JIS

JIS specifies solderability of an IC terminal (lead) in "JIS-C7022 Test Procedure A-2". An abstract of this standard follows:

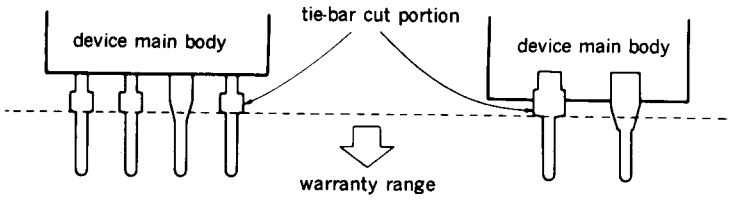
- Rosin flux must be used, and the terminal must be dipped in it for 5-10 seconds.
- H63A or equivalent solder must be used, and the terminal must be dipped in the solder which been heated to 230°C±5°C for 5±1 seconds.
- Using a microscope, measure the area (%) deposited with solder. JIS specifies that more than 95% of the total area should be coated with solder.

(2) Area for soldering warranty

Soldering is warranted for a specific portion of the terminal. The warranted portion is shown in the following figure.

The tie-bar cut portion also serves as a dam to prevent the sealing resin flowing out during device fabrication; it is cut off at the end of the process. Since the terminal is exposed at the cut-off end, the area for soldering is restricted. The portion near the resin is often covered with burrs when sealing with resin; it is not in the soldering warranty area.

warranty area for soldering



Resistance to soldering heat

(1) Specification of JIS

JIS specifies the method for testing the resistance to soldering heat. This method is used for guaranteeing the IC resistance against thermal stresses by soldering. An abstract of this standard is as follows:

- Dip the device terminal only once for 10±1 seconds in a solder bath of 260°C±5°C, or for $3^{+0.5}_{0}$ seconds in a solder bath of 350°C±10°C, for a distance of up to 1 to 1.5 mm from the main body.

  For the solder flow system temperature should be 260°C±5°C. To solder by soldering iron temperature should be 350°C±10°C.
- Leave the device for more than two hours after dipping, then measure the device characteristics.
- Normally, the warranty is limited to 10 seconds at 260°C±5°C. The distance between the device main body and solder bath is 1.6 mm.

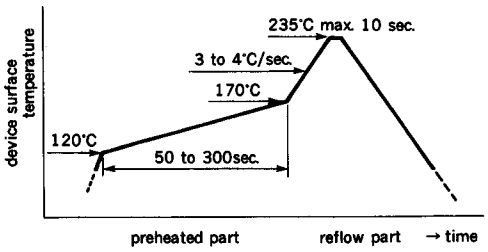
(2) Resistance to soldering heat when mounting infrared reflow.

When surface mount Devices (SOP, QFP etc) are dipped directly into a solder pot.

The device moisture resistance may deteriorate and thermal stress generate cracks in the pallet.

Carefully observe the mounting conditions.

Recommended temperature profile when mounting infrared reflows is shown in the figure below.



(3) CCD image sensor soldering

CCD image sensor cannot be guaranteed when subjected to solder flow processing because this type of soldering is known to cause cracks in the glass.

In order to prevent the solder iron and the solder from heating the device surface over 80°C, using a 30W solder iron (tip temperature: 300°C, tip diameter 4.5mm × length 32mm) and performing soldering for each terminal within 2 sec. is recommended.

5. Quality Assurance and Reliability

The Concept to Quality Assurance

There are 2 fundamental principles guiding Sony Semiconductors.

1. Customer satisfaction
2. Top level performance

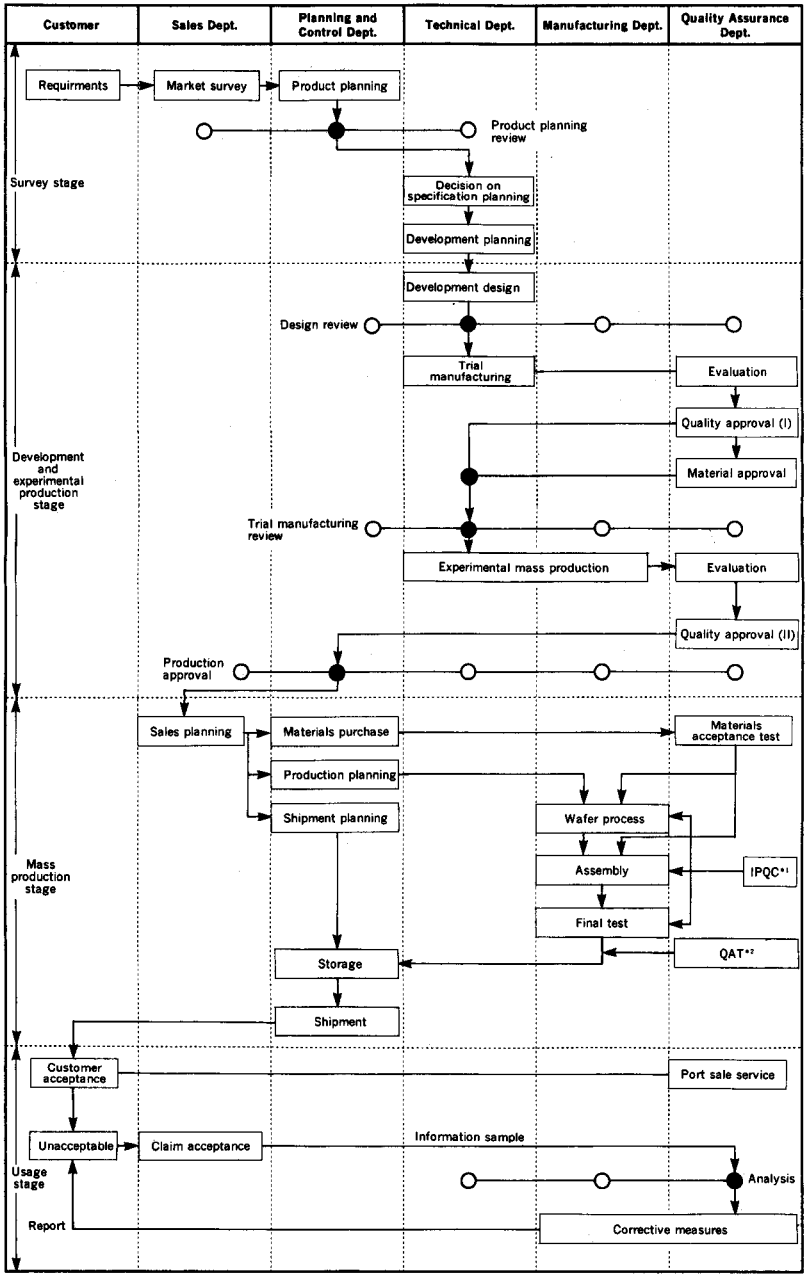
What comes first is the ability to respond convincingly to given requirements in terms of Quality, Delivery, Cost and Servicing. This involves all operations involved in the process. The second requisite is the quest for superior accomplishment. Here, talent is demanded to fulfill customer expectations, where quality is concerned, and pursue related activities.

To this effect an elaborate system of quality assurance is firmly established. From the early stages of research and development well into production, sales and servicing, orderly control is applied for the maintenance of high standards and further improvement. Systematization and automation are pushed ahead to provide a stable output of high quality production.

In this respect, the force in charge of implementing the program is nonetheless subject to constant polishing. Gifted people well aware of the problems inherent to their tasks are at the core of the excellence reflected on their yield.

With the aim of providing the most economical, the most useful and at the same time the most gratifying products where quality is the criterion, Sony keeps fueling a relentless urge for achievement.

Quality assurance system of semiconductor products



*1. IPQC: In Process Quality Control
*2. QAT: Quality Assurance Test

Quality assurance criteria and reliability test criteria

1) Quality assurance in shipping

Establishing quality in the design and in fabrication is essential to keep the quality and reliability levels of the semiconductor devices at a high level. This is done by the "Zero-defect" (ZD) movement. Further sampling checks, in units of shipping lot, is done on products that have been "totally-inspected" at the final fabrication stage, thus ensuring no detective items. This sampling inspection is done in accordance with MIL-STD-105D.

2) Reliability

The reliability test is done, periodically, to confirm reliability level.

Periodic Reliability Test

Item		Testing time	LTPD
Electrical Characteristics Test		In order to know the initial quality level, some types are selected and tested again.	
Life Test	high temperature operation	up to 1000 h	10%
	high temperature and high humidity with bias	up to 1000 h	10%
	pressure cooker *	up to 200 h	10%
Environmental Test	soldering heat resistance *	10s	15%
	heat cycle	100 cycles	15%
Mechanical Test	solderability	Japan Industrial Standard (JIS)	15%
	length strength		15%
Other Tests	If necessary, tests are selected according to JIS C7021 C7022 and EIAJ SD121 IC121.		

Note) These tests are selected by sampling standard. * Does not apply to CCD image Sensors.

LTPD: Lot Tolerance Percent Defective

These tests and inspection data are useful not only to improve design and wafer processes, but also serve to forecast reliability at the consumer level.

Reliability Test Standards

Types of test	Condition	Supply voltages	Testing time	LTPD
High temperature operation	Ta=125°C, 150°C, {85°C}	Typical	1000h	5%
High temperature with bias	Ta=125°C, 150°C, {85°C}	Typical	1000h	5%
High temperature storage	Ta=150°C, {125°C}		1000h	5%
Low temperature storage	Ta=−65°C, {−30°C}		1000h	5%
High temperature and high humidity storage	Ta=85°C 85%RH, {60°C 90%RH}		1000h	5%
High temperature and high humidity with bias	Ta=85°C 85%RH, {60°C 90%RH}	Typical	1000h	5%
Pressure cooker *	Ta=121°C 100%RH 203kPa		96h	5%
Temperature cycle	Ta=−65°C to+150°C, {−30°C to +85°C}		100c	10%
Heat shock *	Ta=−65°C to+150°C		100c	10%
Soldering heat resistance *	T solder=260°C		10s	10%
Solderability	T solder=230°C (rosin type flux)		5s	10%
Mechanical shock	X, Y, Z 15,000m/s² Half part of sinusoidal wave of 0.5ms		3times for each direction	10%
Vibration	X, Y, G 200m/s² 10Hz to 2000Hz to 10Hz (4min) Sinusoidal wave vibration		16minutes for each direction	10%
Constant acceleration	X, Y, Z 200,000m/s² Centrifugal acceleration		1minute for each direction	10%
Free fall	Free fall from the height of 75cm to maple plate		3times	10%
Lead strength (bend) (pull)	based on JIS			10%
Electrostatic strength	Device must be designed again, when electrostatic strength below standard supplying surge voltage to each pin under the condition of C=200pF and Rs=0Ω.			

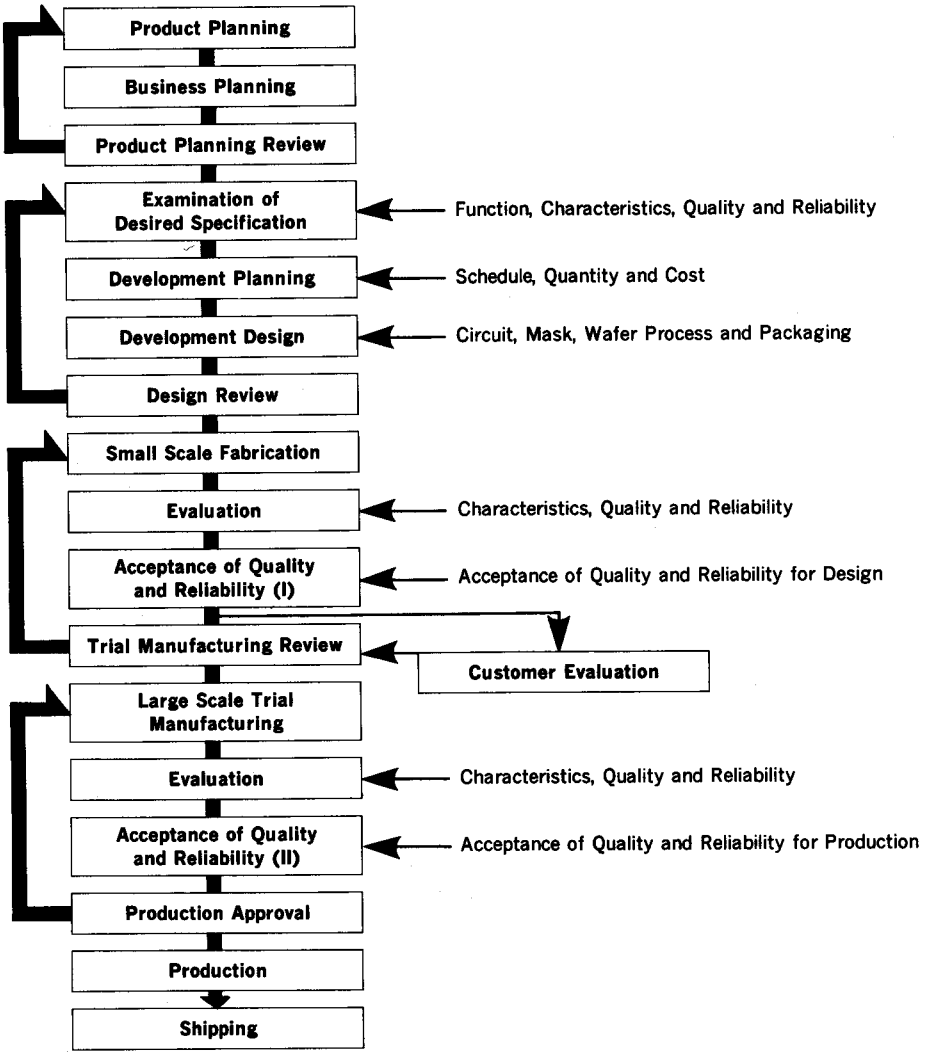
Note) LTPD: Lot Tolerance Percent Defective

* Does not apply to CCD image Sensors.

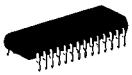
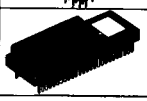
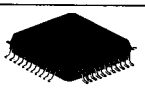
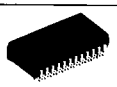
Conditions within { } apply to CCD image Sensors.

Flow Chart from Development to Manufacturing

Sony attains high quality and high reliability of semiconductor products by designing devices with quality and reliability from the initial steps of development and evaluating them sufficiently in each step of the development.



Package Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	DIP	DUAL IN-LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		SIP	SINGLE IN-LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		ZIP	ZIG-ZAG IN-LINE PACKAGE		P	2.54mm (100MIL) Zig-Zag in-line	Through Hole Lead	1-direction
		PGA	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	Package under side
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN-LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
		SZIP	SHRINK ZIG-ZAG IN-LINE PACKAGE		P	1.778mm (70MIL) Zig-Zag in-line	Through Hole Lead	1-direction
Surface mounted	Standard flat package	QFP	QUAD FLAT L-LEADED PACKAGE		P C	1.0mm 0.8mm 0.65mm	Gull-Wing	4-direction
		SOP	SMALL OUTLINE L-LEADED PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Standard 2-direction chip carrier	SOJ	SMALL OUTLINE J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull-Wing	2-direction
		TSOP	THIN SMALL OUTLINE PACKAGE		P	0.5mm (0.55mm)	Gull-Wing	2-direction
	Standard chip carrier	QFJ	QUAD FLAT J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	4-direction
		QFN	QUAD FLAT NON-LEADED PACKAGE		C	1.27mm (50MIL)	Leadless	Package under side

* P……Plastic, C……Ceramic

CCD Image Sensor (Color)

1) CCD Image Sensor (Color)

Type	Functions				Page
	Optical size	TV System	Effective pixels	Features	
ICX022BN-3	2/3 inches	NTSC	768H×493V	Complementary mosaic filter, Variable speed electronic shutter equipped	31
ICX024BN-3	2/3 inches	PAL	756H×581V	Complementary mosaic filter, Variable speed electronic shutter equipped	48
ICX026BKA	1/2 inch	NTSC	510H×492V	Complementary mosaic filter, Variable speed electronic shutter equipped	65
ICX026CKA					80
ICX027BKA	1/2 inch	PAL	500H×582V	Complementary mosaic filter, Variable speed electronic shutter equipped	95
ICX027CKA					110
ICX044BKA	1/3 inch	NTSC	510H×492V	Complementary mosaic filter, Variable speed electronic shutter equipped	125
ICX045BKA		PAL	500H×582V		142
IU022AK-30A/40A IU024AK-30A/40A	2/3 inches	NTSC	768H×493V	• Integration of CCD image sensor, quartz low pass filter, and infrared rays cut filter • Unnecessary for optical positioning	159
		PAL	756H×581V		

SONY® ICX022BN-3

Interline-type CCD Solid Image Sensor

Description

ICX022BN-3 is an interline-type CCD solid imaging device designed for color video cameras. Effective pixels number 768 horizontally and 493 vertically.

HAD (Hole Accumulation Diode) sensors are employed as photosensor elements to ensure much reduced dark current.

Color filters incorporated Ye, G, Mg and Cy are mosaic filters of high resolution and high sensitivity.

The device employs the field integration system to obtain a high resolution.

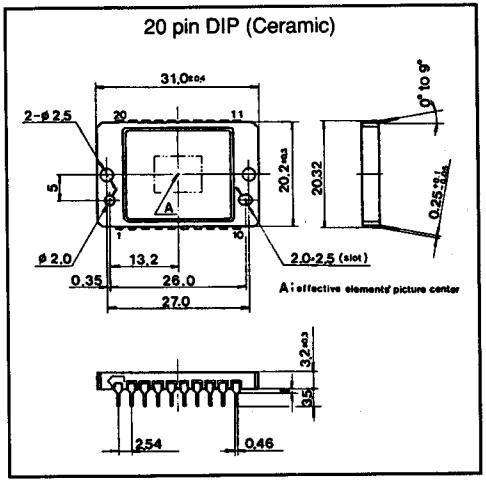
Electric charges are swept out of the substrate, so the sensor has electronic shutter capability with variable charge storage time.

Features

- Image size: 2/3 inches (8.8 mm (H) × 6.6 mm (V))
- Effective pixels: 768H × 493V
- Effective optical black
  Horizontal: Front 5 pixels
  Back 45 pixels
  Vertical: Front 16 pixels
  Back 4 pixels
- High resolution
- High sensitivity
- Low noise
- Low smear
- Low dark current
- Electronic shutter
- Low antiblooming
- No graphic distortion, no microphonic noise
- γ characteristics: 1

Package Outline

Unit: mm



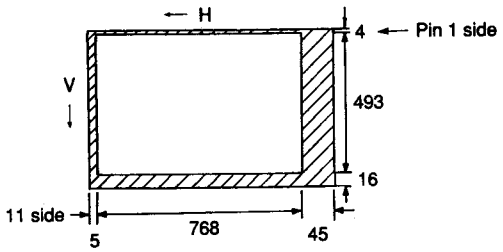


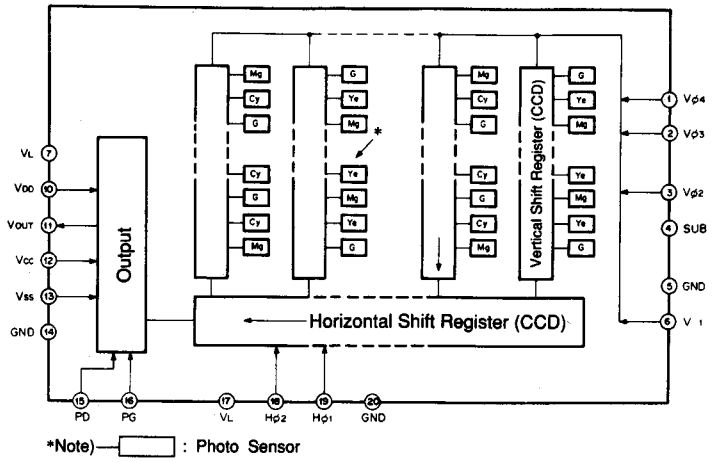
Fig. 1 Optical black configuration

Device Structure

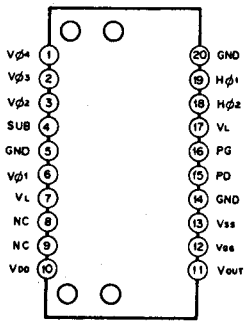
- Interline type CCD image sensor
- Chip size: 10.0 mm (H) × 8.2 mm (V)
- Unit cell size: 11.0 μm (H) × 13.0 μm (V)
- Dummy bits: Horizontal 22-bits, vertical 1-bit
  (Even fields only)
- HAD (Hole Accumulation Diode) sensor
- High sensitivity output amplifier
- Ye, Cy, Mg, G on chip type complementary color mosaic filter
- N type substrate P-well structure

E90226-YA

Imaging Device Function Block



Pin Configuration and Description (Top View)



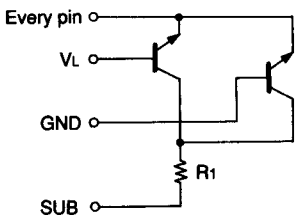
No.	Symbol	Description	No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	11	VOUT	Signal output
2	Vφ3	Vertical register transfer clock	12	VGG	Output amplifier gate
3	Vφ2	Vertical register transfer clock	13	VSS	Output amplifier source
4	SUB	Substrate (OFD) bias	14	GND	GND
5	GND	GND	15	PD	Pre-charge drain bias
6	Vφ1	Vertical register transfer clock	16	PG	Output reset clock
7	VL	Protection transistor bias	17	VL	Protection transistor bias
8	NC		18	Hφ2	Horizontal register transfer clock
9	NC		19	Hφ1	Horizontal register transfer clock
10	VDD	Output amplifier drain supply	20	GND	GND

Absolute Maximum Ratings

Item	Ratings	Unit	Remarks
SUB-GND	-0.3 to +55	V	
V_{DD}, PD, V_{OUT}, V_{SS}-GND	-0.3 to +20	V	
V_{DD}, PD, V_{OUT}, V_{SS}-SUB	-55 to +10	V	Note 1
Horizontal and vertical transfer clock inputs - GND	-15 to +20	V	
Horizontal and vertical transfer clock inputs - SUB	-65 to +10	V	Note 1
Potential difference between vertical transfer clock inputs	+15	V	Note 2
Potential difference between horizontal transfer clock inputs	+17	V	
$H\phi_1$, $H\phi_2$ - $V\phi_4$	-17 to +17	V	
PG, V_{GG} - GND	-10 to +15	V	
PG, V_{GG} - SUB	-55 to +10	V	Note 1
V_L - SUB	-65 to +0.3	V	
Pins other than GND, SUB and V_L-V_L	-0.3 to +27	V	
Storage temperature	-30 to +80	°C	
Operation guarantee ambient temperature	-10 to +55	°C	

Note) 1. This imaging device consists of an N substrate P-Well structure where a protection transistor is connected to each pin accordingly. If a voltage exceeding 10 V is applied to pins other than V_L against the SUB pin, a punch through current will flow. Since a series resistance R_L is located between each pin and SUB, the device will withstand destruction through any rush voltage over 10 V.
The series resistance R_L must be more than 1 kΩ between Vp-p and SUB, more than 500 Ω between V_{OUT} and SUB and more than 5kΩ between Vss or PD and SUB. The series resistance between other pins (except V_L and GND) and SUB must be more than 5 kΩ.

① V_{DD}, PD, V_{OUT} and Vss pins



② Pins other than ① (except V_L and GND)

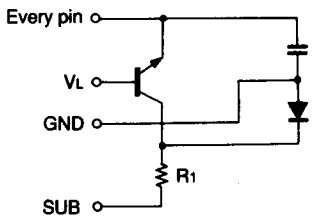


Fig. 2 Equivalent circuit

2. In case of clock width <10 µs and clock duty factor <0.1%, up to 27 V is guaranteed.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage of output circuit	V_{DD}	14.55	15.0	15.45	V	
	V_{PD}	14.55	15.0	15.45	V	Note 1
	V_{GG}	1.6	2.0	2.4	V	
	V_{SS}	Ground with a 390 Ω resistance				±5 %
Substrate voltage adjustable range	V_{SUB}	9		19	V	Note 2
Regulation range after substrate voltage adjustment	V_{SUB}	−3		3	%	
Protection transistor bias	V_L	−12	−11	Note 6	V	

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output circuit current	I_{DD}		5.0		mA	Note 3
Input current	I_{IN1}			1	μA	Note 4
	I_{IN2}			10	μA	Note 5

Note) 1. V_{PD} and V_{DD} must have the same voltage.

2. Indication of the substrate voltage (V_{SUB}) set value:
The set value is indicated on the rear of the imaging device by a code. Adjust to obtain the indicated voltage at the SUB pin.

V_{SUB} code – Two digit indication

The integral codes correspond to the following actual values:

Integral codes	9	A	B	C	D	E	F	G	H	I	J
Actual values	9	10	11	12	13	14	15	16	17	18	19

EX.) F5 → 15.5 (V)

3. Ground Vss with a 390Ω resistance.
4. 1) Current flowing to the ground when a voltage of 20 V is applied to V_{DD}, PD, V_{OUT}, Vss and SUB pins. Test ground all the pins other than those under test.
   2) Current flowing to the ground when a voltage of 25 V is applied to $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $H\phi_1$ and $H\phi_2$ pins in the order. Apply pin a voltage of 25 V to the SUB pin and ground pins other than those under test.
   3) Current flowing to the ground when a voltage of 15 V is applied to PG and V_{GG} pins in the order. Apply a voltage of 15 V to the SUB pin and ground pins other than those under test.
   4) Current flowing to the ground when V_L pin is grounded, GND and SUB pins are open and a voltage of 27 V is applied to other pins.
5. Current flowing to the ground when a voltage of 55 V is applied to the SUB pin. In this case ground pins other than those under test.
6. Vertical transfer clock low level clamp bias

Clock Voltage Conditions

Clock voltage

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Read clock voltage	V_{VT}	13.0		15.0	V	Note 1
Vertical transfer clock voltage	V_{VHH}			1.3	V	Note 2
	V_{VH}	-0.3		0.7	V	
	$V_{\phi V}$	8.0			V	
	V_{VLL}	-11.0			V	
Horizontal transfer clock voltage	V_{HHH}			5.5	V	Note 3
	V_{HL}	-3.0		-1.7	V	
	$V_{\phi H}$	5.2		8.0	V	
	V_{HLL}	-3.0			V	
Output reset clock voltage	V_{PGL}		0		V	Note 4
	$V_{\phi PG}$	7.0		13.0	V	
Substrate clock voltage	$V_{\phi SUB}$	23.0		27.0	V	Note 5

Clock capacitance

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Vertical transfer clock - GND	$C_{\phi V}$		5000		pF	
Capacitance between vertical transfer clocks	$C_{\phi VV}$		1500		pF	
Horizontal transfer clock - GND	$C_{\phi H}$		180		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Output reset clock - GND	$C_{\phi PG}$		10		pF	
Substrate clock - GND	$C_{\phi SUB}$		500		pF	

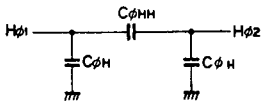


Fig. 4 Equivalent circuit of horizontal transfer clock capacitance

Note) 1. Read clock voltage

1) The symbol "ϕ_L" expresses the voltage level while the read clock "V_T" of the vertical transfer clocks ("$V\phi_1$" and "$V\phi_3$") is set. The maximum value in the read clock waveform is expressed as "ϕ_H".
2) The period in which the voltage level becomes ($\phi_H - \phi_L$)/2 is expressed as "tsr". The voltage levels at "tsr/2" are expressed as "V_{T1}" (at $V\phi_1$) and "V_{T3}" (at $V\phi_3$). The smaller of "V_{T1}" and "V_{T3}" is defined as the read clock voltage "V_{VT}".

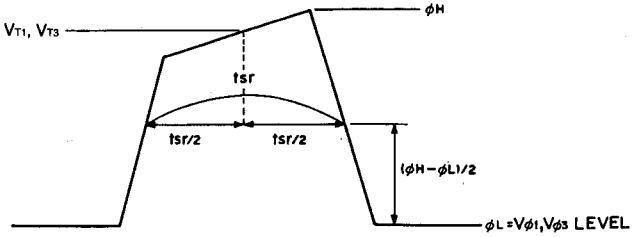


Fig. 5 Read clock waveform

2. Vertical clock voltage (Refer to Fig. 6)
T = 559 ns (with a horizontal driving frequency of 14.32 MHz)

1) Definition of the vertical transfer clock amplitude

Level 2T after the rising edge of "$V\phi_3$" is expressed as "V_{3A}".
Level T after the falling edge of "$V\phi_1$" is expressed as "V_{1B}".
Level 2T after the rising edge of "$V\phi_4$" is expressed as "V_{4A}".
Level T after the falling edge of "$V\phi_2$" is expressed as "V_{2B}".
Level 2T after the rising edge of "$V\phi_1$" is expressed as "V_{1A}".
Level T after the falling edge of "$V\phi_3$" is expressed as "V_{3B}".
Level 4T after the rising edge of "$V\phi_2$" is expressed as "V_{2A}".
Level 3T after the falling edge of "$V\phi_4$" is expressed as "V_{4B}".

$V\phi_2$ level T after the falling edge of "$V\phi_1$" is expressed as "V_{2C}".
$V\phi_3$ level T after the falling edge of "$V\phi_2$" is expressed as "V_{3C}".
$V\phi_4$ level T after the falling edge of "$V\phi_3$" is expressed as "V_{4C}".
$V\phi_1$ level 3T after the falling edge of "$V\phi_4$" is expressed as "V_{1C}".

$\Delta 31 = (V_{3A} + V_{2C}) / 2 - V_{1B}$
$\Delta 42 = (V_{4A} + V_{3C}) / 2 - V_{2B}$
$\Delta 13 = (V_{1A} + V_{4C}) / 2 - V_{3B}$
$\Delta 24 = (V_{2A} + V_{1C}) / 2 - V_{4B}$

The minimum value of these is defined as the vertical transfer clock amplitude "$V\phi_V$".

2) The maximum value from V_{1A}, V_{2A}, V_{3A}, and V_{4A}, is defined as the high level V_{VH} of the clock.
3) The minimum level in a waveform which includes the vertical clock coupling is expressed as "V_{VLL}". "V_{VHH}" expresses the maximum level except in the period where read clock V_T is applied (in $V\phi_1$ and $V\phi_3$ only).

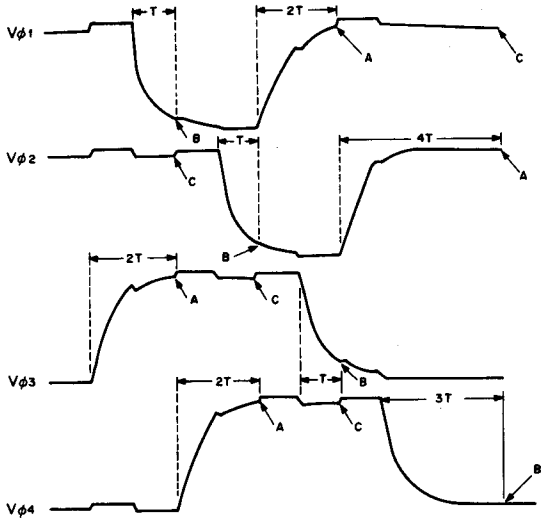


Fig. 6 Vertical transfer clock waveform
T = 559ns (with a horizontal driving frequency of 4 fsc)

3. Horizontal transfer clock voltage
   1) For the horizontal transfer clocks "Hφ1" and "Hφ2", the low-level period is expressed as "thl" and the high-level period is expressed as "thh". The symbol "tho" expresses the overlap period of "thl" and "thh".
   2) The low level at which "thl", "thh" and "tho" satisfy the following time duration is expressed as "H_{1B}" and "H_{2B}".
      And the high level is expressed as "H_{1A}" and "H_{2A}"

      thl ≥ 10 ns, thh ≥ 10 ns, tho ≥ 5 ns

      $\Delta 21 = H_{1A} - H_{2B}$
      $\Delta 12 = H_{2A} - H_{1B}$

      The smaller of Δ21 and Δ12 is defined as the horizontal transfer clock amplitude "$V_{\phi H}$". The low level at that point is expressed as "V_{HL}".
   3) The minimum level in the waveform which contains the coupling of the horizontal transfer clocks "Hφ1" and "Hφ2" is expressed as "V_{HLL}" and the minimum level is expressed as "V_{HHH}".

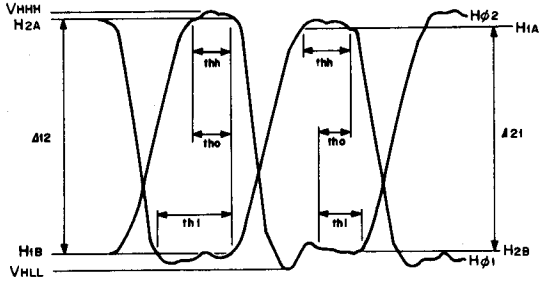


Fig. 7 Horizontal transfer clock waveform

4. Output reset clock voltage
   1) The low level of the output reset clock is to be the GND in the circuit.
   2) The amplitude of the output reset PG clock "$V\phi_{PG}$" is defined as the maximum value of the amplitude which provides a high level period over 10 ns.

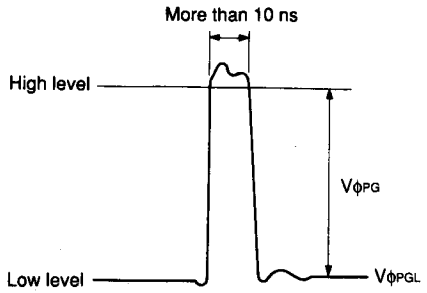


Fig. 8 Waveform of PG clock

5. Substrate clock voltage
   1) Substrate voltage is expressed as ϕ_L, and the substrate clock waveform maximum value as ϕ_H.
   2) The period where voltage level turns to $(\phi_H-\phi_L)/2$ is expressed as tsr. The difference between ϕ_L and voltage level at tsr/2 is defined as the substrate clock voltage $V\phi_{SUB}$.

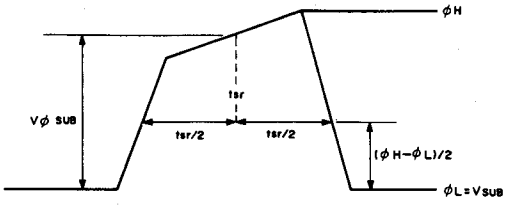


Fig. 9 Substrate clock waveform

Driving Clock Waveform Conditions

1. Definition of ϕ_H (100%) and ϕ_L (0%)
   1) For the horizontal transfer clocks ($H\phi_1$, $H\phi_2$), output reset clock ($PG\phi$) and vertical transfer clocks ($V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$), the maximum value in the clock waveform which includes no coupling is expressed as "ϕ_H" and the minimum value is expressed as "ϕ_L".
   2) For the read clock (V_T), the maximum value in the clock waveform is expressed as "ϕ_H"."ϕ_L" expresses the voltage level while the read clock (V_T) of the vertical transfer clocks ($V\phi_1$, $V\phi_2$) is applied.
   3) For the substrate clock ($SUB\phi$), the maximum value in the clock waveform is expressed as "ϕ_H" and the substrate voltage (V_{SUB}) as "ϕ_L".

2. Standard driving clock conditions (Typ.)

Horizontal drive frequency: 14.32 MHz

Clock (Symbol)	twh	twl	tr	tf	Unit	Remarks
Hφ1	18	33.7	10	8	ns	Imaging period
Hφ2	18	33.7	10	8		
Hφ1	4.9		0.01	0.01	μs	Parallel-serial converting period
Hφ2		4.9	0.01	0.01		
φPG	12	53.7	2	2	ns	
Vφ1/Vφ2	61.6	1.6	0.1	0.1	μs	Imaging period
Vφ3/Vφ4	2.8	60.45	0.05	0.1		
Vφt	2.4		0.2	0.1		Reading period
SUBφ	1.0		0.08	0.1	μs	Electron drained into substrate period

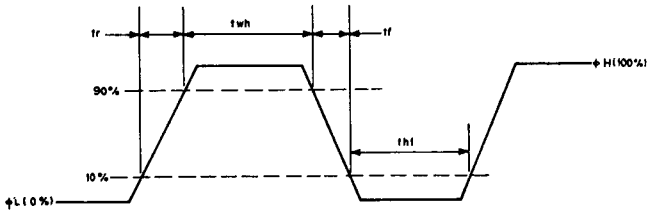


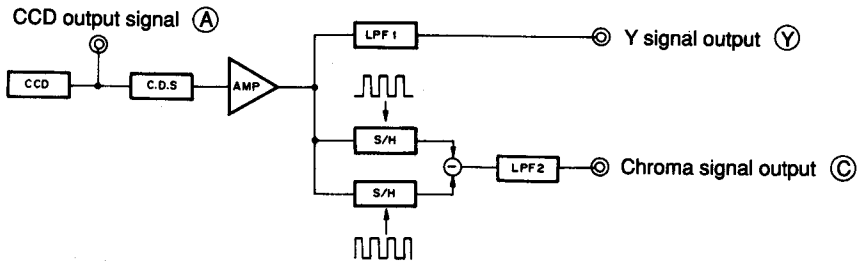
Fig. 10 Clock waveform

Imaging Characteristics

(See Fig. 10.)
Ta=25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Testing method	Remarks
Sensitivity	Sy	260	330		mV	1	
Output saturation signal	Ysat	600			mV	2	Ta=55°C
Smear	SM		0.005	0.012	%	3	
Blooming margin		1000			times	4	
Video signal shading	SHy			20	%	5	Zone ϕ, I
				25	%	5	Zone ϕ to II
Uniformity between signal channels	ΔSr			10	%	6	
	ΔSb			10	%	6	
Dark signal	Ydt			2	mV	7	Ta=55°C
Dark signal shading	ΔYdt			1	mV	8	Ta=55°C
Flicker Y	Fy			2	%	9	
R-Y	Fcr			5	%	9	
B-Y	Fcb			5	%	9	
Horizontal stripes R	Lcr			3.0	%	10	
G	Lcg			3.0	%	10	
B	Lcb			3.0	%	10	
W	Lcw			3.0	%	10	
Lag	ΔYlag			0.5	%	11	

Test Circuit



Note) Adjust AMP amplifier so that total gains between Ⓐ and Ⓨ and between Ⓐ and Ⓒ equal 1.

Test Method

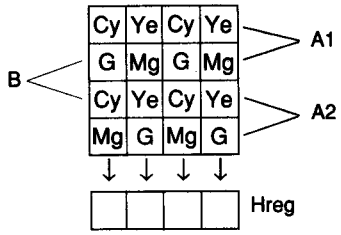
Test conditions

1) Through the following tests the substrate voltage should set to the value displayed on the device, while the device drive conditions should be kept within the range of the bias and clock voltage conditions.

2) Through the following tests defects are excluded and, unless otherwise specified the optical black level (Hence forth referred to as OPB) is set as the reference for the signal output which is taken as the Y signal output or the Chroma signal output of the testing system.

Color coding of CFA (Color Filter Array) & Composition of luminance (Y) and chrominance (C) signals.

CFA of this imager is shown in the Figure. This complementary CFA is used with a "field integration mode", where all of the photosites are read out during each video field. Signals from two vertically adjacent photosites, such as line A1 or A2 for field A, are summed when the image charge is transferred into the vertical storage columns. The readout line pairing is shifted down one line for field B. The sensor output signals through Horizontal register (H reg.) at line A1 are



Color Coding Diagram

[G+Cy], [Mg+Ye], [G+Cy], [Mg+Ye].

These signals are processed in order to compose Y and C signals. By adding the two adjacent signals at line A1, Y signal is formed as follows:

$$Y = \{(G+Cy) + (Mg+Ye)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

C signal is composed by subtracting the two adjacent signals at line A1.

$$R - Y = \{(Mg+Ye) - (G+Cy)\}$$
$$= \{2R-G\}$$

Next, the signals through H reg. at line A2 are

[Mg+Cy], [G+Ye], [Mg+Cy], [G+Ye]

Similarly, Y and C signals are composed at line A2.

$$Y = \{(G+Ye) + (Mg+Cy)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

$$-(B-Y) = \{(G+Ye) - (Mg+Cy)\}$$
$$= -\{2B-G\}$$

Accordingly, Y signal is balanced in relation to the scanning lines, and C signal takes the form of R–Y and –(B–Y) on alternate lines.
It is the same for B field.

Definition of standard imaging conditions

① Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 Nit, 3200K Halogen source), at F5.6 with a typical test lens, and CM-500S (1.0 mmt) for IR cut filter.

② Standard imaging condition II: Use a light source with uniformity within 2%, color temperature of 3200K and CM-500S (1.0 mmt) as IR cut filter. The light intensity is adjusted in accordance with the average value of Y signals (Y_A) indicated in each item.

1) Set to standard imaging condition I and measure Y signal (S) at the center of the screen.

2) Set to imaging condition II. Adjust light intensity to 10 times when Y signal output average value Y_A=200mV. Then test Y signal Min. Value.

3) Set to imaging condition II. Adjust light intensity to 500 times when Y signal output average value Y_A=200mV. Stop Read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the Max. value Y_{SM} of Ysignal output.

$$SM = (Y_{SM}/Y_A) \times {}^1/_{500} \times {}^1/_{10} \times 100\ (\%) \quad ({}^1/_{10}V)$$

4) Set to imaging condition II. Adjust light intensity to 1000 times when Y signal output average value Y_A=200mV. Then check that there is no blooming.

5) Video signal shading SHy
Set to standard imaging condition II. Test Y signal Max. (Y max.) and Min. (Y min.) values. Adjust light intensity to obtain a Y signal output average value (Y_A) of about 150mV.

$$SHy = (Ymax - Ymin)/Y_A \times 100\ (\%)$$

6) Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 200mV. Test the Max. (Cr max. and Cb max.) and Min. (Cr min. and Cb min.) values of C signals from R-Y and B-Y channels.

$$\Delta Sr = |\ (Crmax - Crmin)/Y_A\ | \times 100\ (\%)$$
$$\Delta Sb = |\ (Cbmax - Cbmin)/Y_A\ | \times 100\ (\%)$$

7) Test the average Y signal voltage when the device ambient temperature is at 55°C and light is obstructed with horizontal idle transfer level as reference.

8) Following 7, test Max. (Ydmax.) and Min. (Ydmin.) values of Y signal output. Only keep spot defects out of this range.

$$\Delta Ydt = Ydmax - Ydmin$$

9) ① Fy
Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 200 mV. Test the Y signal difference (ΔYf) between even field and odd field.

$$Fy = (\Delta Yf/Y_A) \times 100\ (\%)$$

② Fcr, Fcb
Set to standard imaging condition II. Insert R and B filter respectively, and test the C signal difference (ΔCr, ΔCb) between even field and odd field and the C signal output average value (C_{Ar}, C_{Ab}). At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

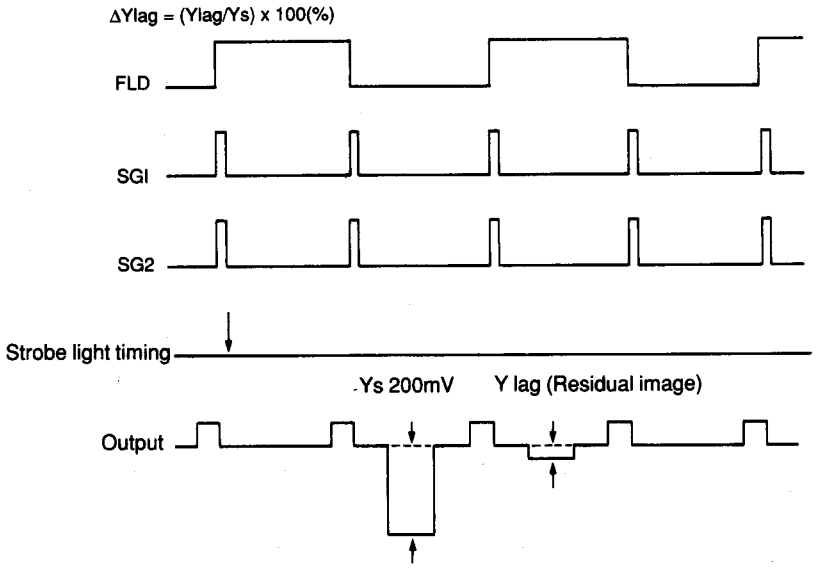
$$Fci = (\Delta Ci/C_{Ai}) \times 100\ (\%) \quad (i = r, b)$$

10) Set to standard imaging condition II. Insert W, R, G and B filters respectively, and test the signal difference (ΔYlw, ΔYlr, ΔYlg, ΔYlb) between Y signal lines of the same field. At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

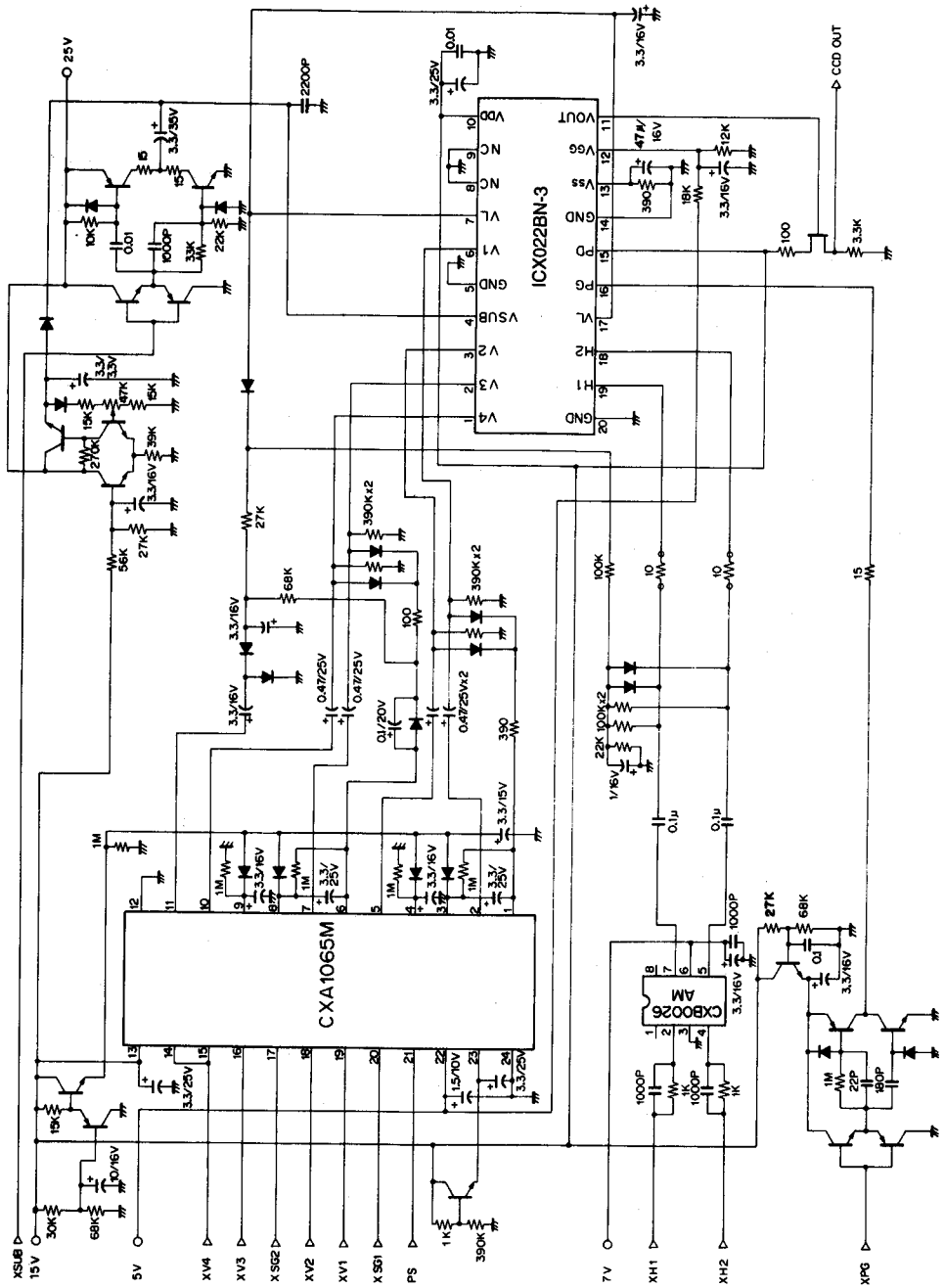
$$Lci = (\Delta Yli/Y_A) \times 100\ (\%) \quad (i = w, r, g, b)$$

11) Light a stroboscopic tube with the following timing and test the residual image.

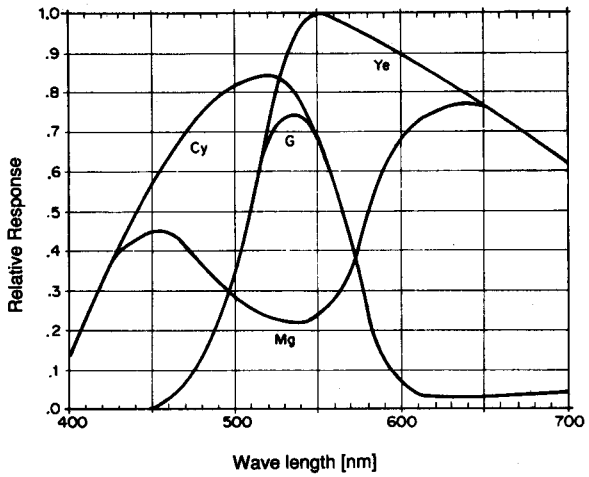
$$\Delta Ylag = (Ylag/Ys) \times 100\ (\%)$$



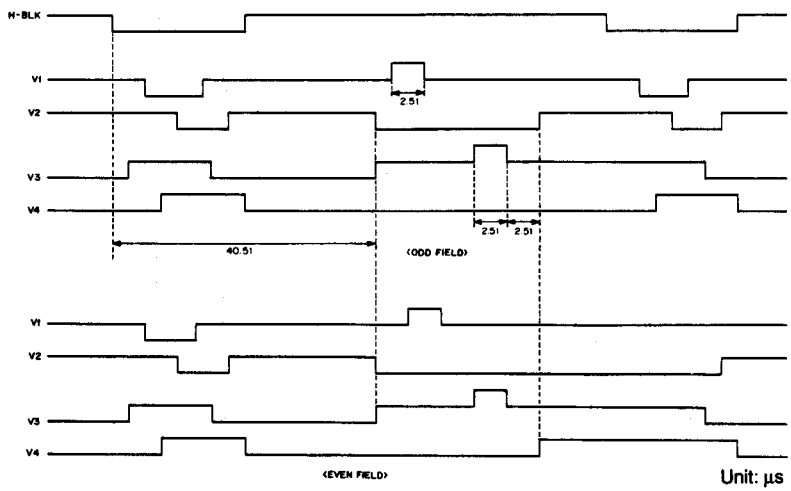
Drive Circuit



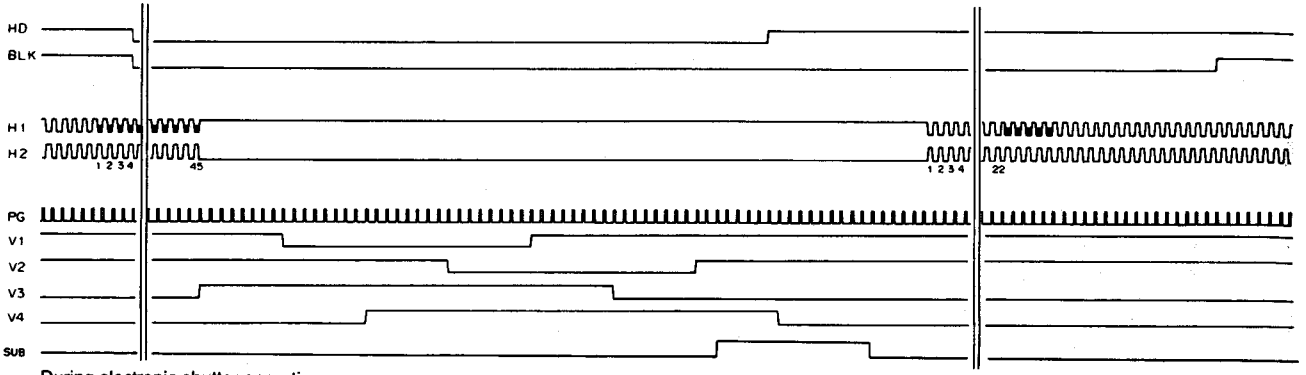
Spectral Sensitivity Characteristics (Excluding light source characteristics)
Fujinon lens H6 × 12.5R



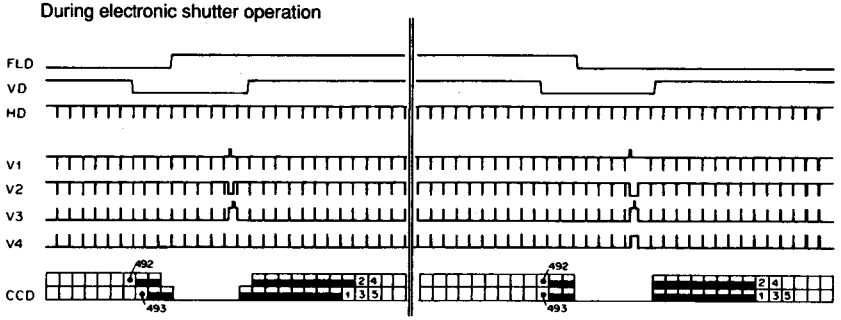
Using read out clock timing chart



Drive Pulse Timing Chart



During electronic shutter operation



Handling Instructions

1) Static charge prevention
CCD image sensor are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount cool sufficiently.
c) To dismount an imaging device do not use a solder pult. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

7) Defect compensation ROM
This is shipped in its own case in pair with the CCD image sensor. Pair with the CCD image sensor bearing the same serial number during mounting. When the CCD image sensor has no defect there is no ROM or serial number.

ICX024BN-3

Interline-type CCD Solid Image Sensor

Description

ICX024BN-3 is an interline-type CCD solid imaging device designed for color video cameras. Effective pixels number 756 horizontally and 581 vertically.

HAD (Hole Accumulation Diode) sensors are employed as photosensor elements to ensure much reduced dark current.

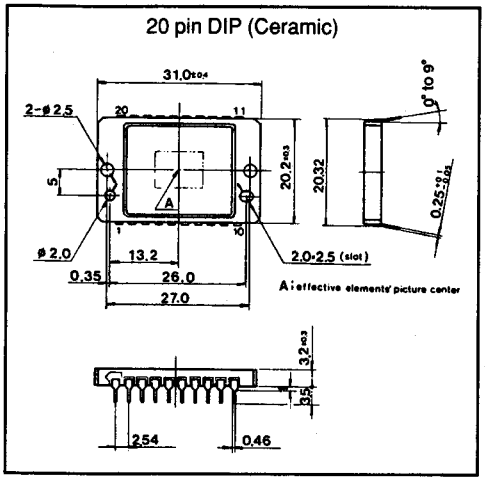
Color filters incorporated Ye, G, Mg and Cy are mosaic filters of high resolution and high sensitivity.

The device employs the field integration system to obtain a high resolution.

Electric charges are swept out of the substrate, so the sensor has electronic shutter capability with variable charge storage time.

Package Outline

Unit: mm



Features

- Image size: 2/3 inches (8.8 mm (H) × 6.6 mm (V))
- Effective pixels: 756H × 581V
- Effective optical black
  - Horizontal: Front 5 pixels
  - Back 55 pixels
  - Vertical: Front 16 pixels
  - Back 6 pixels
- High resolution
- High sensitivity
- Low noise
- Low smear
- Low dark current
- Electronic shutter
- Low antiblooming
- No graphic distortion, no microphonic noise
- γ characteristics: 1

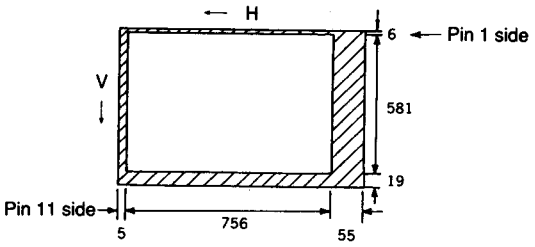


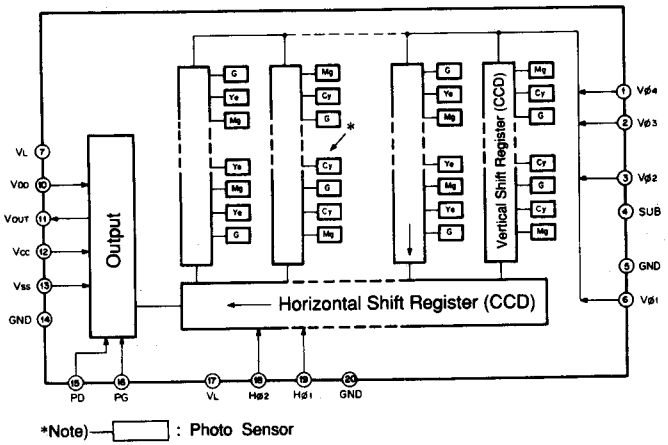
Fig. 1 Optical black configuration

Device Structure

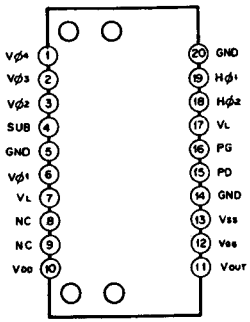
- Interline type CCD image sensor
- Chip size: 10.0 mm (H) × 8.2 mm (V)
- Unit cell size: 11.0 μm (H) × 11.0 μm (V)
- Dummy bits: Horizontal 22-bits, vertical 1-bit (Even fields only)
- HAD (Hole Accumulation Diode) sensor
- High sensitivity output amplifier
- Ye, Cy, Mg, G on chip type complementary color mosaic filter
- N type substrate P-well structure

E90263-YA

Imaging Device Function Block



Pin Configuration and Description (Top View)



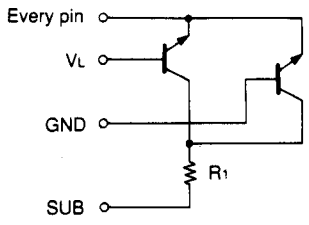
No.	Symbol	Description	No.	Symbol	Description
1	$V\phi_4$	Vertical register transfer clock	11	V_{OUT}	Signal output
2	$V\phi_3$	Vertical register transfer clock	12	V_{GG}	Output amplifier gate
3	$V\phi_2$	Vertical register transfer clock	13	V_{SS}	Output amplifier source
4	SUB	Substrate (OFD) bias	14	GND	GND
5	GND	GND	15	PD	Pre-charge drain bias
6	$V\phi_1$	Vertical register transfer clock	16	PG	Output reset clock
7	V_L	Protection transistor bias	17	V_L	Protection transistor bias
8	NC		18	$H\phi_2$	Horizontal register transfer clock
9	NC		19	$H\phi_1$	Horizontal register transfer clock
10	V_{DD}	Output amplifier drain supply	20	GND	GND

Absolute Maximum Ratings

Item	Ratings	Unit	Remarks
SUB-GND	-0.3 to +55	V	
V_{DD}, PD, V_{OUT}, Vss-GND	-0.3 to +20	V	
V_{DD}, PD, V_{OUT}, Vss-SUB	-55 to +10	V	Note 1
Horizontal and vertical transfer clock inputs - GND	-15 to +20	V	
Horizontal and vertical transfer clock inputs - SUB	-65 to +10	V	Note 1
Potential difference between vertical transfer clock inputs	+15	V	Note 2
Potential difference between horizontal transfer clock inputs	+17	V	
$H\phi_1$, $H\phi_2$ - $V\phi_4$	-17 to +17	V	
PG, V_{GG} - GND	-10 to +15	V	
PG, V_{GG} - SUB	-55 to +10	V	Note 1
V_L - SUB	-65 to +0.3	V	
Pins other than GND, SUB and V_L-V_L	-0.3 to +27	V	
Storage temperature	-30 to +80	°C	
Operation guarantee ambient temperature	-10 to +55	°C	

Note) 1. This imaging device consists of an N substrate P-Well structure where a protection transistor is connected to each pin accordingly. If a voltage exceeding 10 V is applied to pins other than V_L against the SUB pin, a punch through current will flow. Since a series resistance R_L is located between each pin and SUB, the device will withstand destruction through any rush voltage over 10 V.
The series resistance R_L must be more than 1 kΩ between Vp-p and SUB, more than 500 Ω between V_{OUT} and SUB and more than 5kΩ between Vss or PD and SUB. The series resistance between other pins (except V_L and GND) and SUB must be more than 5 kΩ.

① V_{DD}, PD, V_{OUT} and Vss pins



② Pins other than ① (except V_L and GND)

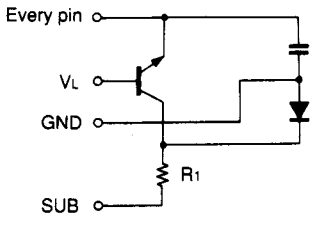


Fig. 2 Equivalent circuit

2. In case of clock width <10 µs and clock duty factor <0.1%, up to 27 V is guaranteed.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage of output circuit	V_{DD}	14.55	15.0	15.45	V	
	V_{PD}	14.55	15.0	15.45	V	Note 1
	V_{GG}	1.6	2.0	2.4	V	
	V_{SS}	Ground with a 390 Ω resistance				±5 %
Substrate voltage adjustable range	V_{SUB}	9		19	V	Note 2
Regulation range after substrate voltage adjustment	V_{SUB}	−3		3	%	
Protection transistor bias	V_L	−12	−11	Note 6	V	

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output circuit current	I_{DD}		5.0		mA	Note 3
Input current	I_{IN1}			1	μA	Note 4
	I_{IN2}			10	μA	Note 5

Note) 1. V_{PD} and V_{DD} must have the same voltage.

2. Indication of the substrate voltage (V_{SUB}) set value:
The set value is indicated on the rear of the imaging device by a code. Adjust to obtain the indicated voltage at the SUB pin.

V_{SUB} code – Two digit indication

The integral codes correspond to the following actual values:

Integral codes	9	A	B	C	D	E	F	G	H	I	J
Actual values	9	10	11	12	13	14	15	16	17	18	19

EX.) F5 → 15.5 (V)

3. Ground Vss with a 390Ω resistance.
4. 1) Current flowing to the ground when a voltage of 20 V is applied to V_{DD}, PD, V_{OUT}, V_{SS} and SUB pins. Test ground all the pins other than those under test.
   2) Current flowing to the ground when a voltage of 25 V is applied to $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $H\phi_1$ and $H\phi_2$ pins in the order. Apply pin a voltage of 25 V to the SUB pin and ground pins other than those under test.
   3) Current flowing to the ground when a voltage of 15 V is applied to PG and V_{GG} pins in the order. Apply a voltage of 15 V to the SUB pin and ground pins other than those under test.
   4) Current flowing to the ground when V_L pin is grounded, GND and SUB pins are open and a voltage of 27 V is applied to other pins.
5. Current flowing to the ground when a voltage of 55 V is applied to the SUB pin. In this case ground pins other than those under test.
6. Vertical transfer clock low level clamp bias

Clock Voltage Conditions
Clock voltage

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Read clock voltage	V_{VT}	13.0		15.0	V	Note 1
Vertical transfer clock voltage	V_{VHH}			1.3	V	Note 2
	V_{VH}	-0.3		0.7	V	
	V_{oV}	8.0			V	
	V_{VLL}	-11.0			V	
Horizontal transfer clock voltage	V_{HHH}			5.5	V	Note 3
	V_{HL}	-3.0		-1.7	V	
	V_{oH}	5.2		8.0	V	
	V_{HLL}	-3.0			V	
Output reset clock voltage	V_{PGL}		0		V	Note 4
	V_{oPG}	7.0		13.0	V	
Substrate clock voltage	V_{oSUB}	23.0		27.0	V	Note 5

Clock capacitance

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Vertical transfer clock - GND	C_{oV}		5000		pF	
Capacitance between vertical transfer clocks	C_{oVV}		1500		pF	
Horizontal transfer clock - GND	C_{oH}		180		pF	
Capacitance between horizontal transfer clocks	C_{oHH}		50		pF	
Output reset clock - GND	C_{oPG}		10		pF	
Substrate clock - GND	C_{oSUB}		500		pF	

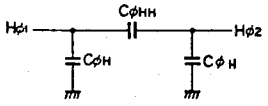


Fig. 4 Equivalent circuit of horizontal transfer clock capacitance

Note) 1. Read clock voltage

1) The symbol "ϕ_L" expresses the voltage level while the read clock "V_T" of the vertical transfer clocks ("$V\phi_1$" and "$V\phi_3$") is set. The maximum value in the read clock waveform is expressed as "ϕ_H".
2) The period in which the voltage level becomes ($\phi_H - \phi_L$)/2 is expressed as "tsr". The voltage levels at "tsr/2" are expressed as "V_{T1}" (at $V\phi_1$) and "V_{T3}" (at $V\phi_3$). The smaller of "V_{T1}" and "V_{T3}" is defined as the read clock voltage "V_{VT}".

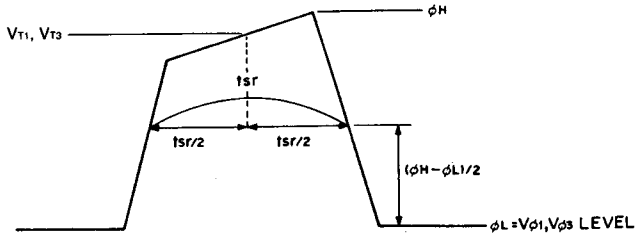


Fig. 5 Read clock waveform

2. Vertical clock voltage (Refer to Fig. 6)
T = 564 ns (with a horizontal driving frequency of 14.19 MHz)

1) Definition of the vertical transfer clock amplitude

Level 2T after the rising edge of "$V\phi_3$" is expressed as "V_{3A}".
Level T after the falling edge of "$V\phi_1$" is expressed as "V_{1B}".
Level 2T after the rising edge of "$V\phi_4$" is expressed as "V_{4A}".
Level T after the falling edge of "$V\phi_2$" is expressed as "V_{2B}".
Level 2T after the rising edge of "$V\phi_1$" is expressed as "V_{1A}".
Level T after the falling edge of "$V\phi_3$" is expressed as "V_{3B}".
Level 4T after the rising edge of "$V\phi_2$" is expressed as "V_{2A}".
Level 3T after the falling edge of "$V\phi_4$" is expressed as "V_{4B}".

$V\phi_2$ level T after the falling edge of "$V\phi_1$" is expressed as "V_{2C}".
$V\phi_3$ level T after the falling edge of "$V\phi_2$" is expressed as "V_{3C}".
$V\phi_4$ level T after the falling edge of "$V\phi_3$" is expressed as "V_{4C}".
$V\phi_1$ level 3T after the falling edge of "$V\phi_4$" is expressed as "V_{1C}".

$\Delta 31 = (V_{3A} + V_{2C}) / 2 - V_{1B}$
$\Delta 42 = (V_{4A} + V_{3C}) / 2 - V_{2B}$
$\Delta 13 = (V_{1A} + V_{4C}) / 2 - V_{3B}$
$\Delta 24 = (V_{2A} + V_{1C}) / 2 - V_{4B}$

The minimum value of these is defined as the vertical transfer clock amplitude "$V\phi v$".

2) The maximum value from V_{1A}, V_{2A}, V_{3A}, and V_{4A}, is defined as the high level V_{VH} of the clock.
3) The minimum level in a waveform which includes the vertical clock coupling is expressed as "V_{VLL}". "V_{VHH}" expresses the maximum level except in the period where read clock V_T is applied (in $V\phi_1$ and $V\phi_3$ only).

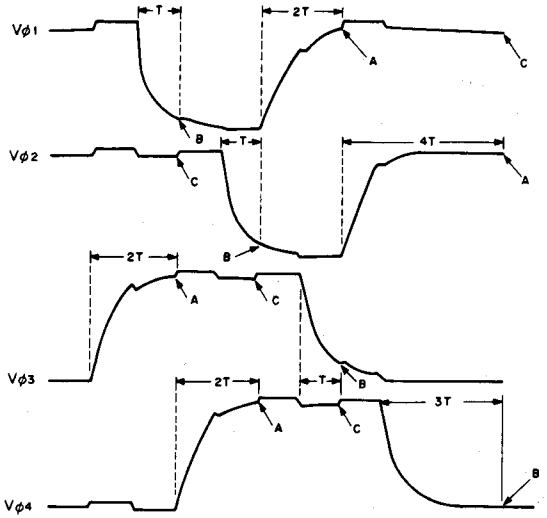


Fig. 6 Vertical transfer clock waveform
T = 564ns (with a horizontal driving frequency of 14.19 MHz)

3. Horizontal transfer clock voltage
   1) For the horizontal transfer clocks "Hφ1" and "Hφ2", the low-level period is expressed as "thl" and the high-level period is expressed as "thh". The symbol "tho" expresses the overlap period of "thl" and "thh".
   2) The low level at which "thl", "thh" and "tho" satisfy the following time duration is expressed as "H_{1B}" and "H_{2B}".
      And the high level is expressed as "H_{1A}" and "H_{2A}"

      thl ≥ 10 ns, thh ≥ 10 ns, tho ≥ 5 ns

      $\Delta 21 = H_{1A} - H_{2B}$
      $\Delta 12 = H_{2A} - H_{1B}$

      The smaller of Δ21 and Δ12 is defined as the horizontal transfer clock amplitude "$V\phi_H$". The low level at that point is expressed as "V_{HL}".
   3) The minimum level in the waveform which contains the coupling of the horizontal transfer clocks "Hφ1" and "Hφ2" is expressed as "V_{HLL}" and the minimum level is expressed as "V_{HHH}".

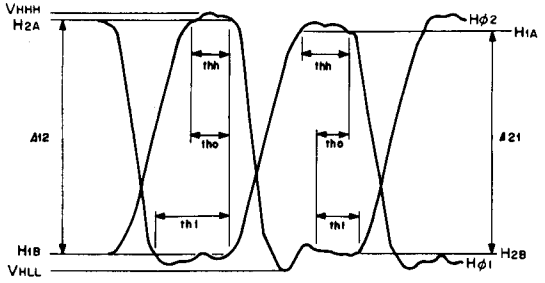


Fig. 7 Horizontal transfer clock waveform

4. Output reset clock voltage
   1) The low level of the output reset clock is to be the GND in the circuit.
   2) The amplitude of the output reset PG clock "$V\phi_{PG}$" is defined as the maximum value of the amplitude which provides a high level period over 10 ns.

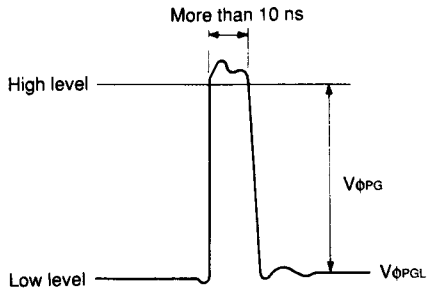


Fig. 8 Waveform of PG clock

5. Substrate clock voltage
   1) Substrate voltage is expressed as ϕ_L, and the substrate clock waveform maximum value as ϕ_H.
   2) The period where voltage level turns to $(\phi_H-\phi_L)/2$ is expressed as tsr. The difference between ϕ_L and voltage level at tsr/2 is defined as the substrate clock voltage $V\phi_{SUB}$.

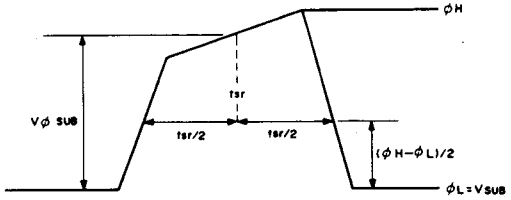


Fig. 9 Substrate clock waveform

Driving Clock Waveform Conditions

1. Definition of ϕ_H (100%) and ϕ_L (0%)
   1) For the horizontal transfer clocks ($H\phi_1$, $H\phi_2$), output reset clock ($PG\phi$) and vertical transfer clocks ($V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$), the maximum value in the clock waveform which includes no coupling is expressed as "ϕ_H" and the minimum value is expressed as "ϕ_L".
   2) For the read clock (V_T), the maximum value in the clock waveform is expressed as "ϕ_H"."ϕ_L" expresses the voltage level while the read clock (V_T) of the vertical transfer clocks ($V\phi_1$, $V\phi_2$) is applied.
   3) For the substrate clock ($SUB\phi$), the maximum value in the clock waveform is expressed as "ϕ_H" and the substrate voltage (V_{SUB}) as "ϕ_L".

2. Standard driving clock conditions (Typ.)

Horizontal drive frequency: 14.19 MHz

Clock (Symbol)	twh	twl	tr	tf	Unit	Remarks
Hφ1	18	33.7	10	8	ns	Imaging period
Hφ2	18	33.7	10	8		
Hφ1	4.9		0.01	0.01	µs	Parallel-serial converting period
Hφ2		4.9	0.01	0.01		
φPG	12	53.7	2	2	ns	
Vφ1/Vφ2	61.6	1.6	0.1	0.1	µs	Imaging period
Vφ3/Vφ4	2.8	60.45	0.05	0.1		
VφT	2.4		0.2	0.1		Reading period
SUBφ	1.0		0.08	0.1		Electron drained into substrate period

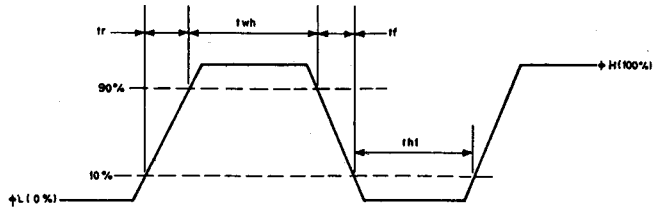


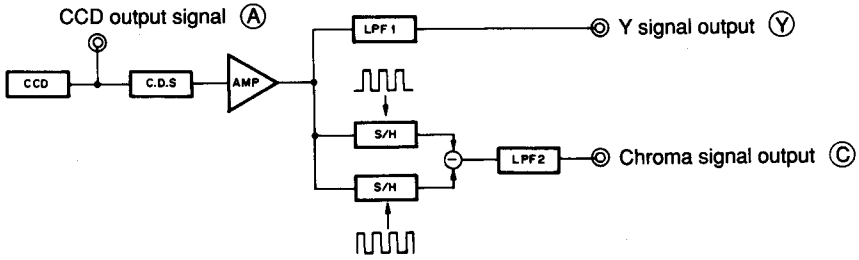
Fig. 10 Clock waveform

Imaging Characteristics

(See Fig. 10.)
Ta=25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Testing method	Remarks
Sensitivity	Sy	260	330		mV	1	
Output saturation signal	Ysat	500			mV	2	Ta=55°C
Smear	SM		0.005	0.012	%	3	
Blooming margin		800			times	4	
Video signal shading	SHy			20	%	5	Zone ϕ, I
				25	%	5	Zone ϕ to II′
Uniformity between signal channels	ΔSr			10	%	6	
	ΔSb			10	%	6	
Dark signal	Ydt			2	mV	7	Ta=55°C
Dark signal shading	ΔYdt			1	mV	8	Ta=55°C
Flicker Y	Fy			2	%	9	
R-Y	Fcr			5	%	9	
B-Y	Fcb			5	%	9	
Horizontal stripes R	Lcr			3.0	%	10	
G	Lcg			3.0	%	10	
B	Lcb			3.0	%	10	
W	Lcw			3.0	%	10	
Lag	ΔYlag			0.5	%	11	

Test Circuit



Note) Adjust AMP amplifier so that total gains between Ⓐ and Ⓨ and between Ⓐ and Ⓒ equal 1.

Test Method

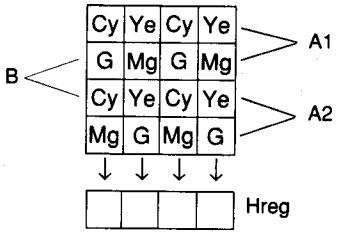
Test conditions

1) Through the following tests the substrate voltage should set to the value displayed on the device, while the device drive conditions should be kept within the range of the bias and clock voltage conditions.

2) Through the following tests defects are excluded and, unless otherwise specified the optical black level (Hence forth referred to as OPB) is set as the reference for the signal output which is taken as the Y signal output or the Chroma signal output of the testing system.

Color coding of CFA (Color Filter Array) & Composition of luminance (Y) and chrominance (C) signals.

CFA of this imager is shown in the Figure. This complementary CFA is used with a "field integration mode", where all of the photosites are read out during each video field. Signals from two vertically adjacent photosites, such as line A1 or A2 for field A, are summed when the image charge is transferred into the vertical storage columns. The readout line pairing is shifted down one line for field B. The sensor output signals through Horizontal register (H reg.) at line A1 are



Color Coding Diagram

[G+Cy], [Mg+Ye], [G+Cy], [Mg+Ye].

These signals are processed in order to compose Y and C signals. By adding the two adjacent signals at line A1, Y signal is formed as follows:

$$Y = \{(G+Cy) + (Mg+Ye)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

C signal is composed by subtracting the two adjacent signals at line A1.

$$R - Y = \{(Mg+Ye) - (G+Cy)\}$$
$$= \{2R-G\}$$

Next, the signals through H reg. at line A2 are

[Mg+Cy], [G+Ye], [Mg+Cy], [G+Ye]

Similarly, Y and C signals are composed at line A2.

$$Y = \{(G+Ye) + (Mg+Cy)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

$$-(B-Y) = \{(G+Ye) - (Mg+Cy)\}$$
$$= -\{2B-G\}$$

Accordingly, Y signal is balanced in relation to the scanning lines, and C signal takes the form of R–Y and –(B–Y) on alternate lines.
It is the same for B field.

Definition of standard imaging conditions

① Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 Nit, 3200K Halogen source), at F5.6 with a typical test lens, and CM-500S (1.0 mmt) for IR cut filter.

② Standard imaging condition II: Use a light source with uniformity within 2%, color temperature of 3200K and CM-500S (1.0 mmt) as IR cut filter. The light intensity is adjusted in accordance with the average value of Y signals (Y_A) indicated in each item.

1) Set to standard imaging condition I and measure Y signal (S) at the center of the screen.

2) Set to imaging condition II. Adjust light intensity to 10 times when Y signal output average value Y_A=200mV. Then test Y signal Min. Value.

3) Set to imaging condition II. Adjust light intensity to 500 times when Y signal output average value Y_A=200mV. Stop Read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the Max. value Y_{SM} of Ysignal output.

$$SM = (Y_{SM}/Y_A) \times {}^1/_{500} \times {}^1/_{10} \times 100\ (\%) \quad ({}^1/_{10}V)$$

4) Set to imaging condition II. Adjust light intensity to 1000 times when Y signal output average value Y_A=200mV. Then check that there is no blooming.

5) Video signal shading SHy
Set to standard imaging condition II. Test Y signal Max. (Y max.) and Min. (Y min.) values. Adjust light intensity to obtain a Y signal output average value (Y_A) of about 150mV.

$$SHy = (Ymax - Ymin)/Y_A \times 100\ (\%)$$

6) Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 200mV. Test the Max. (Cr max. and Cb max.) and Min. (Cr min. and Cb min.) values of C signals from R-Y and B-Y channels.

$$\Delta Sr = | (Crmax - Crmin)/Y_A | \times 100\ (\%)$$
$$\Delta Sb = | (Cbmax - Cbmin)/Y_A | \times 100\ (\%)$$

7) Test the average Y signal voltage when the device ambient temperature is at 55°C and light is obstructed with horizontal idle transfer level as reference.

8) Following 7, test Max. (Ydmax.) and Min. (Ydmin.) values of Y signal output. Only keep spot defects out of this range.

$$\Delta Ydt = Ydmax - Ydmin$$

9) ① Fy
Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 200 mV. Test the Y signal difference (ΔYf) between even field and odd field.

$$Fy = (\Delta Yf/Y_A) \times 100\ (\%)$$

② Fcr, Fcb
Set to standard imaging condition II. Insert R and B filter respectively, and test the C signal difference (ΔCr, ΔCb) between even field and odd field and the C signal output average value (C_{Ar}, C_{Ab}). At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

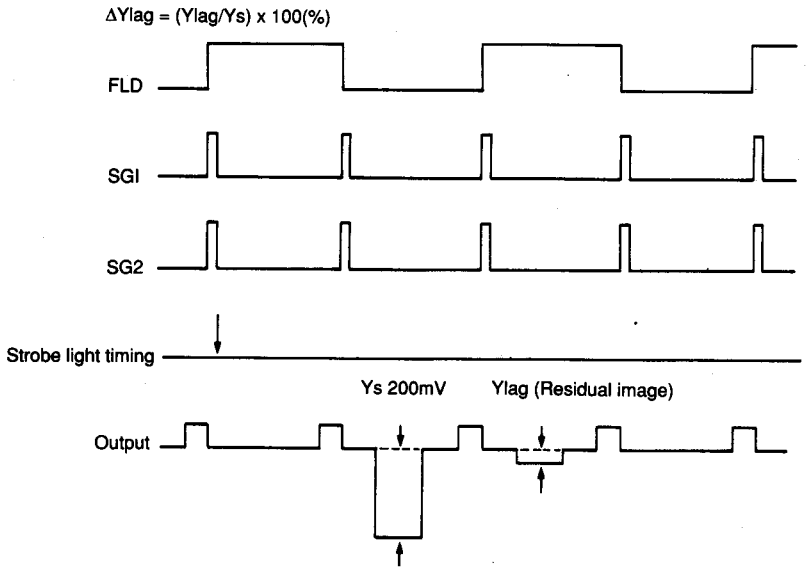
$$Fci = (\Delta Ci/C_{Ai}) \times 100\ (\%) \quad (i = r, b)$$

10) Set to standard imaging condition II. Insert W, R, G and B filters respectively, and test the C signal difference (ΔYlw, ΔYlr, ΔYlg, ΔYlb) between Y signal lines of the same field. At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

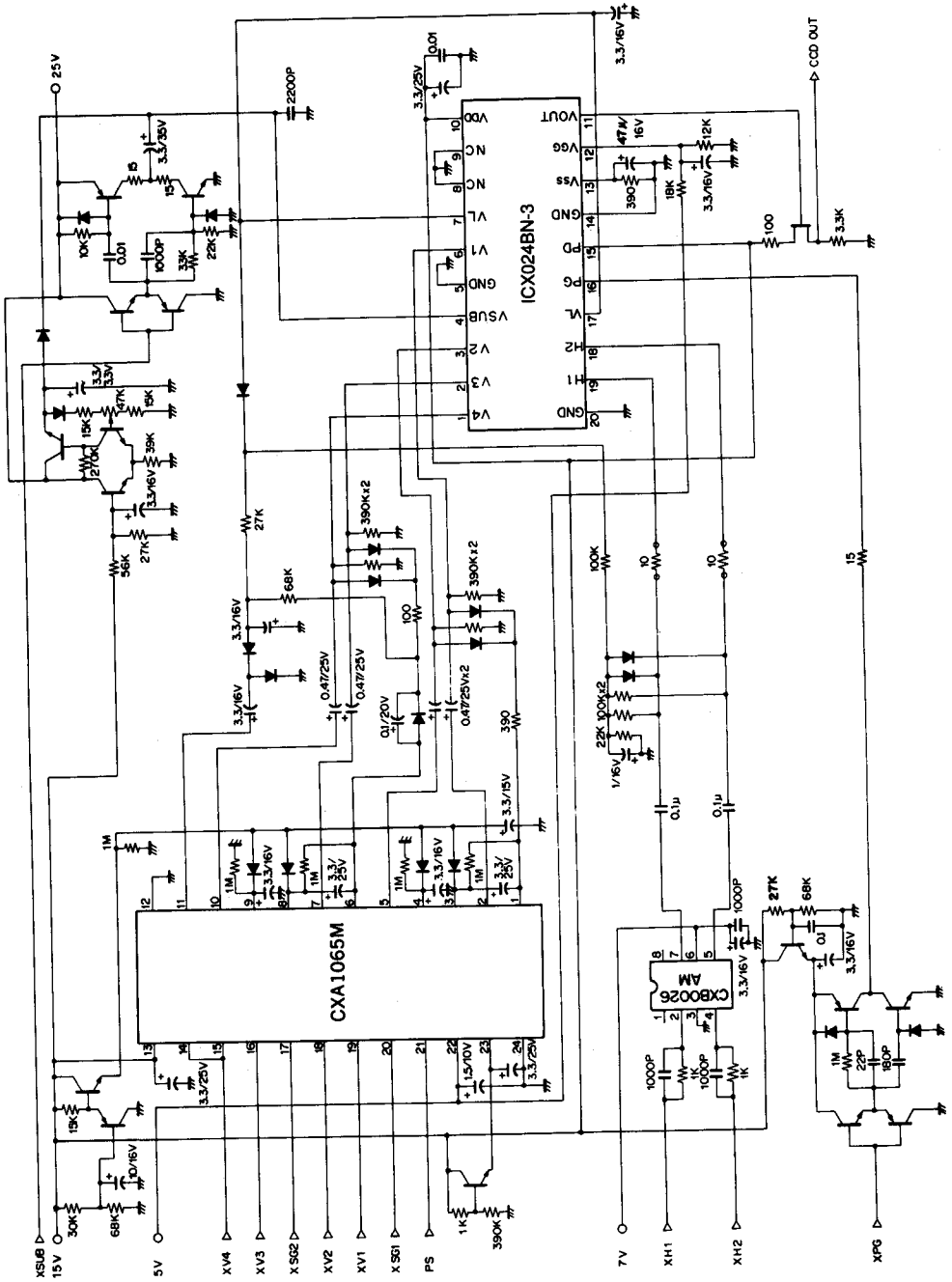
$$Lci = (\Delta Yli/Y_A) \times 100\ (\%) \quad (i = w, r, g, b)$$

11) Light a stroboscopic tube with the following timing and test the residual image.

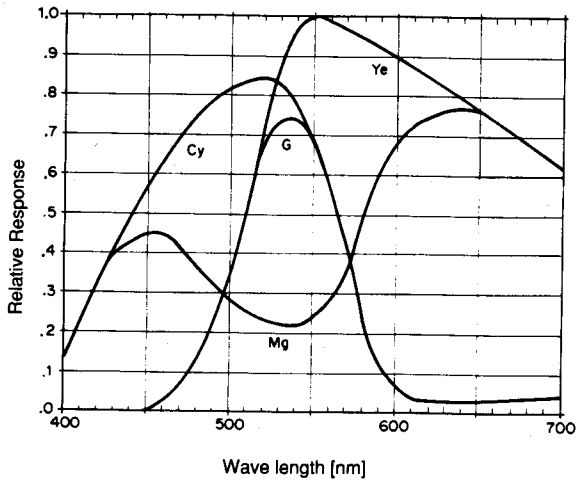
$$\Delta Ylag = (Ylag/Ys) \times 100\ (\%)$$



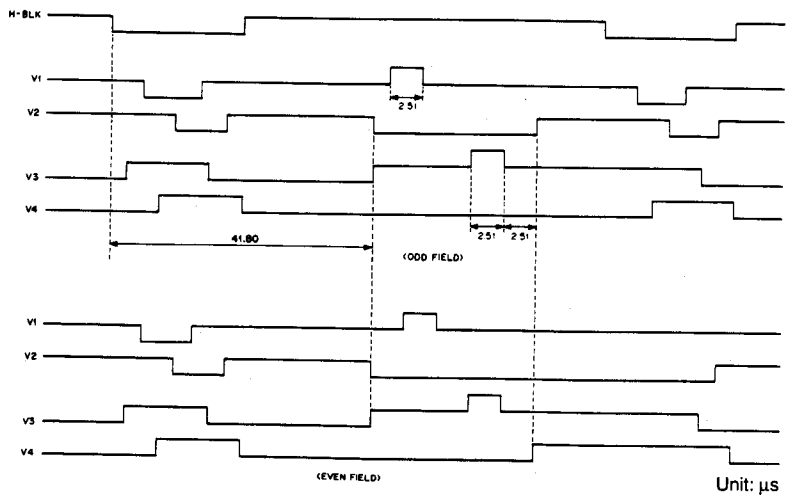
Drive Circuit



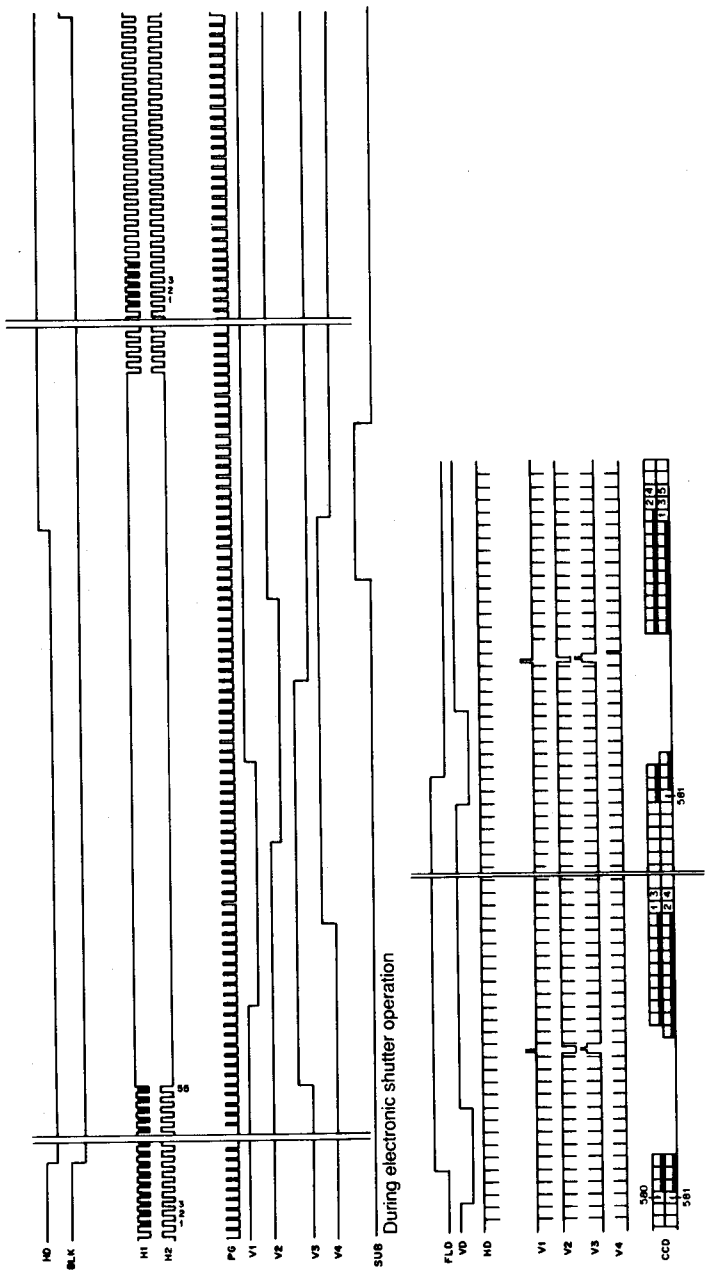
Spectral Sensitivity Characteristics (Excluding light source characteristics)
Fujinon lens H6 × 12.5R



Using read out clock timing chart



Drive Pulse Timing Chart (PAL)



Handling Instructions

1) Static charge prevention
CCD image sensor are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount cool sufficiently.
c) To dismount an imaging device do not use a solder pult. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

7) Defect compensation ROM
This is shipped in its own case in pair with the CCD image sensor. Pair with the CCD image sensor bearing the same serial number during mounting. When the CCD image sensor has no defect there is no ROM or serial number.

SONY®

ICX026BKA

1/2 inch CCD Image Sensor for NTSC Color Camera

Description

ICX026BKA is an interline transfer CCD solid-state imager suitable for NTSC 1/2 inch color video cameras. High sensitiveness is achieved through the adoption of Ye, Cy, Mg and G complementary color mosaic filters and HAD (Hole Accumulated Diode) sensors.

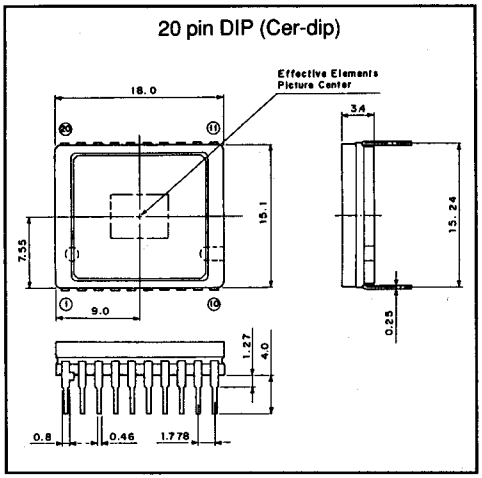
This chip features a field integration read out system, an electronic shutter with variable charge-storage time and 20pin Cer-DIP package.

Features

- High sensitivity (+6 dB compare with ICX026AK)
- Optical size 1/2 inch format
- Field integration read out system
- Low dark current. High sensitivity HAD sensor
- Ye, Cy, Mg, G on chip type complementary color mosaic filter.
- Horizontal register 5V drive
- High antiblooming
- Low smear
- Variable speed electronic shutter

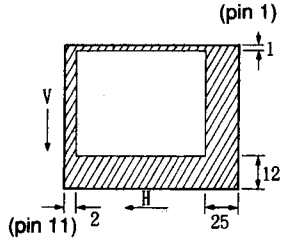
Package Outline

Unit: mm



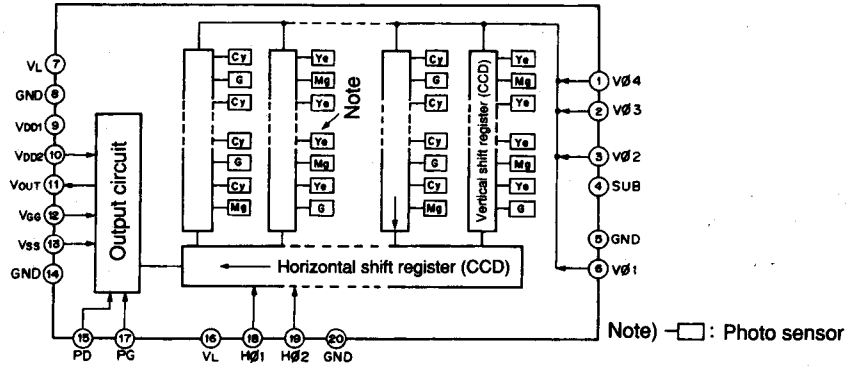
Device Structure

- Number of effective pixels 510 (H) × 492 (V)
- Number of total pixels 537 (H) × 505 (V)
- Interline transfer CCD image sensor
- Chip size 7.84 mm (H) × 6.40 mm (V)
- Unit cell size 12.7 µm (H) × 9.8 µm (V)
- Optical black
  - Horizontal (H) direction Front 2 pixels Rear 25 pixels
  - Vertical (V) direction Front 12 pixels Rear 1 pixels
- Number of dummy bits
  - Horizontal 16
  - Vertical 1 (even field only)
- Substrate material silicon



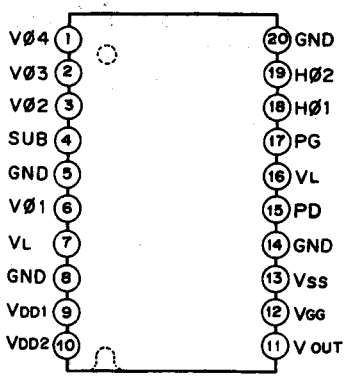
Optical black position (Top View)

Block Diagram



E91635-YA

Pin Configuration (Top View)



Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	11	VOUT	Signal output
2	Vφ3	Vertical register transfer clock	12	VGG	Output amplifier gate bias
3	Vφ2	Vertical register transfer clock	13	VSS	Output amplifier source
4	SUB	Substrate (Overflow drain)	14	GND	GND
5	GND	GND	15	PD	Precharge drain bias
6	Vφ1	Vertical register transfer clock	16	VL	Protective transistor bias
7	VL	Protective transistor bias	17	PG	Precharge gate clock
8	GND	GND	18	Hφ1	Horizontal register transfer clock
9	VDD1	Output amplifier drain supply	19	Hφ2	Horizontal register transfer clock
10	VDD2	Output amplifier drain supply	20	GND	GND

Absolute Maximum Ratings

• Substrate voltage	SUB – GND	–0.3 to +55 V
• Supply voltage	VDD1, VDD2, PD, VOUT, VSS, – GND	–0.3 to +18 V
	VDD1, VDD2, PD, VOUT, VSS, – SUB	–55 to +10 V
• Clock input voltage	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – GND	–15 to +20 V
	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – SUB	–65 to +10 V
• Voltage difference between vertical clock input pins		+15 V *
• Voltage difference between horizontal clock input pins		+17 V
• Hφ1, Hφ2, – Vφ4,		–17 to +17 V
• PG, VGG – GND		–10 to +15 V
• PG, VGG – SUB		–55 to +10 V
• VL – SUB		–65 to +0.3 V
• Beside GND, SUB, VL – VL		–0.3 to +30 V
• Storage temperature		–30 to +80 °C
• Operating temperature		–10 to +55 °C

***Note)** +27 V (Max.) when clock width < 10 µs, duty factor < 0.1%.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD1}, V_{DD2}	14.55	15.0	15.45	V	V_{DD1} = V_{DD2}
Precharge drain voltage	V_{PD}	14.55	15.0	15.45	V	V_{PD} = V_{DD1} = V_{DD2}
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	V_{SS}	Ground through 680 Ω resistor				±5%
Substrate voltage adjustment range	V_{SUB}	7		19	V	*1
Fluctuation range after substrate voltage adjustment	V_{SUB}	-3		+3	%	
Protective transistor bias	V_L	*2				

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		2.5		mA	I_{DD} = I_{DD1} + I_{DD2}
Input current	I_{IN1}			1	μA	*3
Input current	I_{IN2}			10	μA	*4

Note) *1. Substrate voltage (V_{SUB}) setting value display.
Substrate voltage setting value is displayed at the back of the device through a code address. Adjust so as to obtain the displayed voltage at SUB pin.

V_{SUB} code address – two digits display

□ □
↑ ↑
Integral part Decimal part

The relation between code address of integral part and actual numerical values.

Code address of integral part	7	8	9	A	B	C	D	E	F	G	H	I	J
Numerical value	7	8	9	10	11	12	13	14	15	16	17	18	19

<Example> F5 → 15.5 (V)

*2. V_L setting is V_{VL} of the vertical transfer clock waveform.

*3. 1) Current to earth when 18V is applied to pins V_{DD1}, V_{DD2}, V_{OUT}, Vss and SUB pin. However, pins that are not tested are grounded.
2) Current to earth when 20V is sequentially applied to pins Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, and Hφ2. However, 20V is applied to SUB while pins that are not tested are grounded.
3) Current to earth when 15V is sequentially applied to pins PG and V_{GG}. However, 15V is applied to SUB while pins that are not tested are grounded.

*4. 1) Current to earth when 55V is applied to SUB pin. Pins that are not tested are grounded.
2) Current to earth when V_L is grounded, GND and SUB are open and 30V is applied to other pins.

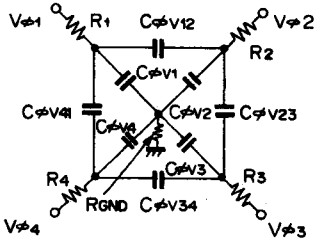
Clock Voltage Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	No.	Remarks
Read out clock voltage	V_{VT}	14.3	15.0	15.7	V	2,6	*1
Vertical transfer clock voltage *2	V_{VH1},V_{VH2},V_{VH3},V_{VH4}	−0.2	0	0.2	V	1,2,3,6	$V_{VH}=(V_{VH1}+V_{VH2})/2$
	V_{VL1},V_{VL2},V_{VL3},V_{VL4}	−9.6	−9.0	−8.3	V	1,2,3,6	$V_{VL}=(V_{VL3}+V_{VL4})/2$
	$V_{\phi V}$	8.1	9.0	9.8	V	1,2,3,6	$V_{\phi V}=V_{VHn}-V_{VLn}$ (n=1 to 4)
	$\lvert V_{VH1} - V_{VH2} \rvert$			0.2	V	3,6	
	$V_{VH3} - V_{VH}$	−0.4		0.1	V	2,3,6	
	$V_{VH4} - V_{VH}$	−0.4		0.1	V	1,3,6	
	V_{VHH}			0.8	V	1,2,3,6	High level coupling
	V_{VHL}			1.0	V	1,2,3,6	High level coupling
	V_{VLH}			0.8	V	1,2,3,6	Low level coupling
	V_{VLL}			0.8	V	1,2,3,6	Low level coupling
Horizontal transfer clock voltage	$V_{\phi H}$	4.7	5.0	5.3	V	18,19	*3
	V_{HL}	−0.05	0	0.05	V	18,19	
Precharge gate clock voltage	$V_{\phi PG}$	8.0		11.5	V	17	*4
	V_{PGL}	−0.1	0	0.1	V	17	
Substrate clock voltage	$V_{\phi SUB}$	23.0		34.0	V	4	*5

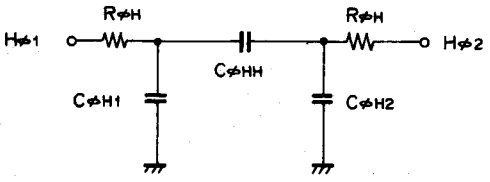
Note) *1. See Fig. 1.
*2. See Fig. 2.
*3. See Fig. 3.
*4. See Fig. 3.
*5. See Fig. 4.

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$, $C_{\phi V3}$		1000		pF	
Capacitance between vertical transfer clock and GND	$C_{\phi V2}$, $C_{\phi V4}$		1200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$, $C_{\phi V34}$		1200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V23}$, $C_{\phi V41}$		750		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, $C_{\phi H2}$		70		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Capacitance between precharge gate clock and GND	$C_{\phi PG}$		8		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		400		pF	
Vertical transfer clock serial resistor	R_1,R_2,R_3,R_4		33		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock serial resistor	$R_{\phi H}$		10		Ω	



Vertical transfer clock equivalent circuit



Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

1. Read out clock waveform

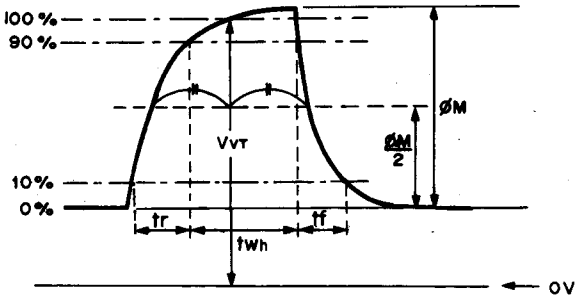


Fig.1

2. Vertical transfer clock waveform

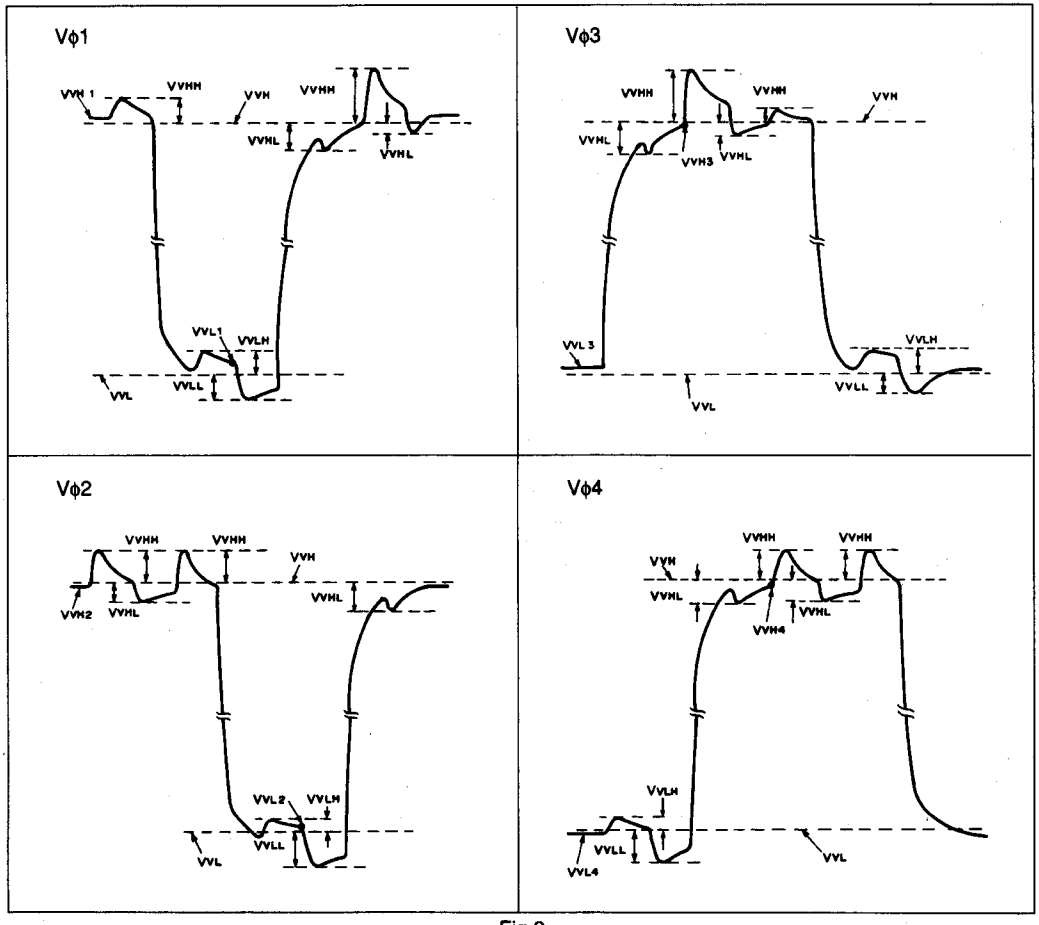


Fig.2

3. Horizontal transfer clock waveform/Precharge gate clock waveform

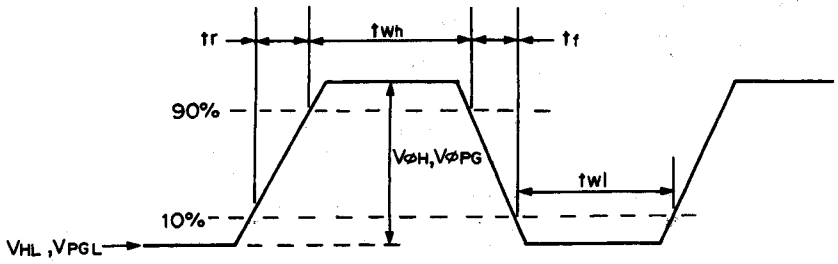


Fig. 3

4. Substrate clock waveform

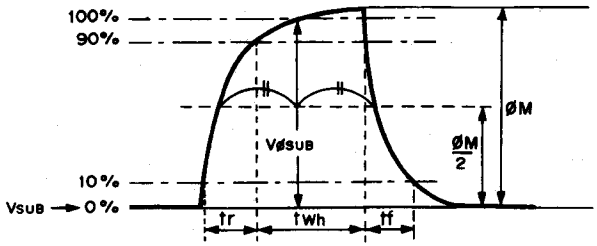


Fig. 4

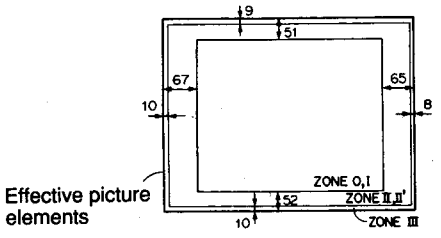
Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max	Min.	Typ.	Max	Min.	Typ.	Max.	Min.	Typ.	Max		
Read out clock	VT	1.5	1.85							0.5			0.5	µs	During read out
Vertical transfer clock	Vφ1,Vφ2,Vφ3,Vφ4									0.45	0.015		0.25	µs	*
Horizontal transfer clock	Hφ	37	41		38	42			12	15		10	15	ns	During imaging
Horizontal transfer clock	Hφ1		5.6						0.012			0.01		µs	During parallel serial conversion.
Horizontal transfer clock	Hφ2					5.6			0.012			0.01		µs	During parallel serial conversion.
Precharge gate clock	φPG	15	17		75	81			4			3		ns	
Substrate clock	φSUB	1.5	2.1							0.5			0.5	µs	During charge drain.

***Note)** When vertical transfer clock driver CXD1250 is in use.

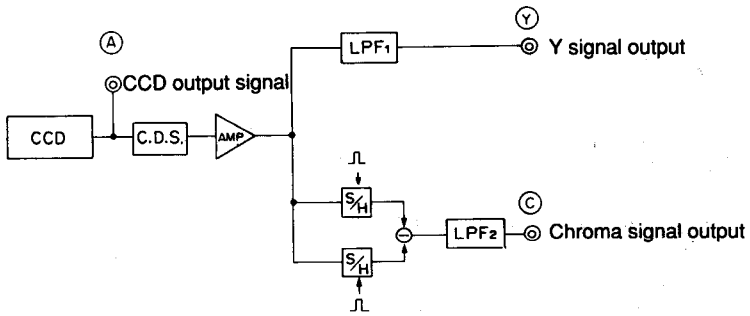
Operating Characteristics Ta = 25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	260	340		mV	1	Ta=55°C
Saturation signal	Ysat	500			mV	2	
Smear	SM		0.005	0.015	%	3	
Blooming margin		1000			times	4	
Video signal shading	SHy			20	%	5	Zone0, I
				25	%	5	Zone0 to II'
Uniformity between signal channels	ΔSr			10	%	6	
	ΔSb			10	%	6	
Dark signal	Ydt			2	mV	7	Ta=55°C
Dark signal shading	ΔYdt			1	mV	8	Ta=55°C
Flicker Y	Fy			2	%	9	
Flicker R-Y	Fcr			5	%	9	
Flicker B-Y	Fcb			5	%	9	
Horizontal stripes R	Lcr			4	%	10	
Horizontal stripes G	Lcg			4	%	10	
Horizontal stripes B	Lcb			4	%	10	
Horizontal stripes W	Lcw			4	%	10	
Lag	ΔYlag			0.5	%	11	

Zone chart of Video signal shading



Testing System



Note) Adjust AMP amplifier so that total gains between Ⓐ and Ⓨ and between Ⓐ and Ⓒ equal 1.

Test Method

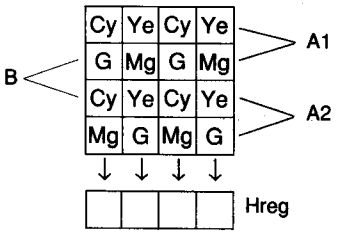
Test conditions

1) Through the following tests the substrate voltage should set to the value displayed on the device, while the device drive conditions should be kept within the range of the bias and clock voltage conditions.

2) Through the following tests defects are excluded and, unless otherwise specified the optical black level (Hence forth referred to as OPB) is set as the reference for the signal output which is taken as the Y signal output or the Chroma signal output of the testing system.

Color coding of CFA (Color Filter Array) & Composition of luminance (Y) and chrominance (C) signals.

CFA of this imager is shown in the Figure. This complementary CFA is used with a "field integration mode", where all of the photosites are read out during each video field. Signals from two vertically adjacent photosites, such as line A1 or A2 for field A, are summed when the image charge is transferred into the vertical storage columns. The readout line pairing is shifted down one line for field B. The sensor output signals through the horizontal register (H reg.) at line A1 are



Color Coating Diagram

[G+Cy], [Mg+Ye], [G+Cy], [Mg+Ye].

These signals are processed in order to compose Y and C signals. By adding the two adjacent signals at line A1, Y signal is formed as follows:

$$Y = \{(G+Cy) + (Mg+Ye)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

C signal is composed by subtracting the two adjacent signals at line A1.

$$R - Y = \{(Mg+Ye) - (G+Cy)\}$$
$$= \{2R-G\}$$

Next, the signals through H reg. at line A2 are

[Mg+Cy], [G+Ye], [Mg+Cy], [G+Ye]

Similarly, Y and C signals are composed at line A2.

$$Y = \{(G+Ye) + (Mg+Cy)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

$$-(B-Y) = \{(G+Ye) - (Mg+Cy)\}$$
$$= -\{2B-G\}$$

Accordingly, Y signal is balanced in relation to the scanning lines, and C signal takes the form of R–Y and –(B–Y) on alternate lines.
It is the same for B field.

Definition of standard imaging conditions

①Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 cd/m² 3200K Halogen source), at F5.6 with a typical test lens, and CM-500S (t=1.0 mm) for IR cut filter.

②Standard imaging condition II: Use a light source with uniformity within 2%, color temperature of 3200K and CM-500S (t=1.0 mm) as IR cut filter. The light intensity is adjusted in accordance with the average value of Y signals (Y_A) indicated in each item.

1) Set to standard imaging condition I and measure Y signal (S) at the center of the screen.

2) Set to imaging condition II. Adjust light intensity to 10 times when Y signal output average value Y_A=150mV. Then test Y signal Min. Value.

3) Set to imaging condition II. Adjust light intensity to 500 times when Y signal output average value Y_A=150mV. Stop Read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the Max. value Y_{SM} of Ysignal output.

$$SM = (Y_{SM}/Y_A) \times {}^1/_{500} \times {}^1/_{10} \times 100\ (\%) \quad ({}^1/_{10}V)$$

4) Set to imaging condition II. Adjust light intensity to 1000 times when Y signal output average value Y_A=150mV. Then check that there is no blooming.

5) Video signal shading SHy
Set to standard imaging condition II. Test Y signal Max. (Y max.) and Min. (Y min.) values. Adjust light intensity to obtain a Y signal output average value (Y_A) of about 150mV.

$$SHy = (Ymax - Ymin)/Y_A \times 100\ (\%)$$

6) Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 150mV. Test the Max. (Cr max. and Cb max.) and Min. (Cr min. and Cb min.) values of C signals from R-Y and B-Y channels.

$$\Delta Sr = | (Crmax - Crmin)/Y_A | \times 100\ (\%)$$
$$\Delta Sb = | (Cbmax - Cbmin)/Y_A | \times 100\ (\%)$$

7) Test the average Y signal voltage when the device ambient temperature is at 55°C and light is obstructed with horizontal idle transfer level as reference.

8) Following 7, test Max. (Yd max.) and Min. (Yd min.) values of Y signal output. Only keep spot defects out of this range.

$$\Delta Ydt = Ydmax - Ydmin$$

9) ① Fy
Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 150 mV. Test the Y signal difference (ΔYf) between even field and odd field.

$$Fy = (\Delta Yf/Y_A) \times 100\ (\%)$$

② Fcr, Fcb
Set to standard imaging condition II. Insert R and B filter respectively, and test the C signal difference (ΔCr, ΔCb) between even field and odd field and the C signal output average value (C_{Ar}, C_{Ab}). At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

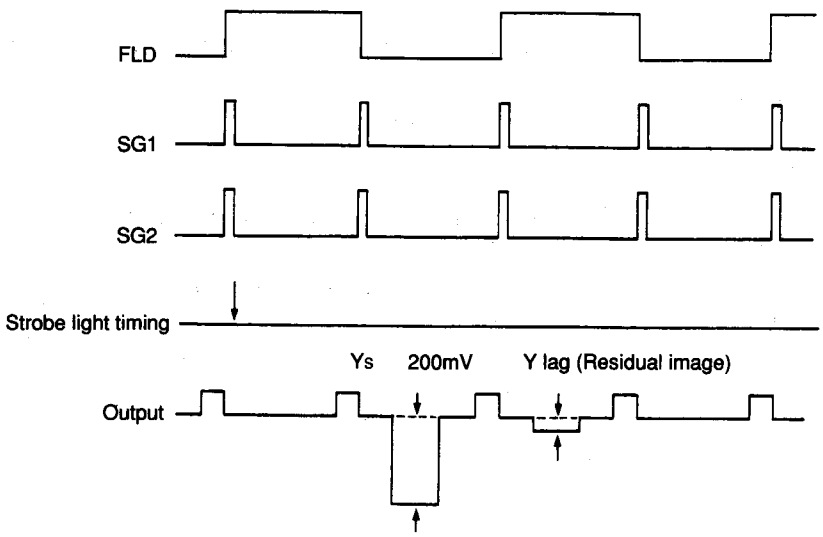
$$Fci = (\Delta Ci/C_{Ai}) \times 100\ (\%) \quad (i = r, b)$$

10) Set to standard imaging condition II. Insert W, R, G and B filters respectively, and test the signal difference (ΔYlw, ΔYlr, ΔYlg, ΔYlb) between Y signal lines of the same field. At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

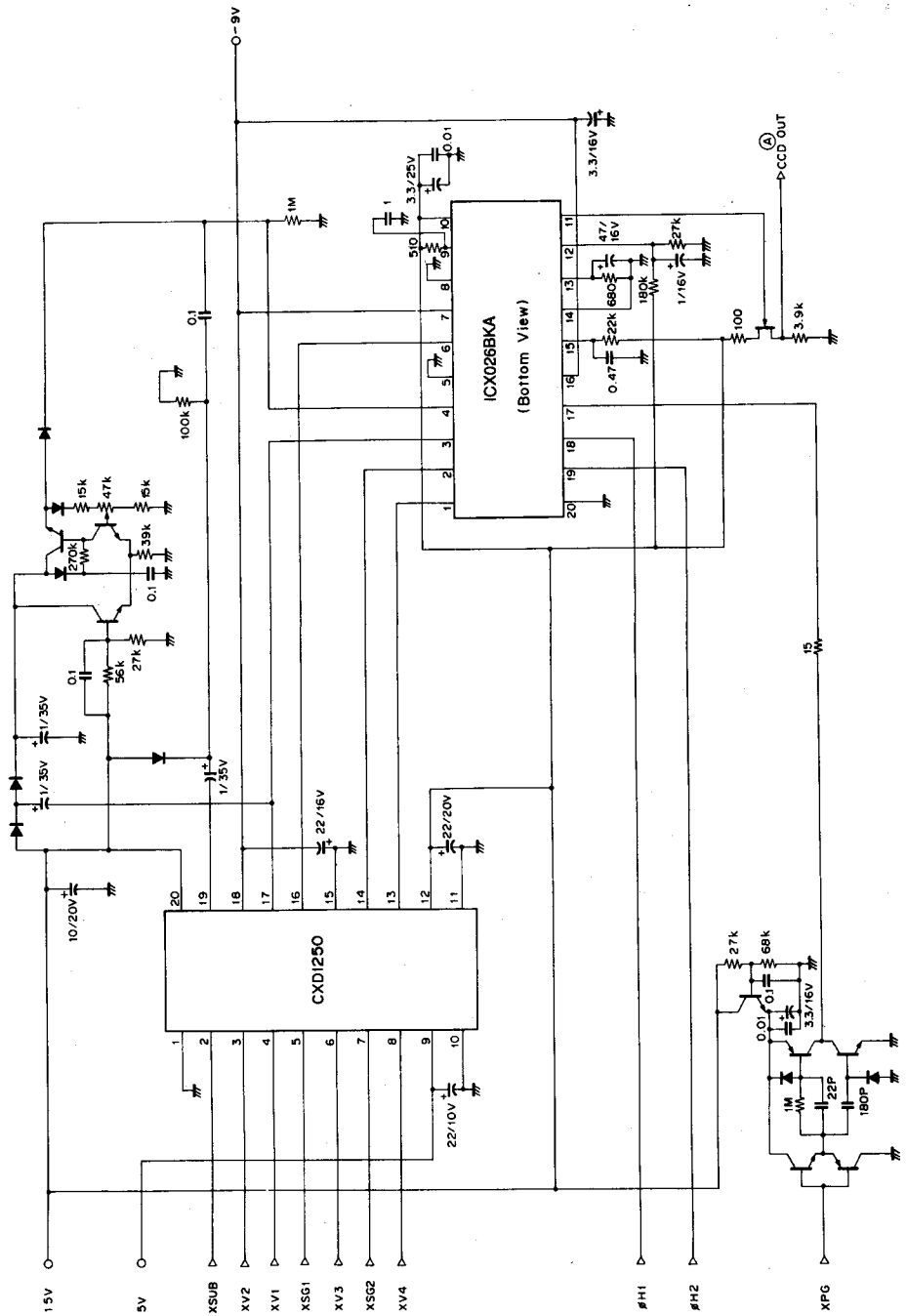
$$Lci = (\Delta Yli/Y_A) \times 100\ (\%) \quad (i = w, r, g, b)$$

11) Light a stroboscopic tube with the following timing and test the residual image.

$$\Delta Ylag = (Ylag/Ys) \times 100\ (\%)$$

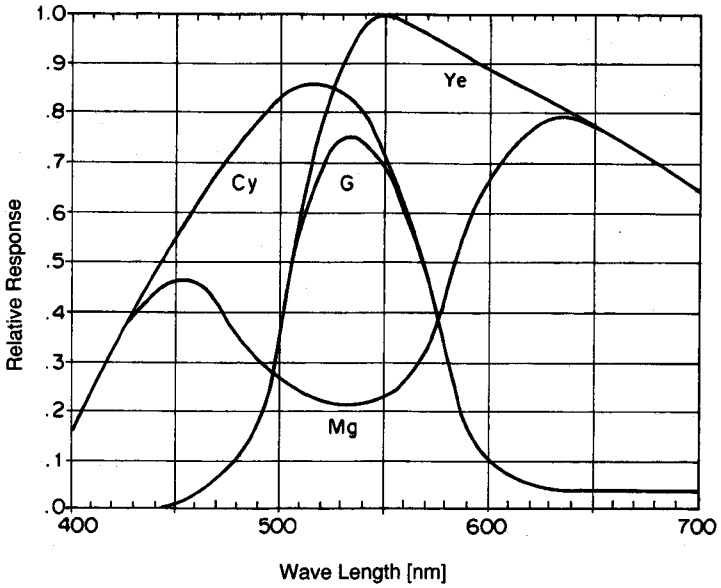


Drive Circuit

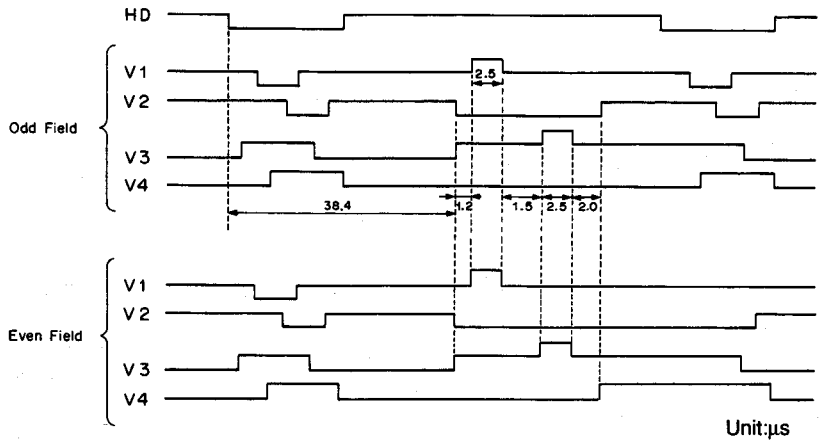


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

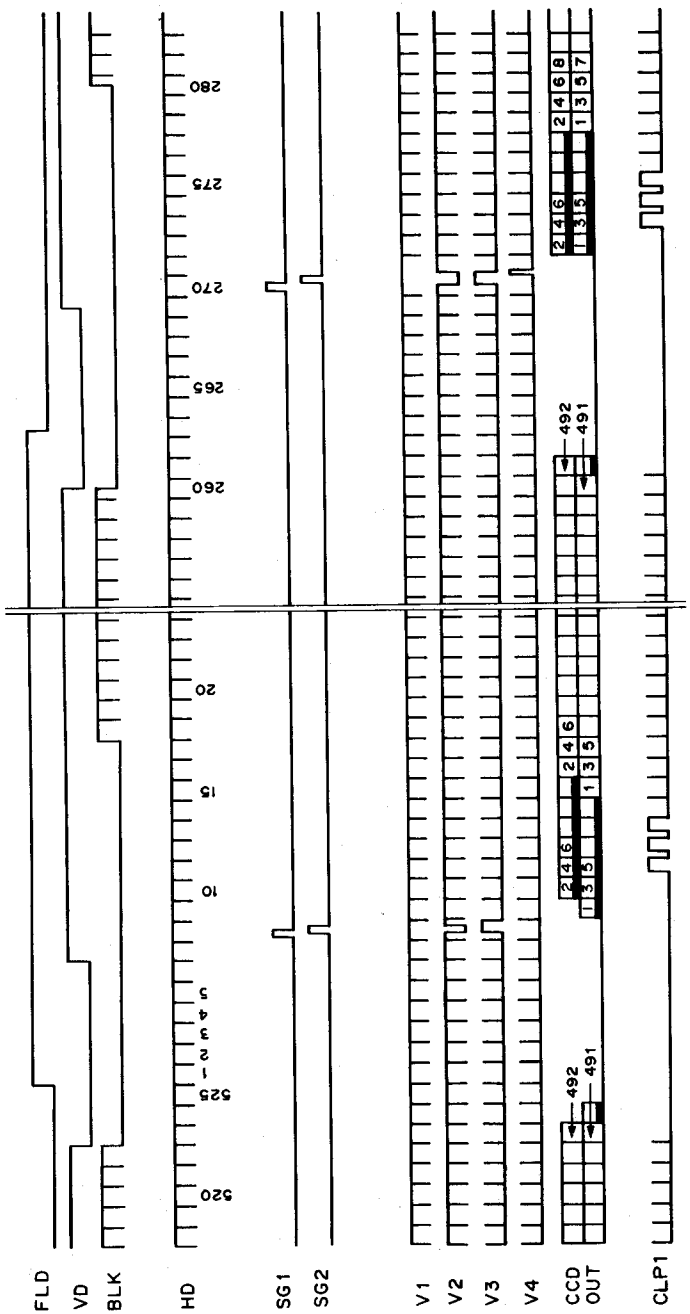
Spectral Sensitivity Characteristics
(Excluding light source characteristics, including lens characteristics)



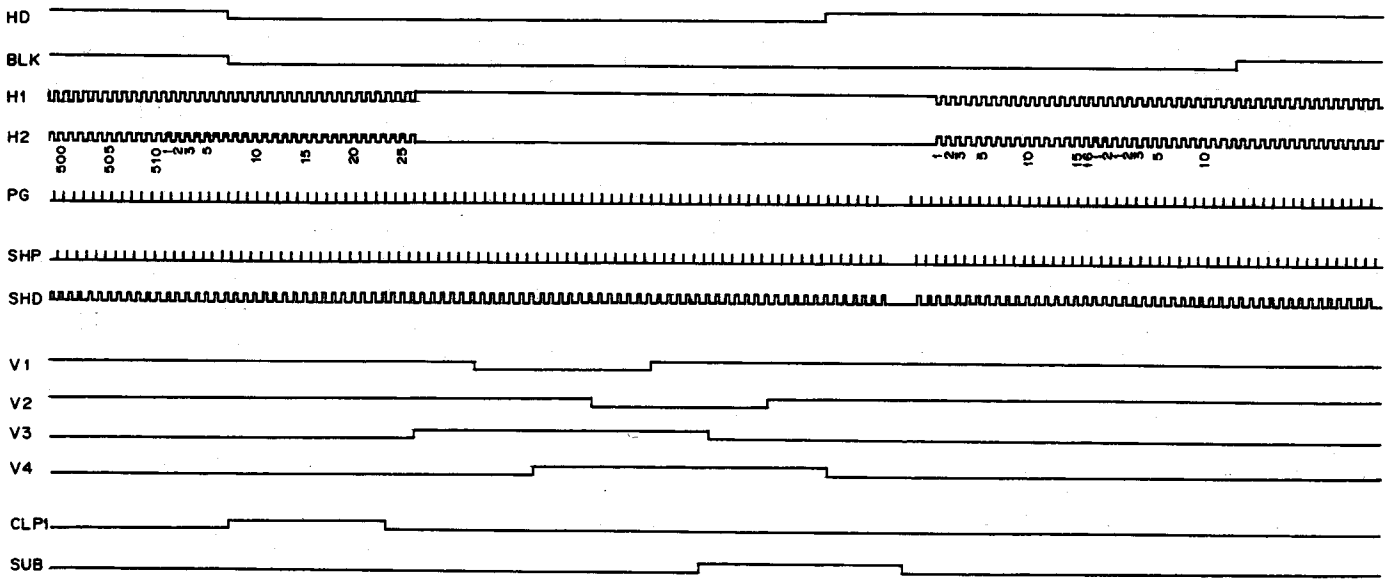
Using read out clock timing chart



Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



During electronic shutter operation

Handling Instructions

1) Static charge prevention
CCD image sensor are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount cool sufficiently.
c) To dismount an imaging device do not use a solder pult. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

SONY

ICX026CKA

1/2 inch CCD Image Sensor for NTSC Color Camera

Description

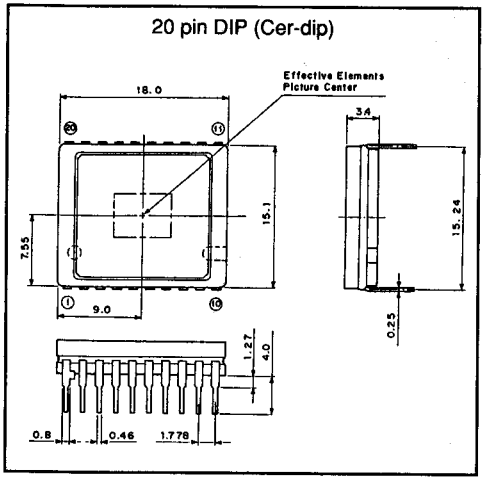
ICX026CKA is an interline transfer CCD solid-state image sensor suitable for NTSC 1/2 inch color video cameras. High sensitivity is achieved through the adoption of Ye, Cy, Mg and G complementary color mosaic filters and HAD (Hole-Accumulation Diode) sensors.

Beside correspondence with timing generator CXD1253, 5V drive of the reset gate is also possible.

This chip features a field integration read out system, an electronic shutter with variable charge-storage time and 20pin Cer-DIP package.

Package Outline

Unit: mm

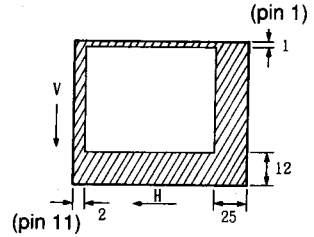


Features

- High sensitivity (+6 dB compare with ICX026AK)
- Optical size 1/2 inch format
- Field integration read out system
- Low dark current. High sensitivity HAD sensor
- Ye, Cy, Mg, G on chip type complementary color mosaic filter.
- Horizontal register 5V drive
- Reset gate 5V drive
- High antiblooming
- Low smear
- Variable speed electronic shutter

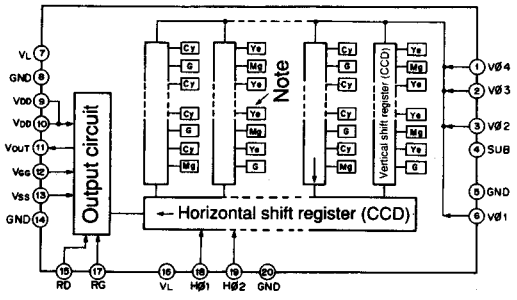
Device Structure

- Number of effective pixels 510 (H) × 492 (V)
- Number of total pixels 537 (H) × 505 (V)
- Interline transfer CCD image sensor
- Chip size 7.84 mm (H) × 6.40 mm (V)
- Unit cell size 12.7 µm (H) × 9.8 µm (V)
- Optical black
  - Horizontal (H) direction Front 2 pixels Rear 25 pixels
  - Vertical (V) direction Front 12 pixels Rear 1 pixel
- Number of dummy bits
  - Horizontal 16
  - Vertical 1 (even field only)
- Substrate material silicon



Optical black position (Top View)

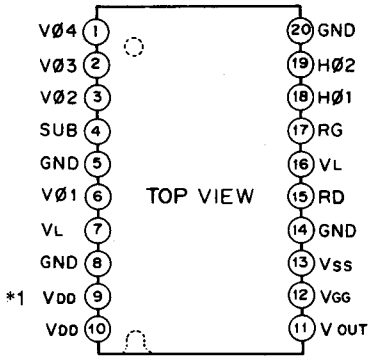
Block Diagram



Note) –□ : Photo sensor

E91637-YA

Pin Configuration (Top View)



*1 As Pins 9 and 10 are internally shorted, either one can be connected to the power supply while the other is kept open. Should both be connected to the power supply, make sure the same voltage is applied.

Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	11	VOUT	Signal output
2	Vφ3	Vertical register transfer clock	12	VGG	Output amplifier gate bias
3	Vφ2	Vertical register transfer clock	13	VSS	Output amplifier source
4	SUB	Substrate (Overflow drain)	14	GND	GND
5	GND	GND	15	RD	Reset drain bias
6	Vφ1	Vertical register transfer clock	16	VL	Protective transistor bias
7	VL	Protective transistor bias	17	RG	Reset gate clock
8	GND	GND	18	Hφ1	Horizontal register transfer clock
9	VDD	Output amplifier drain supply	19	Hφ2	Horizontal register transfer clock
10	VDD	Output amplifier drain supply	20	GND	GND

Absolute Maximum Ratings

• Substrate voltage	SUB – GND	–0.3 to +55	V
• Supply voltage	VDD, RD, VOUT, VSS, – GND	–0.3 to +18	V
	VDD, RD, VOUT, VSS, – SUB	–55 to +10	V
• Clock input voltage	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – GND	–15 to +20	V
	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – SUB	–65 to +10	V
• Voltage difference between vertical clock input pins		+15	V *2
• Voltage difference between horizontal clock input pins		+17	V
• Hφ1, Hφ2, – Vφ4		–17 to +17	V
• RG, VGG – GND		–10 to +15	V
• RG, VGG – SUB		–55 to +10	V
• VL – SUB		–65 to +0.3	V
• Beside GND, SUB, VL – VL		–0.3 to +30	V
• Storage temperature		–30 to +80	°C
• Operating temperature		–10 to +60	°C

*2 +27 V (Max.) when clock width < 10 µs, duty factor < 0.1%.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD}	14.55	15.0	15.45	V	
Reset drain voltage	V_{RD}	14.55	15.0	15.45	V	$V_{RD} = V_{DD}$
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	V_{SS}	Ground through 680 Ω resistor				±5%
Substrate voltage adjustment range	V_{SUB}	7.0		18.5	V	*1
Fluctuation range after substrate voltage adjustment	ΔV_{SUB}	−3		+3	%	
Reset gate clock voltage adjustment range	V_{RGL}	0.5		3.5	V	*1
Fluctuation range after reset gate clock voltage adjustment	ΔV_{RGL}	−3		+3	%	
Protective transistor bias	V_L	*2				

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		2.5		mA	
Input current	I_{IN1}			1	μA	*3
Input current	I_{IN2}			10	μA	*4

Note) *1. Substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) setting values are displayed at the back of the device through a code address. Adjust so as to obtain the displayed voltages at SUB and RG pins respectively.

V_{SUB} code address - 1 digit display
V_{RGL} code address - 1 digit display

□ ↑ V_{RGL} code address

□ ↑ V_{SUB} code address

The relation between code address and actual numerical values.

V_{RGL} code address	0	1	2	3	4	5	6
Numerical value	0.5	1.0	1.5	2.0	2.5	3.0	3.5

V_{SUB} code address	A	b	C	D	E	f	G	h	J	K	L	m
Numerical value	7.0	7.5	8.0	8.5	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5
V_{SUB} code address	N	P	Q	R	S	T	U	V	W	X	Y	Z
Numerical value	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5

<Example> "5L" → V_{RGL} = 3.0 V, V_{SUB} = 12.0 V

*2. V_L setting is V_{VL} of the vertical transfer clock waveform.

*3. 1) Current to earth when 18V is applied to pins V_{DD}, V_{OUT}, Vss and SUB pin. However, pins that are not tested are grounded.
2) Current to earth when 20V is sequentially applied to pins Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, and Hφ2. However, 20V is applied to SUB while pins that are not tested are grounded.
3) Current to earth when 15V is sequentially applied to pins RG and V_{GG}. However, 15V is applied to SUB while pins that are not tested are grounded.

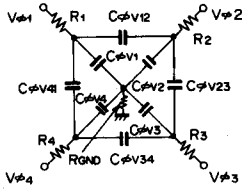
*4. 1) Current to earth when 55V is applied to SUB pin. Pins that are not tested are grounded.
2) Current to earth when V_L is grounded, GND and SUB are open and 30V is applied to other pins.

Clock Voltage Conditions

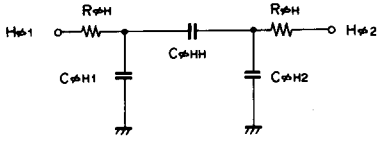
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform	Remarks
Read out clock voltage	V_{VT}	14.3	15.0	15.7	V	1	
Vertical transfer clock voltage	V_{VH1},V_{VH2},V_{VH3},V_{VH4}	–0.2	0	0.2	V	2	$V_{VH}=(V_{VH1}+V_{VH2})/2$
	V_{VL1},V_{VL2},V_{VL3},V_{VL4}	–9.6	–9.0	–8.3	V	2	$V_{VL}=(V_{VL3}+V_{VL4})/2$
	$V_{\phi V}$	8.1	9.0	9.8	V	2	$V_{\phi V}=V_{VHn}-V_{VLn}$ (n=1 to 4)
	$\lvert V_{VH1} - V_{VH2} \rvert$			0.2	V	2	
	$V_{VH3} - V_{VH}$	–0.4		0.1	V	2	
	$V_{VH4} - V_{VH}$	–0.4		0.1	V	2	
	V_{VHH}			0.8	V	2	High level coupling
	V_{VHL}			1.0	V	2	High level coupling
	V_{VLH}			0.8	V	2	Low level coupling
	V_{VLL}			0.8	V	2	Low level coupling
Horizontal transfer clock voltage	$V_{\phi H}$	4.7	5.0	5.3	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
Reset gate clock voltage	$V_{\phi RG}$	4.5	5.0	5.5	V	4	When V_{RGL} is adjusted to the displayed value
	$V_{RGLH} - V_{RGLL}$			0.8	V	4	
	$V_{\phi RG}$	8.0		11.5	V	4	When V_{RGL} is fixed
	V_{RGL}	–0.1	0	0.1	V	4	
	$V_{RGLH} - V_{RGLL}$			0.8	V	4	
Substrate clock voltage	$V_{\phi SUB}$	23.0		34.0	V	5	

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$, $C_{\phi V3}$		1000		pF	
Capacitance between vertical transfer clock and GND	$C_{\phi V2}$, $C_{\phi V4}$		1200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$, $C_{\phi V34}$		1200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V23}$, $C_{\phi V41}$		750		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, $C_{\phi H2}$		70		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		8		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		400		pF	
Vertical transfer clock serial resistor	R_1,R_2,R_3,R_4		33		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock serial resistor	$R_{\phi H}$		10		Ω	



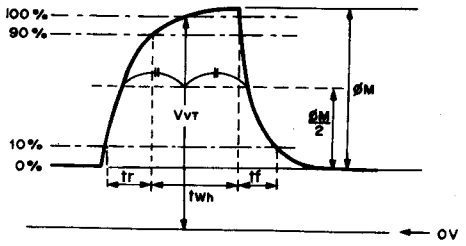
Vertical transfer clock equivalent circuit



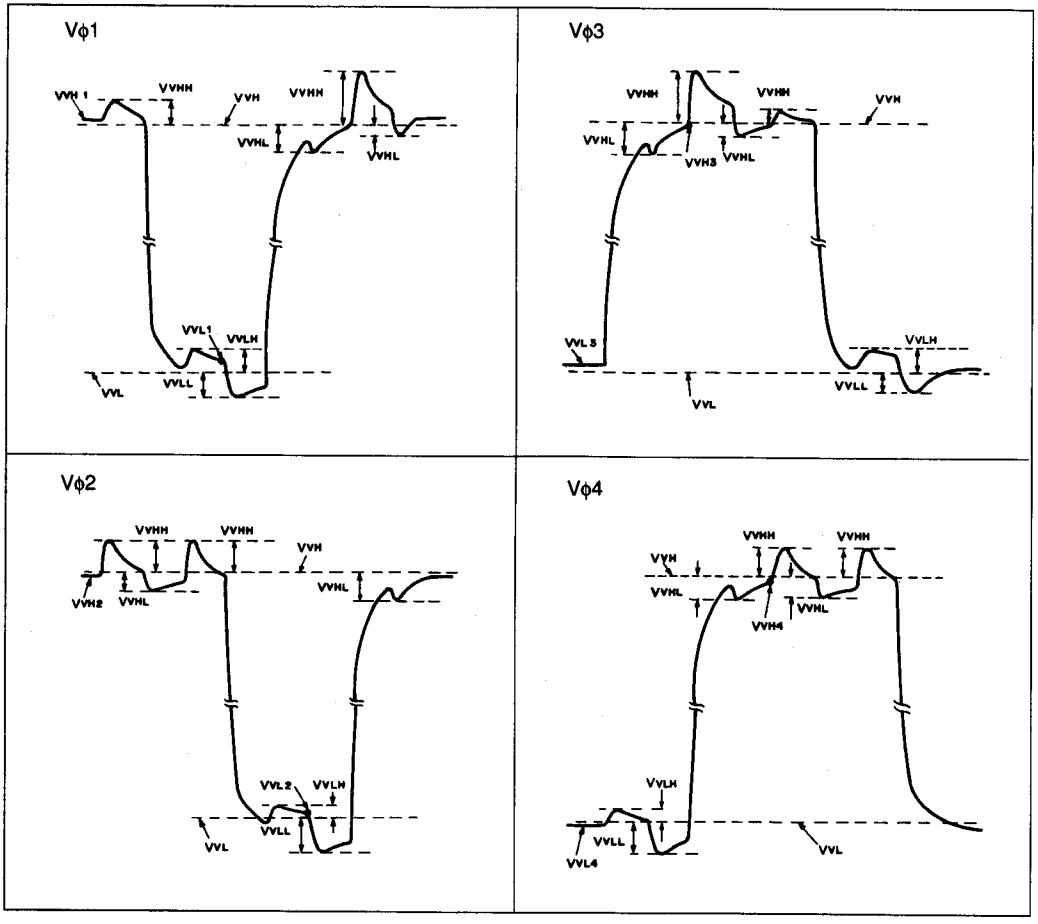
Horizontal trasfer clock equivalent circuit

Drive Clock Waveform Conditions

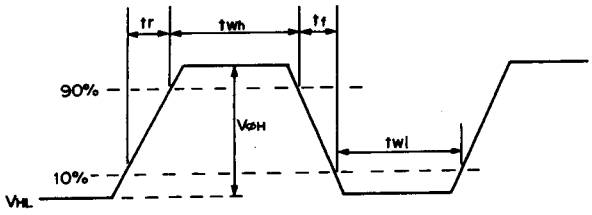
1. Read out clock waveform



2. Vertical transfer clock waveform



3. Horizontal transfer clock waveform



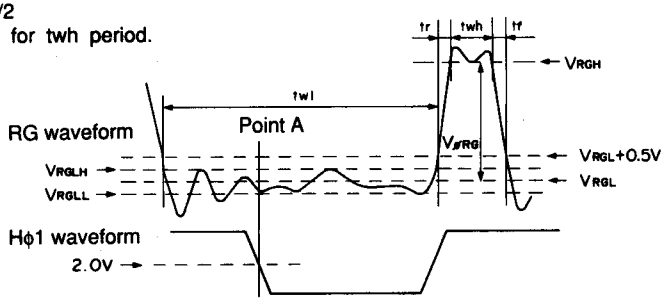
4. Reset gate clock waveform

VRGLH is the maximum value and VRGLL the minimum value of the coupling waveform of the period from Point A, in the diagram above, up to RG rise. VRGL is the mean value for VRGLH and VRGLL.

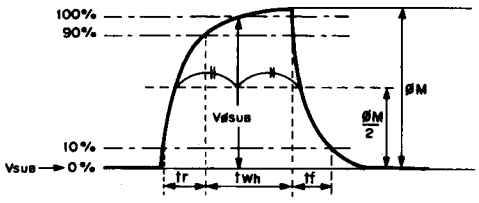
VRGL = (VRGLH + VRGLL)/2

VRGH is the minimum value for twh period.

VφRG = VRGH − VRGL



5. Substrate clock waveform



Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	VT	1.5	1.85							0.5			0.5	μs	During read out
Vertical transfer clock	Vφ1,Vφ2,Vφ3,Vφ4									0.45	0.015		0.25	μs	*1
Horizontal transfer clock	Hφ	34	39		38	40			14	17	8	12	15	ns	During imaging *2
Horizontal transfer clock	Hφ1		5.6						0.014			0.012		μs	During parallel serial conversion.
Horizontal transfer clock	Hφ2					5.6			0.014			0.012		μs	During parallel serial conversion.
Reset gate clock	φRG	14	15		75	79			6.5			4.5		ns	
Substrate clock	φSUB	1.5	2.1							0.5			0.5	μs	During charge drain.

*1) When vertical transfer clock driver CXD1250 is in use. tr and tf are defined as the rising and falling time of 10% to 90% the period between VVL and VVH.

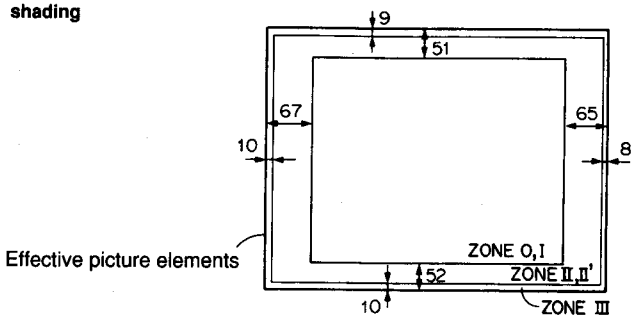
*2) Where, tr-tf is < 4ns, the waveform crosspoint voltage (Vcr) of Hφ1 and Hφ2, is taken as 2.3V<Vcr<2.7V.

Operating Characteristics

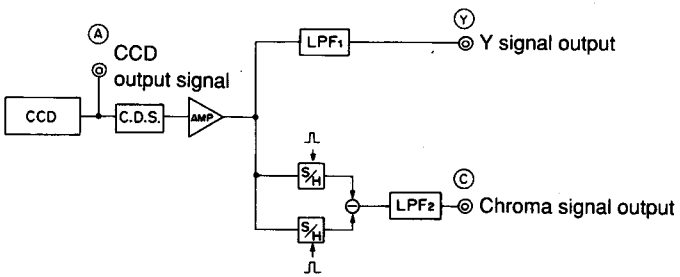
Ta = 25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	260	340		mV	1	
Saturation signal	Ysat	500			mV	2	Ta=60°C
Smear	SM		0.005	0.015	%	3	
Blooming margin		1000			times	4	
Video signal shading	SHy			20	%	5	Zone0, I
				25	%	5	Zone0, I to II, II'
Uniformity between signal channels	ΔSr			10	%	6	
	ΔSb			10	%	6	
Dark signal	Ydt			2	mV	7	Ta=60°C
Dark signal shading	ΔYdt			1	mV	8	Ta=60°C
Flicker Y	Fy			2	%	9	
Flicker R-Y	Fcr			5	%	9	
Flicker B-Y	Fcb			5	%	9	
Horizontal stripes R	Lcr			4	%	10	
Horizontal stripes G	Lcg			4	%	10	
Horizontal stripes B	Lcb			4	%	10	
Horizontal stripes W	Lcw			4	%	10	
Lag	ΔYlag			0.5	%	11	

Zone chart of Video signal shading



Testing System



Note) Adjust AMP amplifier so that total gains between A and Y and between A and C equal 1.

Test Method

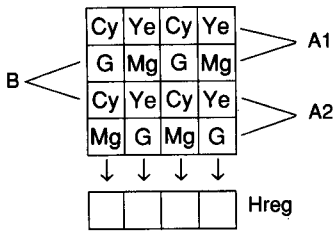
Test conditions

1) Through the following tests the substrate voltage should set to the value displayed on the device, while the device drive conditions should be kept within the range of the bias and clock voltage conditions.

2) Through the following tests defects are excluded, and unless otherwise specified the optical black level (Hence forth referred to as OPB) is set as the reference for the signal output which is taken as the Y signal output or the Chroma signal output of the testing system.

Color coding of CFA (Color Filter Array) & Composition of luminance (Y) and chrominance (C) signals.

CFA of this image sensor is shown in the Figure. This complementary CFA is used with a "field integration mode", where all of the photosites are read out during each video field. Signals from two vertically adjacent photosites, such as line A1 or A2 for field A, are summed when the image charge is transferred into the vertical storage columns. The readout line pairing is shifted down one line for field B. The sensor output signals through the horizontal shift register (H reg.) at line A1 are



Color Coding Diagram

[G+Cy], [Mg+Ye], [G+Cy], [Mg+Ye].

These signals are processed in order to compose Y and C signals. By adding the two adjacent signals at line A1, Y signal is formed as follows:

$$Y = \{(G+Cy) + (Mg+Ye)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

C signal is composed by subtracting the two adjacent signals at line A1.

$$R - Y = \{(Mg+Ye) - (G+Cy)\}$$
$$= \{2R-G\}$$

Next, the signals through H reg. at line A2 are

[Mg+Cy], [G+Ye], [Mg+Cy], [G+Ye]

Similarly, Y and C signals are composed at line A2.

$$Y = \{(G+Ye) + (Mg+Cy)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

$$-(B-Y) = \{(G+Ye) - (Mg+Cy)\}$$
$$= -\{2B-G\}$$

Accordingly, Y signal is balanced in relation to the scanning lines, and C signal takes the form of R–Y and –(B–Y) on alternate lines.
It is the same for B field.

Definition of standard imaging conditions

①Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 cd/m² 3200K Halogen source), at F5.6 with a typical test lens, and CM-500S (t=1.0 mm) for IR cut filter.

②Standard imaging condition II: Use a light source with uniformity within 2%, color temperature of 3200K and CM-500S (t=1.0 mm) as IR cut filter. The light intensity is adjusted in accordance with the average value of Y signals (Y_A) indicated in each item.

1) Set to standard imaging condition I and measure Y signal (S) at the center of the screen.

2) Set to imaging condition II. Adjust light intensity to 10 times when Y signal output average value Y_A=150mV. Then test Y signal Min. value.

3) Set to imaging condition II. Adjust light intensity to 500 times when Y signal output average value Y_A=150mV. Stop Read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the Max. value Y_{SM} of Y signal output.

$$SM = (Y_{SM}/Y_A) \times {}^1/_{500} \times {}^1/_{10} \times 100\ (\%) \quad ({}^1/_{10}V)$$

4) Set to imaging condition II. Adjust light intensity to 1000 times when Y signal output average value Y_A=150mV. Then check that there is no blooming.

5) Video signal shading SHy
Set to standard imaging condition II. Test Y signal Max. (Y max.) and Min. (Y min.) values. Adjust light intensity to obtain a Y signal output average value (Y_A) of about 150mV.

$$SHy = (Ymax - Ymin)/Y_A \times 100\ (\%)$$

6) Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 150mV. Test the Max. (Cr max. and Cb max.) and Min. (Cr min. and Cb min.) values of C signals from R-Y and B-Y channels.

$$\Delta Sr = |\ (Cr\ max. - Cr\ min.)/Y_A\ | \times 100\ (\%)$$
$$\Delta Sb = |\ (Cb\ max. - Cb\ min.)/Y_A\ | \times 100\ (\%)$$

7) Test the average Y signal voltage when the device ambient temperature is at 60°C and light is obstructed with horizontal idle transfer level as reference.

8) Following 7, test Max. (Yd max.) and Min. (Yd min.) values of Y signal output. Only keep spot defects out of this range.

$$\Delta Ydt = Yd\ max - Yd\ min$$

9) ① Fy
Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 150 mV. Test the Y signal difference (ΔYf) between even field and odd field.

$$Fy = (\Delta Yf/Y_A) \times 100\ (\%)$$

② Fcr, Fcb
Set to standard imaging condition II. Insert R and B filter respectively, and test the C signal difference (ΔCr, ΔCb) between even field and odd field and the C signal output average value (C_{Ar}, C_{Ab}). At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

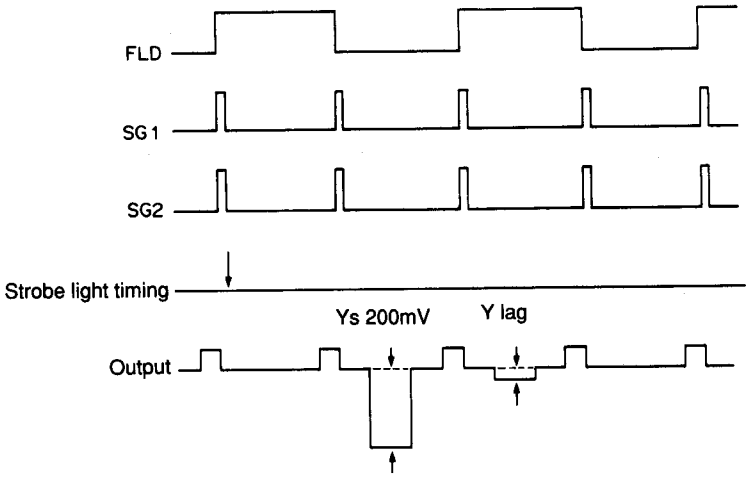
$$Fci = (\Delta Ci/C_{Ai}) \times 100\ (\%) \quad (i = r, b)$$

10) Set to standard imaging condition II. Insert W, R, G and B filters respectively, and test the signal difference (ΔYlw, ΔYlr, ΔYlg, ΔYlb) between Y signal lines of the same field. At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

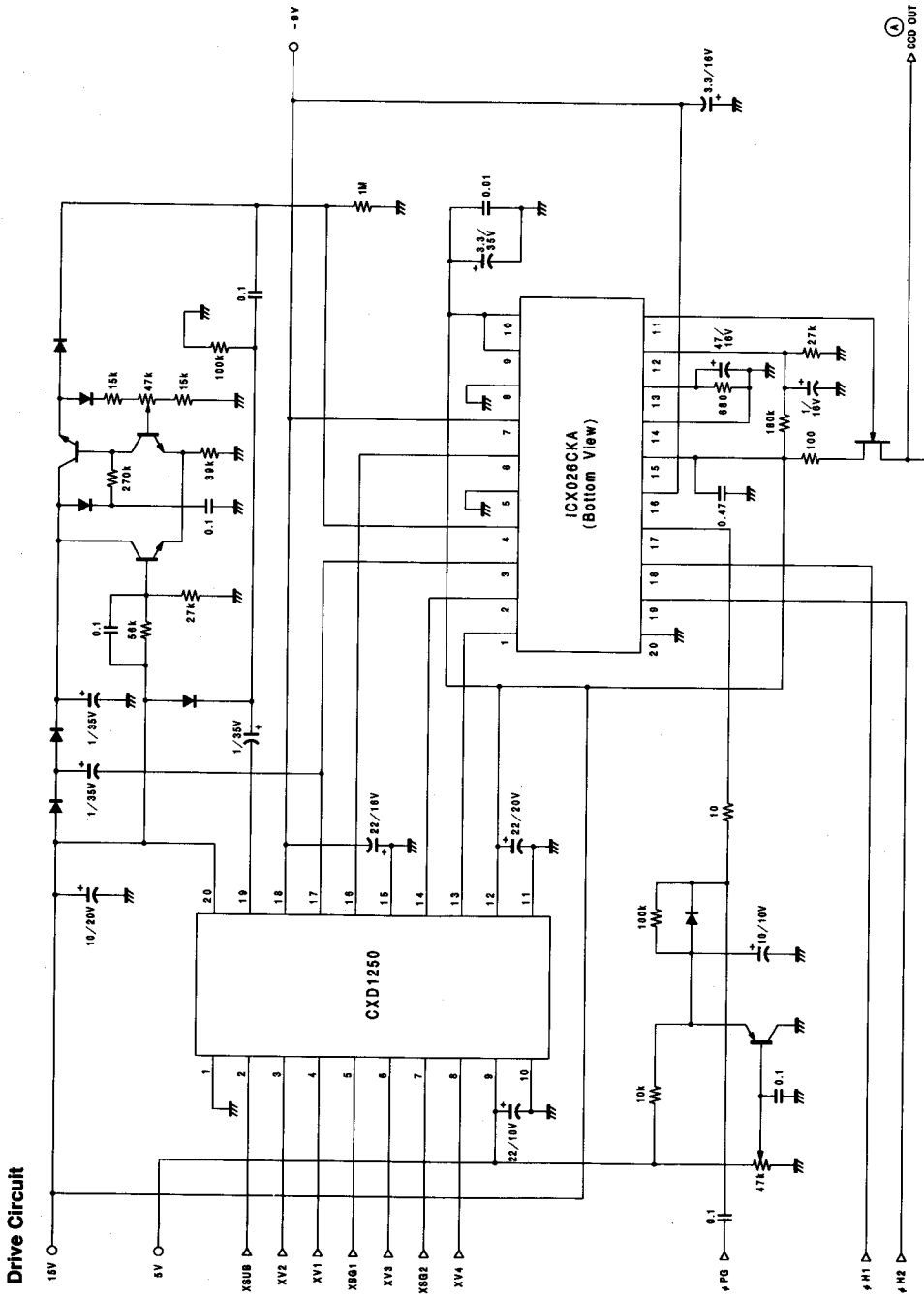
$$Lci = (\Delta Yli/Y_A) \times 100\ (\%) \quad (i = w, r, g, b)$$

11) Light a stroboscopic tube with the following timing and test the lag.

$$\Delta Ylag = (Ylag/Ys) \times 100\ (\%)$$

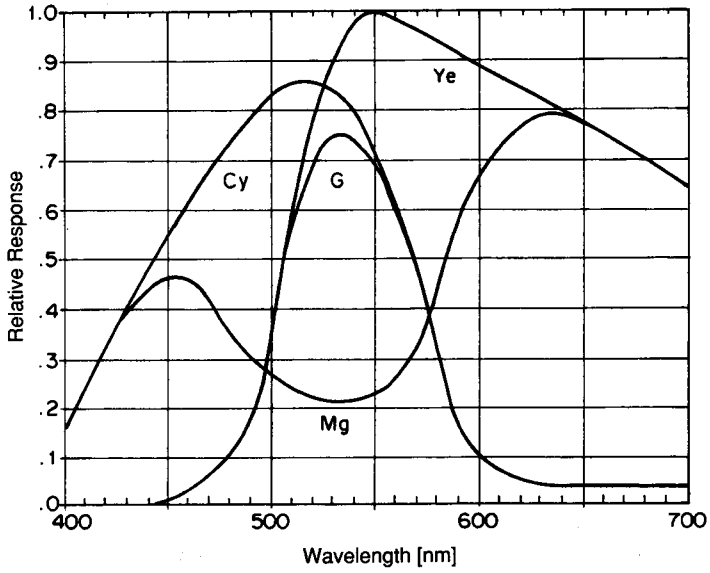


Drive Circuit

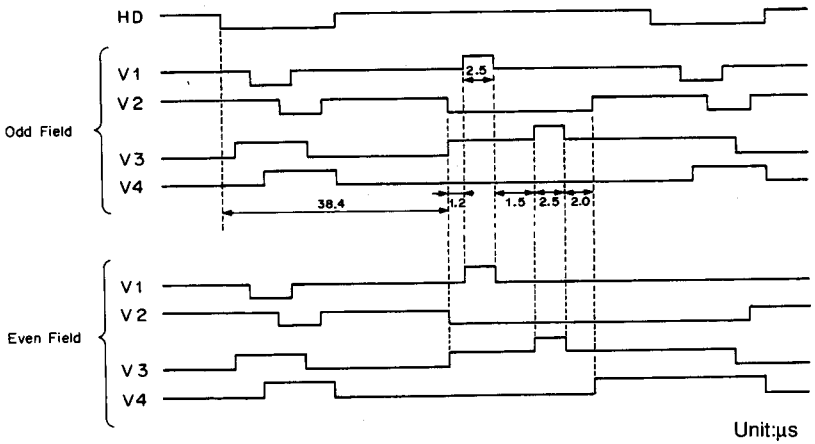


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

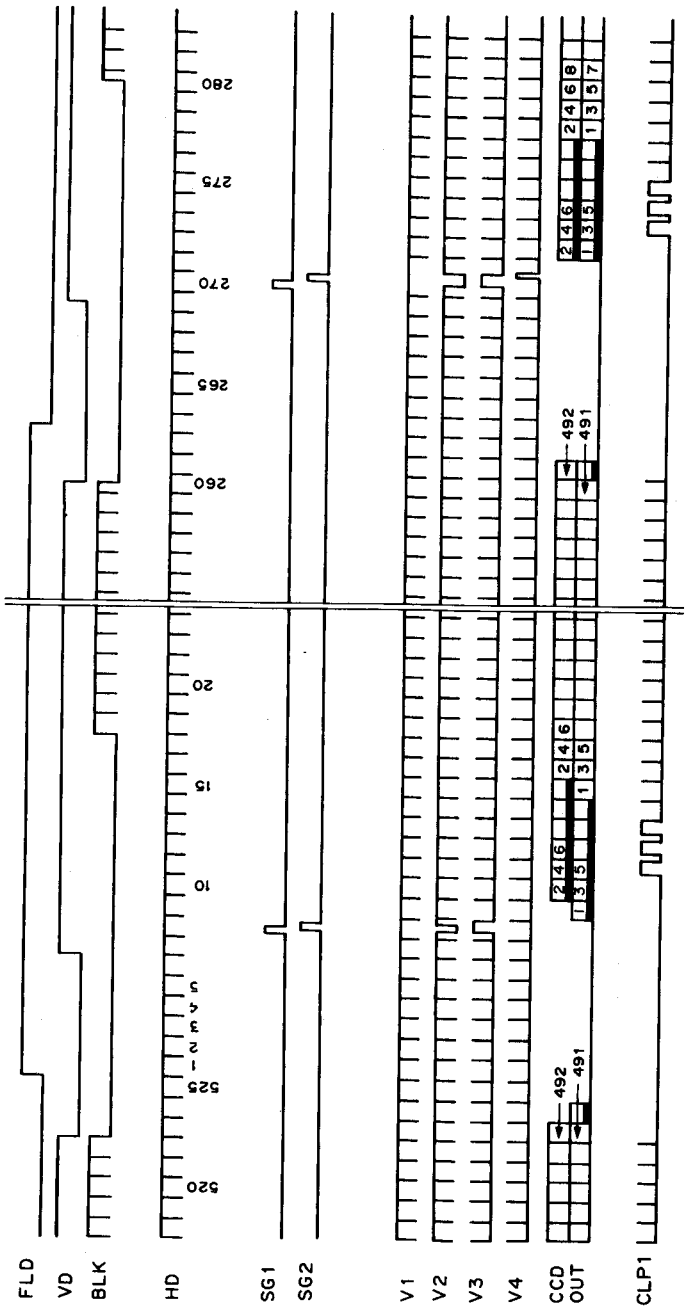
Spectral Sensitivity Characteristics
(Excluding light source characteristics, including lens characteristics)



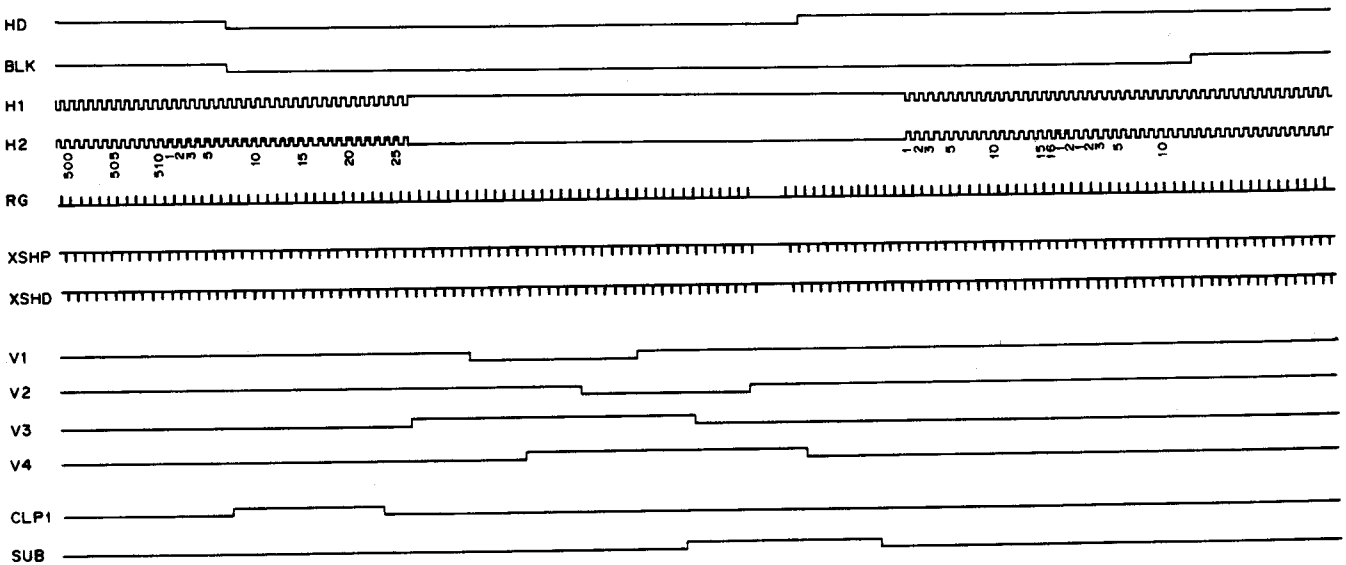
Using read out clock timing chart



Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



(During electronic shutter operation)

Handling Instructions

1) Static charge prevention
CCD image sensor are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount cool sufficiently.
c) To dismount an imaging device do not use a solder pult. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

SONY®

ICX027BKA

1/2 inch CCD Image Sensor for PAL Color Camera

Description

ICX027BKA is an interline transfer CCD solid-state imager suitable for PAL 1/2 inch color video cameras. High sensitiveness is achieved through the adoption of Ye, Cy, Mg and G complementary color mosaic filters and HAD (Hole Accumulated Diode) sensors.

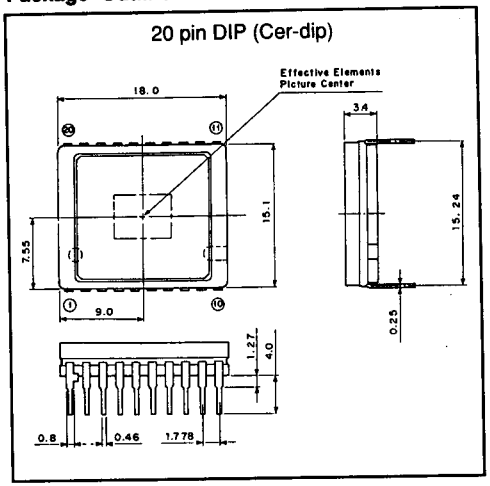
This chip features a field integration read out system, an electronic shutter with variable charge-storage time and 20 pin Cer-DIP package.

Features

- High sensitivity (+6 dB compare with ICX027AK)
- Optical size 1/2 inch format
- Field integration read out system
- Low dark current
- Ye, Cy, Mg, G on chip type complementary color mosaic filter.
- Horizontal register 5V drive
- High antiblooming
- Low smear
- Variable speed electronic shutter

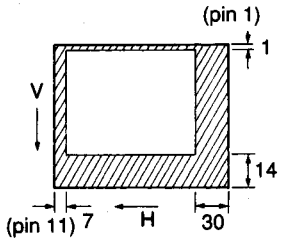
Package Outline

Unit: mm

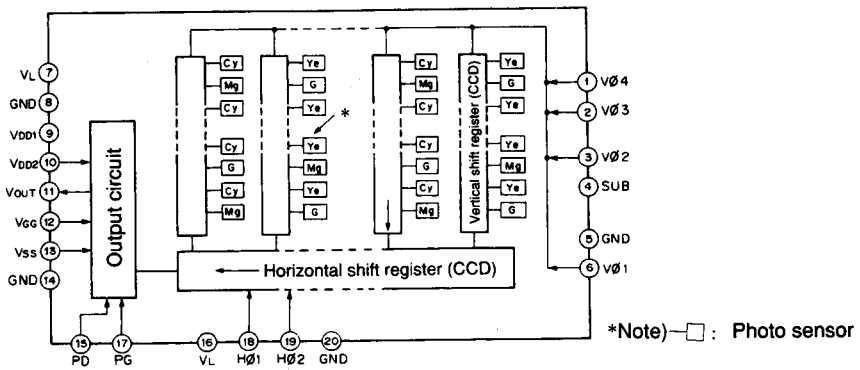


Device Structure

- Number of effective pixels 500 (H) × 582 (V)
- Number of total pixels 537 (H) × 597 (V)
- Interline transfer CCD image sensor
- Chip size 7.84 mm (H) × 6.40 mm (V)
- Unit cell size 12.7 μm (H) × 8.3 μm (V)
- Optical black
  - Horizontal (H) direction Front 7 pixels Rear 30 pixels
  - Vertical (V) direction Front 14 pixels Rear 1 pixels
- Number of dummy bits
  - Horizontal 16
  - Vertical 1 (even field only)
- Substrate material silicon



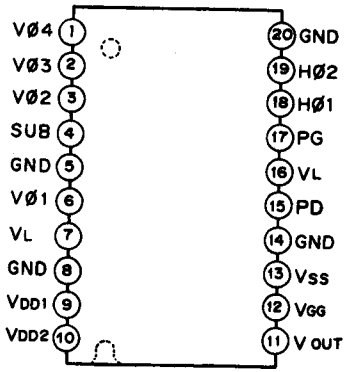
Optical black position (Top View)



*Note)—□ : Photo sensor

E91644-YA

Pin Configuration (Top View)



Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	11	VOUT	Signal output
2	Vφ3	Vertical register transfer clock	12	VGG	Output amplifier gate bias
3	Vφ2	Vertical register transfer clock	13	VSS	Output amplifier source
4	SUB	Substrate (Overflow drain)	14	GND	GND
5	GND	GND	15	PD	Precharge drain bias
6	Vφ1	Vertical register transfer clock	16	VL	Protective transistor bias
7	VL	Protective transistor bias	17	PG	Precharge gate clock
8	GND	GND	18	Hφ1	Horizontal register transfer clock
9	VDD1	Output amplifier drain supply	19	Hφ2	Horizontal register transfer clock
10	VDD2	Output amplifier drain supply	20	GND	GND

Absolute Maximum Ratings

• Substrate voltage	SUB – GND	–0.3 to +55 V
• Supply voltage	VDD1, VDD2, PD, VOUT, VSS, – GND	–0.3 to +18 V
	VDD1, VDD2, PD, VOUT, VSS, – SUB	–55 to +10 V
• Clock input voltage	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – GND	–15 to +20 V
	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – SUB	–65 to +10 V
• Voltage difference between vertical clock input pins		15 V*
• Voltage difference between horizontal clock input pins		17 V
• Hφ1, Hφ2, – Vφ4,		–17 to +17 V
• PG, VGG – GND		–10 to +15 V
• PG, VGG – SUB		–55 to +10 V
• VL – SUB		–65 to +0.3 V
• Beside GND, SUB, VL – VL		–0.3 to +30 V
• Storage temperature		–30 to +80°C
• Operating temperature		–10 to +55°C

***Note)** +27 V (Max.) when clock width < 10 μs, duty factor < 0.1%.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD1}, V_{DD2}	14.55	15.0	15.45	V	V_{DD1} = V_{DD2}
Precharge drain voltage	V_{PD}	14.55	15.0	15.45	V	V_{PD} = V_{DD1} = V_{DD2}
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	V_{SS}	Ground through 680 Ω resistor				±5%
Substrate voltage adjustment range	V_{SUB}	7		19	V	*1
Fluctuation range after substrate voltage adjustment	V_{SUB}	-3		+3	%	
Protective transistor bias	V_L	*2				

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		2.5		mA	I_{DD} = I_{DD1} + I_{DD2}
Input current	I_{IN1}			1	μA	*3
Input current	I_{IN2}			10	μA	*4

Note) *1. Substrate voltage (V_{SUB}) setting value display.
Substrate voltage setting value is displayed at the back of the device through a code address. Adjust so as to obtain the displayed voltage at SUB pin.

V_{SUB} code address – two digits display

□ ↑ Integral part

□ ↑ Decimal part

The relation between code address of integral part and actual numerical values.

Code address of integral part	7	8	9	A	B	C	D	E	F	G	H	I	J
Numerical Value	7	8	9	10	11	12	13	14	15	16	17	18	19

<Example> F5 → 15.5 (V)

*2. V_L setting is V_{VL} of the vertical transfer clock waveform.

*3. 1) Current to earth when 18V is applied to pins V_{DD1}, V_{DD2}, V_{OUT}, Vss and SUB pin. However, pins that are not tested are grounded.
2) Current to earth when 20V is sequentially applied to pins $V\phi1$, $V\phi2$, $V\phi3$, $V\phi4$, $H\phi1$, and $H\phi2$. However, 20V is applied to SUB while pins that are not tested are grounded.
3) Current to earth when 15V is sequentially applied to pins PG and V_{GG}. However, 15V is applied to SUB while pins that are not tested are grounded.

*4. 1) Current to earth when 55V is applied to SUB pin. Pins that are not tested are grounded.
2) Current to earth when V_L is grounded, GND and SUB are open and 30V is applied to other pins.

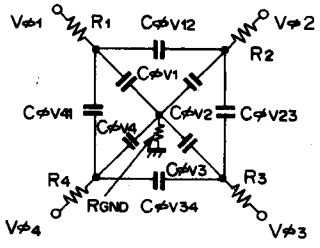
Clock Voltage Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	No.	Remarks
Read out clock voltage	V_{VT}	14.3	15.0	15.7	V	2,6	*1
Vertical transfer clock voltage *2	V_{VH1},V_{VH2},V_{VH3},V_{VH4}	−0.2	0	0.2	V	1,2,3,6	$V_{VH}=(V_{VH1}+V_{VH2})/2$
	V_{VL1},V_{VL2},V_{VL3},V_{VL4}	−9.6	−9.0	−8.3	V	1,2,3,6	$V_{VL}=(V_{VL3}+V_{VL4})/2$
	$V_{\phi V}$	8.1	9.0	9.8	V	1,2,3,6	$V_{\phi V}=V_{VHn}-V_{VLn}$ (n=1 to 4)
	$\lvert V_{VH1} - V_{VH2} \rvert$			0.2	V	3,6	
	$V_{VH3} - V_{VH}$	−0.4		0.1	V	2,3,6	
	$V_{VH4} - V_{VH}$	−0.4		0.1	V	1,3,6	
	V_{VHH}			0.8	V	1,2,3,6	High level coupling
	V_{VHL}			1.0	V	1,2,3,6	High level coupling
	V_{VLH}			0.8	V	1,2,3,6	Low level coupling
	V_{VLL}			0.8	V	1,2,3,6	Low level coupling
Horizontal transfer clock voltage	$V_{\phi H}$	4.7	5.0	5.3	V	18,19	*3
	V_{HL}	−0.05	0	0.05	V	18,19	
Precharge gate clock voltage	$V_{\phi PG}$	8.0		11.5	V	17	*4
	V_{PGL}	−0.1	0	0.1	V	17	
Substrate clock voltage	$V_{\phi SUB}$	23.0		34.0	V	4	*5

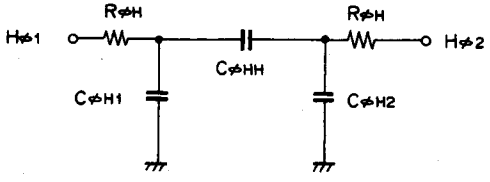
Note) *1. See Fig. 1.
*2. See Fig. 2.
*3. See Fig. 3.
*4. See Fig. 3.
*5. See Fig. 4.

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$, $C_{\phi V3}$		1000		pF	
Capacitance between vertical transfer clock and GND	$C_{\phi V2}$, $C_{\phi V4}$		1200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$, $C_{\phi V34}$		1400		pF	
Capacitance between vertical transfer clocks	$C_{\phi V23}$, $C_{\phi V41}$		900		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, $C_{\phi H2}$		70		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Capacitance between precharge gate clock and GND	$C_{\phi PG}$		8		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		400		pF	
Vertical transfer clock serial resistor	R_1,R_2,R_3,R_4		33		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock serial resistor	$R_{\phi H}$		10		Ω	



Vertical transfer clock equivalent circuit



Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

1. Read out clock waveform

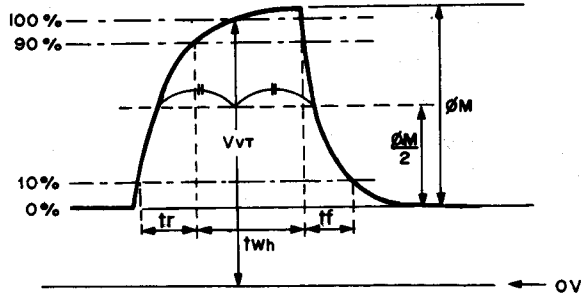


Fig.1

2. Vertical transfer clock waveform

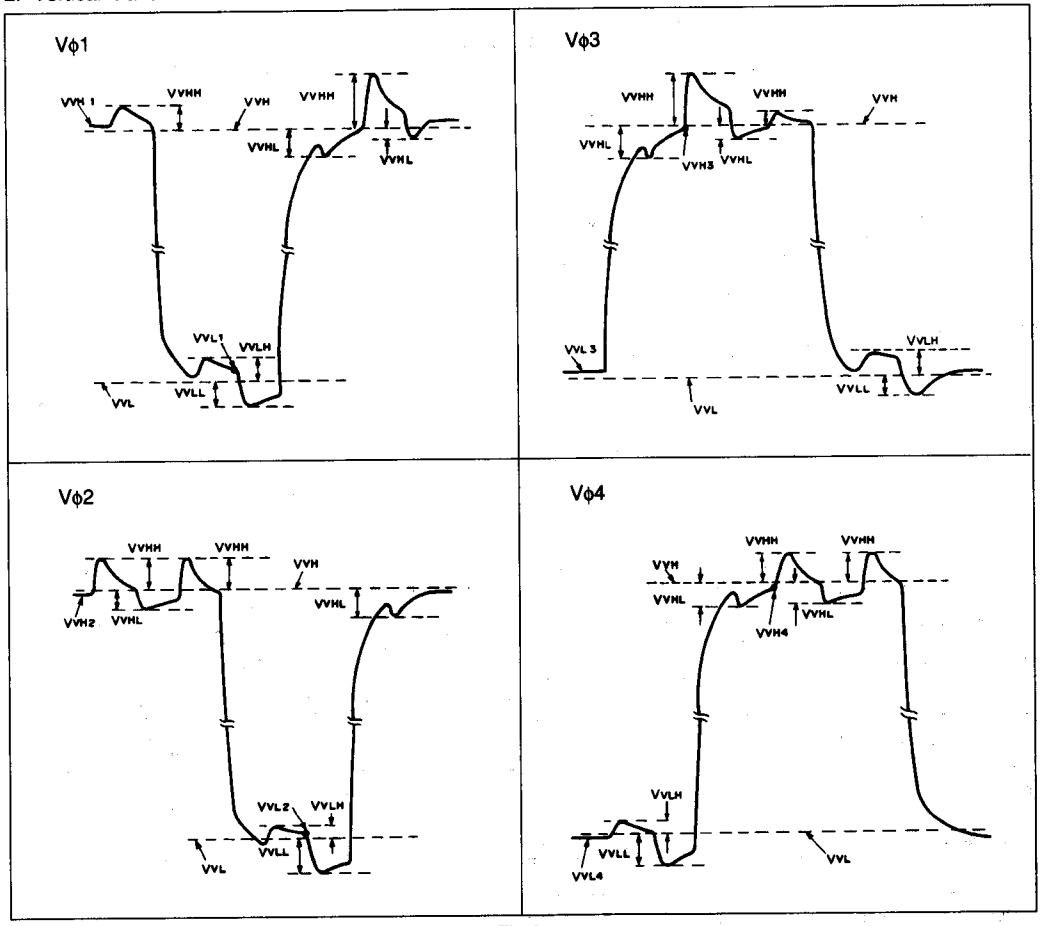


Fig.2

3. Horizontal transfer clock waveform/Precharge gate clock waveform

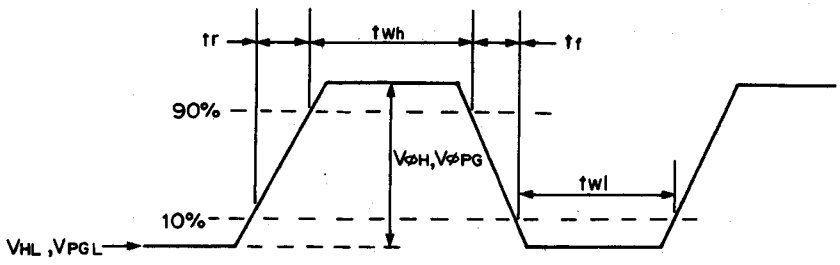


Fig. 3

4. Substrate clock waveform

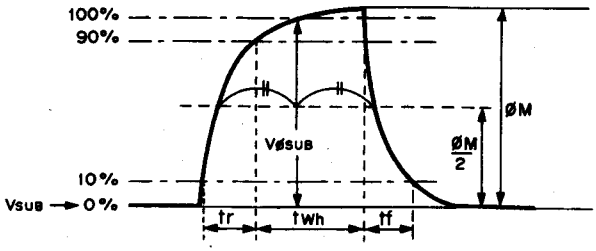


Fig. 4

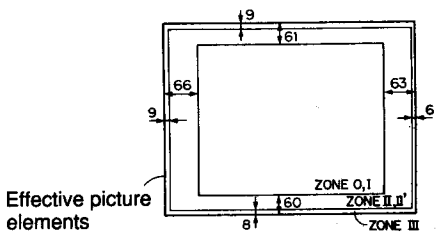
Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	V_T	1.5	1.85							0.5			0.5	µs	During read out
Vertical transfer clock	$V\phi_1, V\phi_2, V\phi_3, V\phi_4$									0.45	0.015		0.25	µs	*
Horizontal transfer clock	$H\phi$	38	42		38	42			12	15		10	15	ns	During imaging
Horizontal transfer clock	$H\phi_1$		5.6						0.012			0.01		µs	During parallel serial conversion.
Horizontal transfer clock	$H\phi_2$					5.6			0.012			0.01		µs	During parallel serial conversion.
Precharge gate clock	ϕ_{PG}	15	17		76	82			4			3		ns	
Substrate clock	ϕ_{SUB}	1.5	2.1							0.5			0.5	µs	During charge drain.

***Note)** When vertical transfer clock driver CXD1250 is in use.

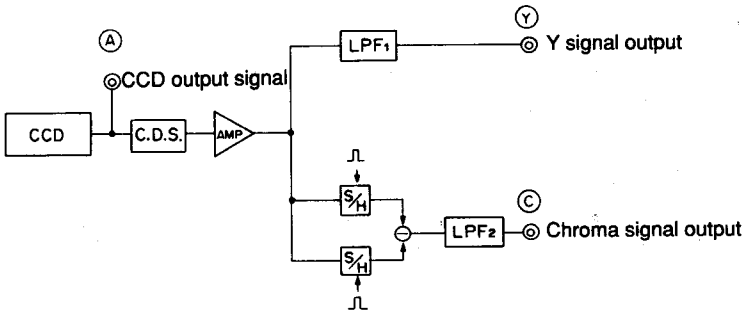
Operating Characteristics Ta = 25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	240	320		mV	1	
Saturation signal	Ysat	450			mV	2	Ta=55°C
Smear	SM		0.005	0.015	%	3	
Blooming margin		1000			times	4	
Video signal shading	SHy			20	%	5	Zon0, I
				25	%	5	Zone0 to II'
Uniformity between signal channels	ΔSr			10	%	6	
	ΔSb			10	%	6	
Dark signal	Ydt			2	mV	7	Ta=55°C
Dark signal shading	ΔYdt			1	mV	8	Ta=55°C
Flicker Y	Fy			2	%	9	
Flicker R-Y	Fcr			5	%	9	
Flicker B-Y	Fcb			5	%	9	
Horizontal stripes R	Lcr			4	%	10	
Horizontal stripes G	Lcg			4	%	10	
Horizontal stripes B	Lcb			4	%	10	
Horizontal stripes W	Lcw			4	%	10	
Lag	ΔYlag			0.5	%	11	

Zone chart of Video signal shading



Testing System



Note) Adjust AMP amplifier so that total gains between Ⓐ and Ⓨ and between Ⓐ and Ⓒ equal 1.

Test Method

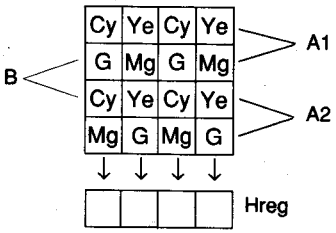
Test conditions

1) Through the following tests the substrate voltage should set to the value displayed on the device, while the device drive conditions should be kept within the range of the bias and clock voltage conditions.

2) Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OPB) is set as the reference for the signal output which is taken as the Y signal output or the Chroma signal output of the testing system.

Color coding of CFA (Color Filter Array) & Composition of luminance (Y) and chrominance (C) signals.

CFA of this imager is shown in the Figure. This complementary CFA is used with a "field integration mode", where all of the photosites are read out during each video field. Signals from two vertically adjacent photosites, such as line A1 or A2 for field A, are summed when the image charge is transferred into the vertical storage columns. The readout line pairing is shifted down one line for field B. The sensor output signals through the horizontal register (H reg.) at line A1 are



Color Coating Diagram

[G+Cy], [Mg+Ye], [G+Cy], [Mg+Ye].

These signals are processed in order to compose Y and C signals. By adding the two adjacent signals at line A1, Y signal is formed as follows:

$$Y = \{(G+Cy) + (Mg+Ye)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

C signal is composed by subtracting the two adjacent signals at line A1.

$$R - Y = \{(Mg+Ye) - (G+Cy)\}$$
$$= \{2R-G\}$$

Next, the signals through H reg. at line A2 are

[Mg+Cy], [G+Ye], [Mg+Cy], [G+Ye]

Similarly, Y and C signals are composed at line A2.

$$Y = \{(G+Ye) + (Mg+Cy)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

$$-(B-Y) = \{(G+Ye) - (Mg+Cy)\}$$
$$= -\{2B-G\}$$

Accordingly, Y signal is balanced in relation to the scanning lines, and C signal takes the form of R–Y and –(B–Y) on alternate lines.
It is the same for B field.

Definition of Standard Imaging Conditions

①Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 cd/m², 3200K Halogen source), at F5.6 with a typical test lens, and CM-500S (t=1.0 mm) for IR cut filter.

②Standard imaging condition II: Use a light source with uniformity within 2%, color temperature of 3200K and CM-500S (t=1.0 mm) as IR cut filter. The light intensity is adjusted in accordance with the average value of Y signals (Y_A) indicated in each item.

1) Set to standard imaging condition I and measure Y signal (S) at the center of the screen.

2) Set to imaging condition II. Adjust light intensity to 10 times when Y signal output average value Y_A=150mV. Then test Y signal Min. Value.

3) Set to imaging condition II. Adjust light intensity to 500 times when Y signal output average value Y_A=150mV. Stop Read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the Max. value Y_{SM} of Ysignal output.

$$SM = (Y_{SM}/Y_A) \times {}^1/_{500} \times {}^1/_{10} \times 100\ (\%) \quad ({}^1/_{10}V)$$

4) Set to imaging condition II. Adjust light intensity to 1000 times when Y signal output average value Y_A=150mV. Then check that there is no blooming.

5) Video signal shading SHy
Set to standard imaging condition II. Test Y signal Max. (Y max.) and Min. (Y min.) values. Adjust light intensity to obtain a Y signal output average value (Y_A) of about 150mV.

$$SHy = (Ymax - Ymin)/Y_A \times 100\ (\%)$$

6) Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 150mV. Test the Max. (Cr max. and Cb max.) and Min. (Cr min. and Cb min.) values of C signals from R-Y and B-Y channels.

$$\Delta Sr = |\ (Crmax - Crmin)/Y_A\ | \times 100\ (\%)$$
$$\Delta Sb = |\ (Cbmax - Cbmin)/Y_A\ | \times 100\ (\%)$$

7) Test the average Y signal voltage when the device ambient temperature is at 55°C and light is obstructed with horizontal idle transfer level as reference.

8) Following 7, test Max. (Yd max) and Min. (Yd min) values of Y signal output. Only keep spot defects out of this range.

$$\Delta Ydt = Ydmax - Ydmin$$

9) ① Fy

Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 150 mV. Test the Y signal difference (ΔYf) between even field and odd field.

$$Fy = (\Delta Yf/Y_A) \times 100\ (\%)$$

② Fcr, Fcb

Set to standard imaging condition II. Insert R and B filter respectively, and test the C signal difference (ΔCr, ΔCb) between even field and odd field and the C signal output average value (C_{Ar}, C_{Ab}). At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

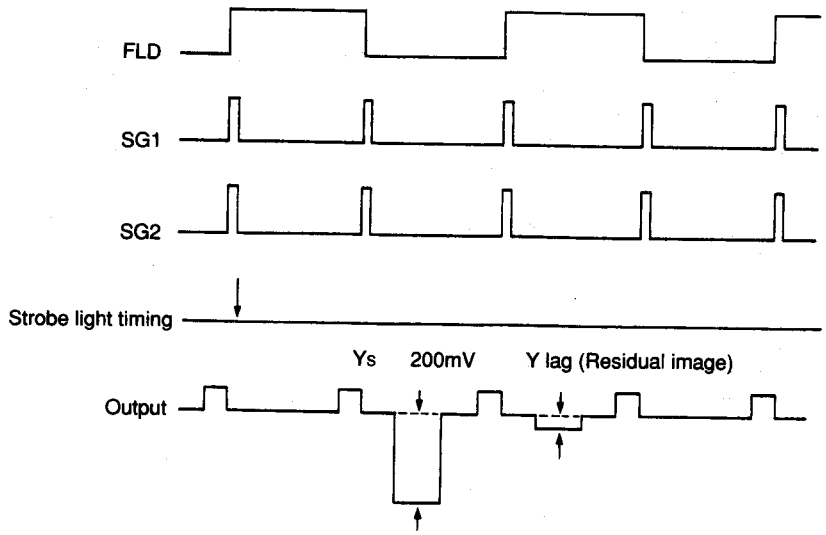
$$Fci = (\Delta Ci/C_{Ai}) \times 100\ (\%) \quad (i = r, b)$$

10) Set to standard imaging condition II. Insert W,R,G and B filters respectively and test the signal difference (ΔYlw, ΔYlr, ΔYlg, ΔYlb) between Y signal lines of the same field. At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

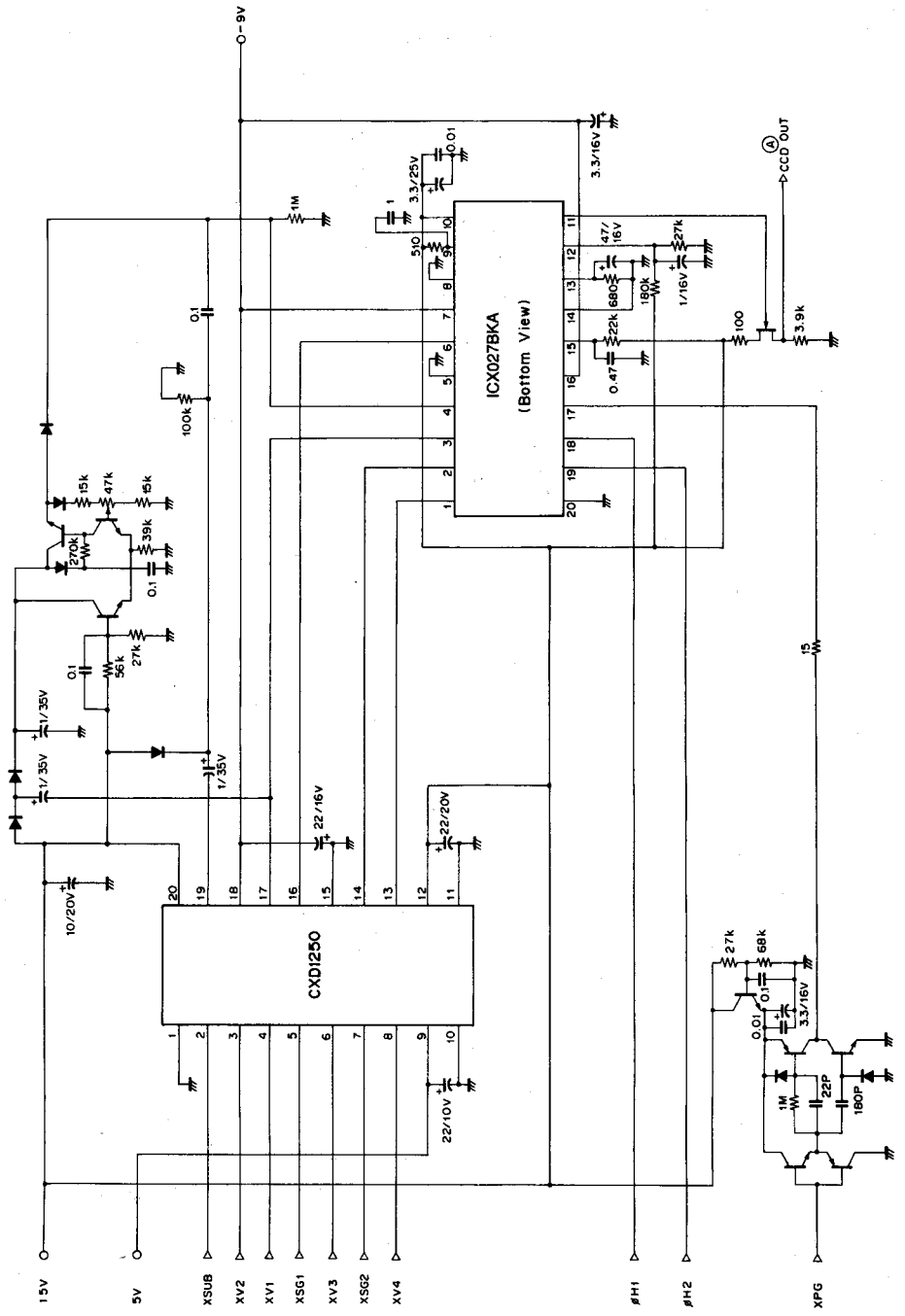
$$Lci = (\Delta Yli/Y_A) \times 100\ (\%) \quad (i = w, r, g, b)$$

11) Light a stroboscopic tube with the following timing and test the residual image.

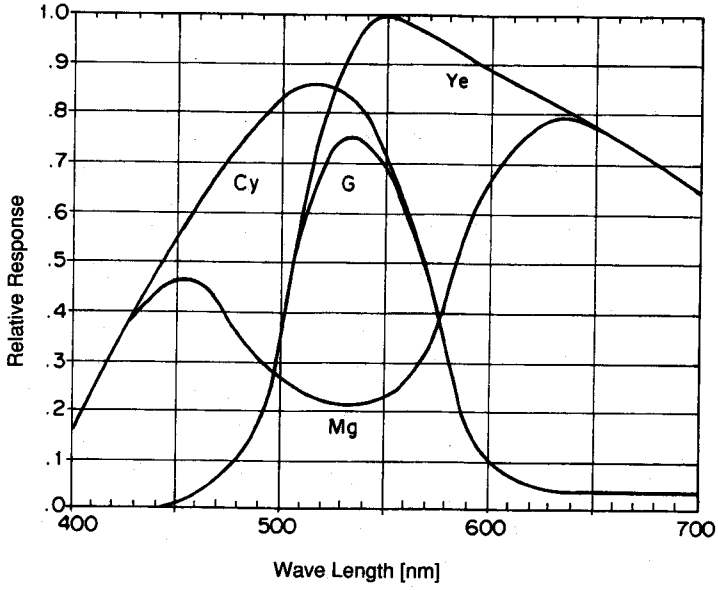
$$\Delta Ylag = (Ylag/Ys) \times 100\ (\%)$$



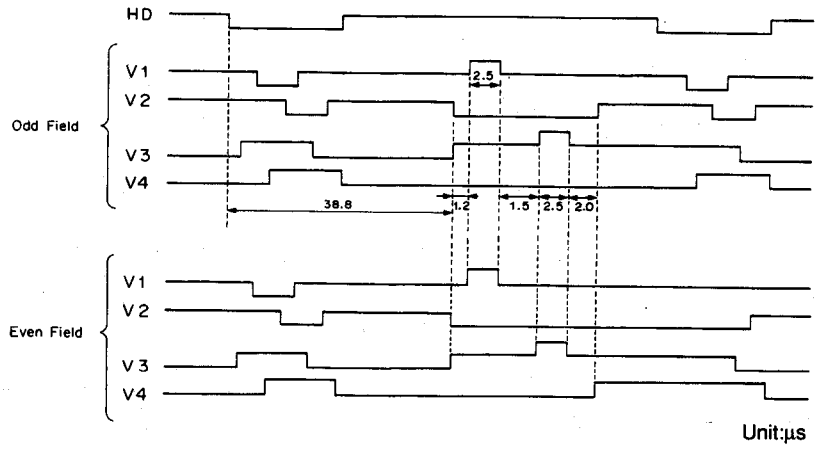
Drive Circuit



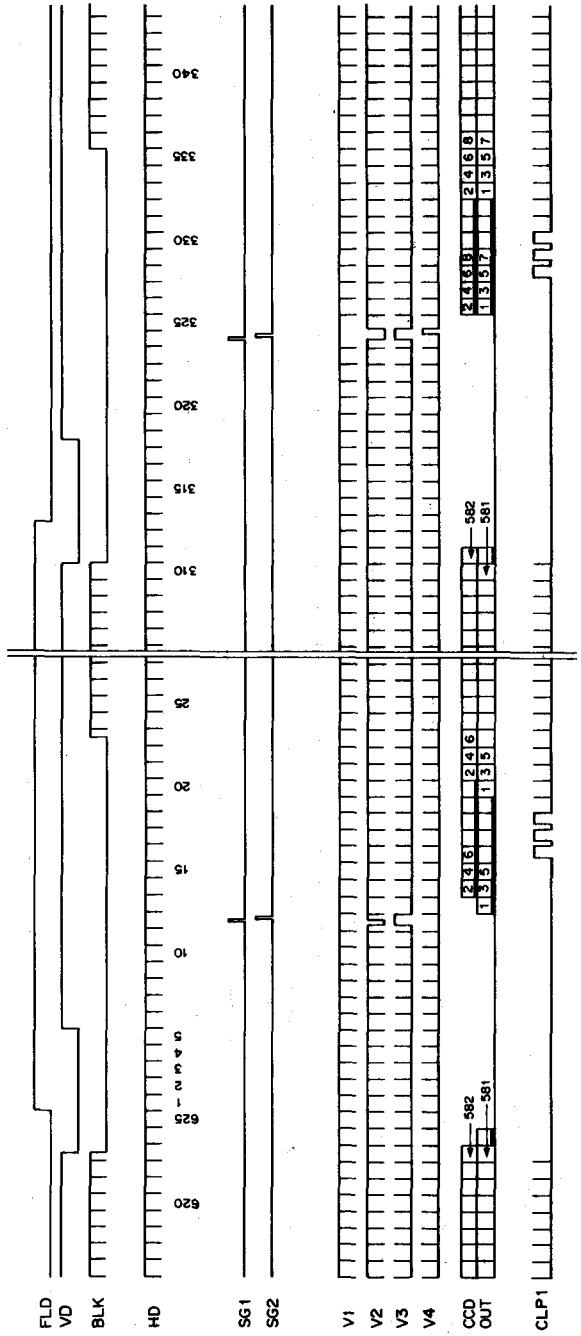
Spectral Sensitivity Characteristics
(Excluding light source characteristics, including lens characteristics)



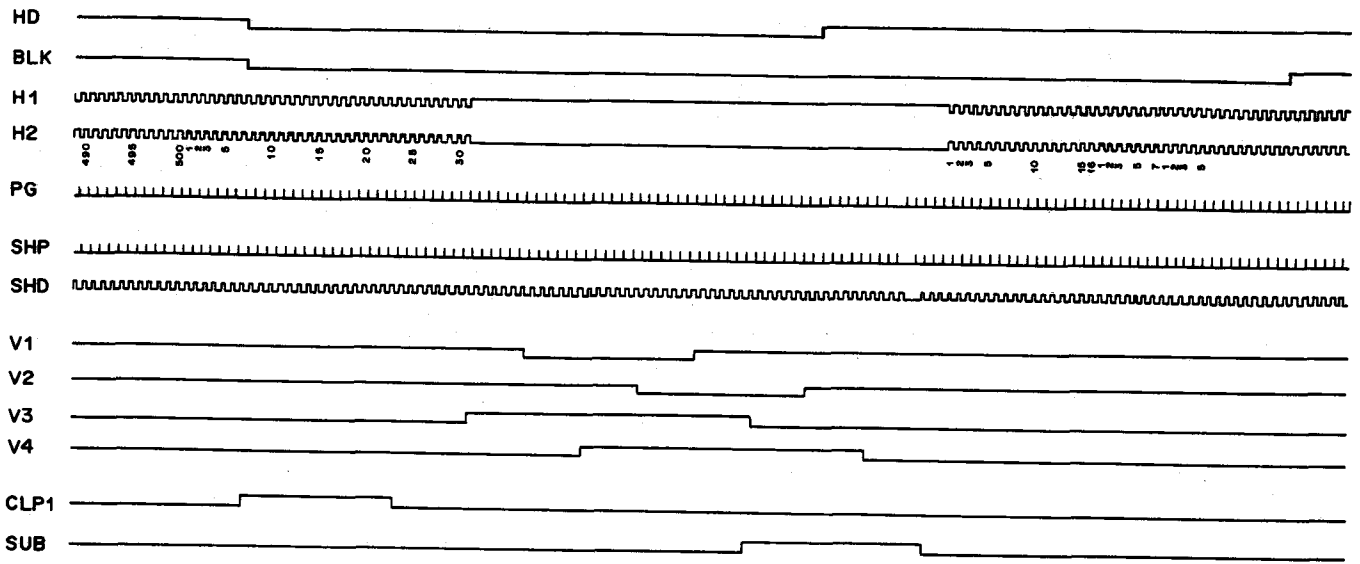
Using read out clock timing chart



Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



During electronic shutter operation

Handling Instructions

1) Static charge prevention
CCD image sensor are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount cool sufficiently.
c) To dismount an imaging device do not use a solder pult. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

SONY®

ICX027CKA

1/2 inch CCD Image Sensor for PAL Color Camera

Description

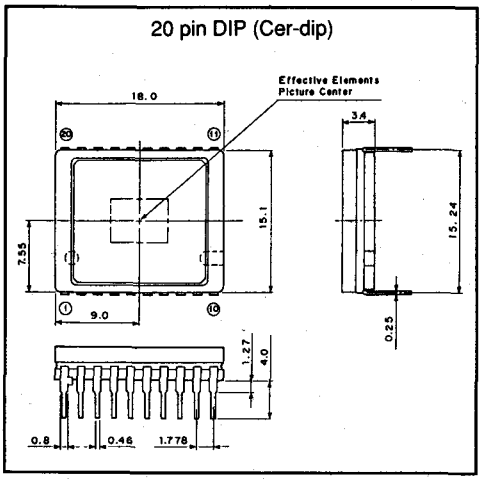
ICX027CKA is an interline transfer CCD solid-state image sensor suitable for PAL1/2 inch color video cameras. High sensitivity is achieved through the adoption of Ye, Cy, Mg and G complementary color mosaic filters and HAD (Hole-Accumulation Diode) sensors.

Beside correspondence with timing generator CXD1253, 5V drive of the reset gate is also possible.

This chip features a field integration read out system, an electronic shutter with variable charge-storage time and 20pin Cer-DIP package.

Package Outline

Unit: mm

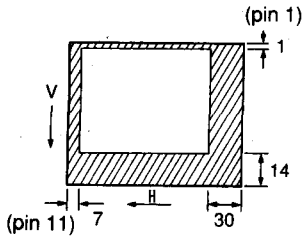


Features

- High sensitivity (+6 dB compare with ICX027AK)
- Optical size 1/2 inch format
- Field integration read out system
- Low dark current. High sensitivity HAD sensor
- Ye, Cy, Mg, G on chip type complementary color mosaic filter.
- Horizontal register 5V drive
- Reset gate 5V drive
- High antiblooming
- Low smear
- Variable speed electronic shutter

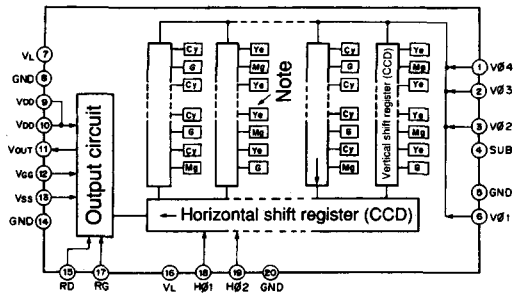
Device Structure

- Number of effective pixels 500 (H) × 582 (V)
- Number of total pixels 537 (H) × 597 (V)
- Interline transfer CCD image sensor
- Chip size 7.84 mm (H) × 6.40 mm (V)
- Unit cell size 12.7 µm (H) × 8.3 µm (V)
- Optical black
  - Horizontal (H) direction Front 7 pixels Rear 30 pixels
  - Vertical (V) direction Front 14 pixels Rear 1 pixel
- Number of dummy bits
  - Horizontal 16
  - Vertical 1 (even field only)
- Substrate material silicon



Optical black position (Top View)

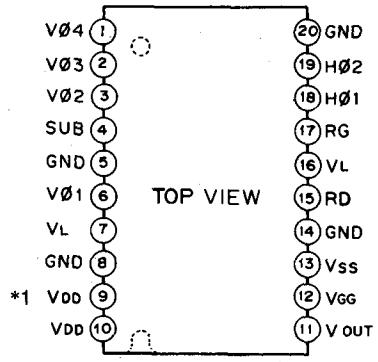
Block Diagram



Note) –□ : Photo sensor

E91646-YA

Pin Configuration (Top View)



*1 As Pins 9 and 10 are internally shorted, either one can be connected to the power supply while the other is kept open. Should both be connected to the power supply, make sure the same voltage is applied.

Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	11	VOUT	Signal output
2	Vφ3	Vertical register transfer clock	12	VGG	Output amplifier gate bias
3	Vφ2	Vertical register transfer clock	13	VSS	Output amplifier source
4	SUB	Substrate (Overflow drain)	14	GND	GND
5	GND	GND	15	RD	Reset drain bias
6	Vφ1	Vertical register transfer clock	16	VL	Protective transistor bias
7	VL	Protective transistor bias	17	RG	Reset gate clock
8	GND	GND	18	Hφ1	Horizontal register transfer clock
9	VDD	Output amplifier drain supply	19	Hφ2	Horizontal register transfer clock
10	VDD	Output amplifier drain supply	20	GND	GND

Absolute Maximum Ratings

• Substrate voltage	SUB – GND	–0.3 to +55	V
• Supply voltage	VDD, RD, VOUT, VSS, – GND	–0.3 to +18	V
	VDD, RD, VOUT, VSS, – SUB	–55 to +10	V
• Clock input voltage	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – GND	–15 to +20	V
	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – SUB	–65 to +10	V
• Voltage difference between vertical clock input pins		+15	V *2
• Voltage difference between horizontal clock input pins		+17	V
• Hφ1, Hφ2, – Vφ4		–17 to +17	V
• RG, VGG – GND		–10 to +15	V
• RG, VGG – SUB		–55 to +10	V
• VL – SUB		–65 to +0.3	V
• Beside GND, SUB, VL – VL		–0.3 to +30	V
• Storage temperature		–30 to +80	°C
• Operating temperature		–10 to +60	°C

*2 +27 V (Max.) when clock width < 10 µs, duty factor < 0.1%.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD}	14.55	15.0	15.45	V	
Reset drain voltage	V_{RD}	14.55	15.0	15.45	V	$V_{RD} = V_{DD}$
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	V_{SS}	Ground through 680 Ω resistor				±5%
Substrate voltage adjustment range	V_{SUB}	7.0		18.5	V	*1
Fluctuation range after substrate voltage adjustment	ΔV_{SUB}	−3		+3	%	
Reset gate clock voltage adjustment range	V_{RGL}	0.5		3.5	V	*1
Fluctuation range after reset gate clock voltage adjustment	ΔV_{RGL}	−3		+3	%	
Protective transistor bias	V_L	*2				

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		2.5		mA	
Input current	I_{IN1}			1	μA	*3
Input current	I_{IN2}			10	μA	*4

Note) *1. Substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) setting values are displayed at the back of the device through a code address. Adjust so as to obtain the displayed voltages at SUB and RG pins respectively.

V_{SUB} code address - 1 digit display
V_{RGL} code address - 1 digit display

□ ↑ V_{RGL} code address

□ ↑ V_{SUB} code address

The relation between code address and actual numerical values.

V_{RGL} code address	0	1	2	3	4	5	6
Numerical value	0.5	1.0	1.5	2.0	2.5	3.0	3.5

V_{SUB} code address	A	b	C	D	E	f	G	h	J	K	L	m
Numerical value	7.0	7.5	8.0	8.5	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5
V_{SUB} code address	N	P	Q	R	S	T	U	V	W	X	Y	Z
Numerical value	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5

<Example> "5L" → V_{RGL} = 3.0 V, V_{SUB} = 12.0 V

*2. V_L setting is V_{VL} of the vertical transfer clock waveform.

*3. 1) Current to earth when 18V is applied to pins V_{DD}, V_{OUT}, Vss and SUB pin. However, pins that are not tested are grounded.
2) Current to earth when 20V is sequentially applied to pins $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $H\phi_1$, and $H\phi_2$. However, 20V is applied to SUB while pins that are not tested are grounded.
3) Current to earth when 15V is sequentially applied to pins RG and V_{GG}. However, 15V is applied to SUB while pins that are not tested are grounded.

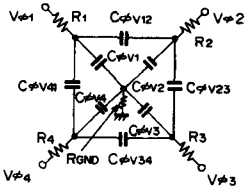
*4. 1) Current to earth when 55V is applied to SUB pin. Pins that are not tested are grounded.
2) Current to earth when V_L is grounded, GND and SUB are open and 30V is applied to other pins.

Clock Voltage Conditions

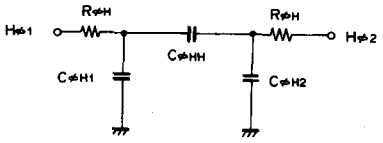
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform	Remarks
Read out clock voltage	V_{VT}	14.3	15.0	15.7	V	1	
Vertical transfer clock voltage	V_{VH1},V_{VH2},V_{VH3},V_{VH4}	−0.2	0	0.2	V	2	$V_{VH}=(V_{VH1}+V_{VH2})/2$
	V_{VL1},V_{VL2},V_{VL3},V_{VL4}	−9.6	−9.0	−8.3	V	2	$V_{VL}=(V_{VL3}+V_{VL4})/2$
	$V_{\phi V}$	8.1	9.0	9.8	V	2	$V_{\phi V}=V_{VHn}-V_{VLn}$ (n=1 to 4)
	$\lvert V_{VH1} - V_{VH2} \rvert$			0.2	V	2	
	$V_{VH3} - V_{VH}$	−0.4		0.1	V	2	
	$V_{VH4} - V_{VH}$	−0.4		0.1	V	2	
	V_{VHH}			0.8	V	2	High level coupling
	V_{VHL}			1.0	V	2	High level coupling
	V_{VLH}			0.8	V	2	Low level coupling
	V_{VLL}			0.8	V	2	Low level coupling
Horizontal transfer clock voltage	$V_{\phi H}$	4.7	5.0	5.3	V	3	
	V_{HL}	−0.05	0	0.05	V	3	
Reset gate clock voltage	$V_{\phi RG}$	4.5	5.0	5.5	V	4	When V_{RGL} is adjusted to the displayed value
	$V_{RGLH} - V_{RGLL}$			0.8	V	4	
	$V_{\phi RG}$	8.0		11.5	V	4	When V_{RGL} is fixed
	V_{RGL}	−0.1	0	0.1	V	4	
	$V_{RGLH} - V_{RGLL}$			0.8	V	4	
Substrate clock voltage	$V_{\phi SUB}$	23.0		34.0	V	5	

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$, $C_{\phi V3}$		1000		pF	
Capacitance between vertical transfer clock and GND	$C_{\phi V2}$, $C_{\phi V4}$		1200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$, $C_{\phi V34}$		1400		pF	
Capacitance between vertical transfer clocks	$C_{\phi V23}$, $C_{\phi V41}$		900		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, C		70		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		8		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		400		pF	
Vertical transfer clock serial resistor	R_1,R_2,R_3,R_4		33		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock serial resistor	$R_{\phi H}$		10			



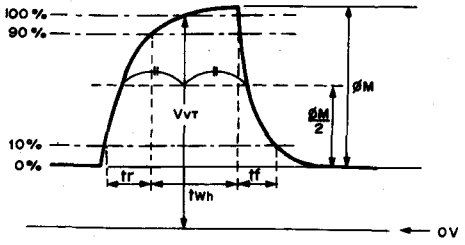
Vertical transfer clock equivalent circuit



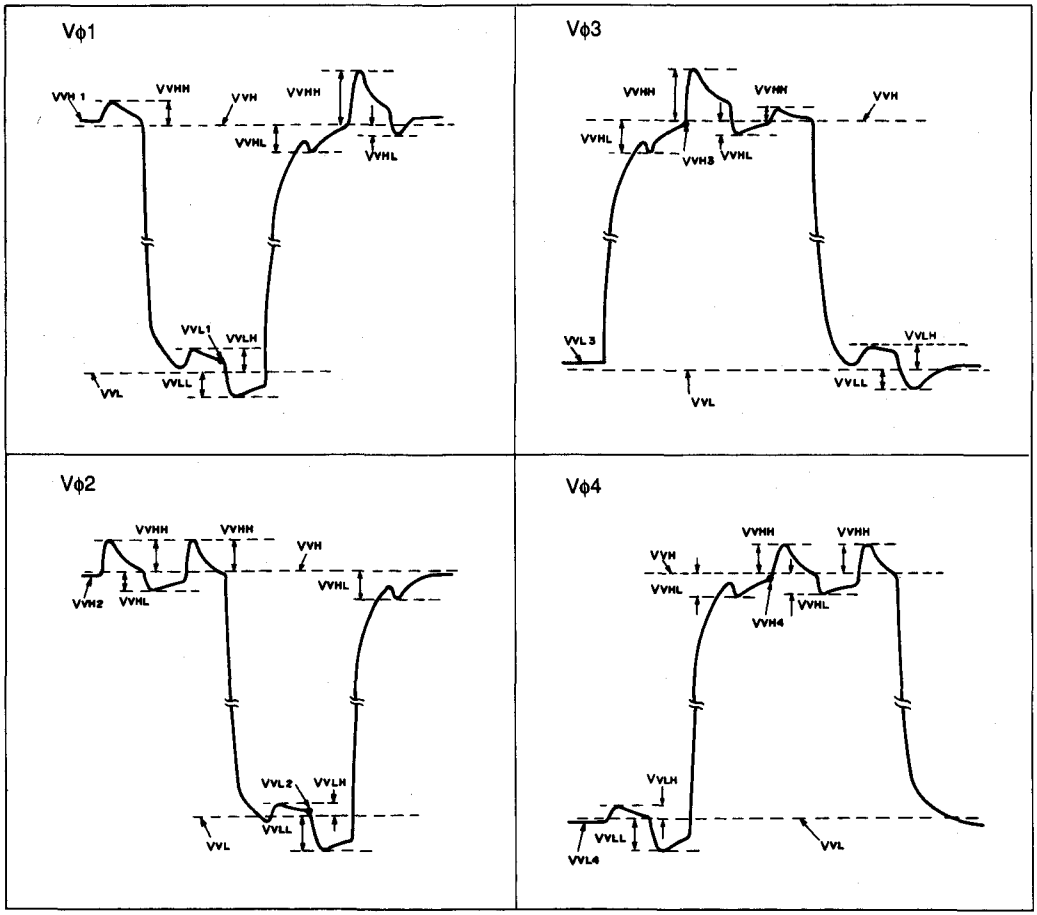
Horizontal trasfer clock equivalent circuit

Drive Clock Waveform Conditions

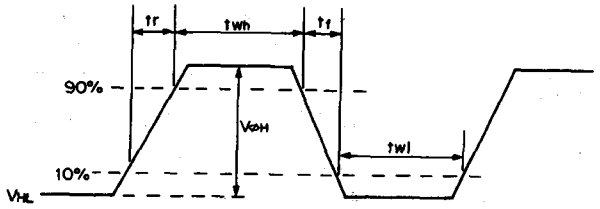
1. Read out clock waveform



2. Vertical transfer clock waveform



3. Horizontal transfer clock waveform



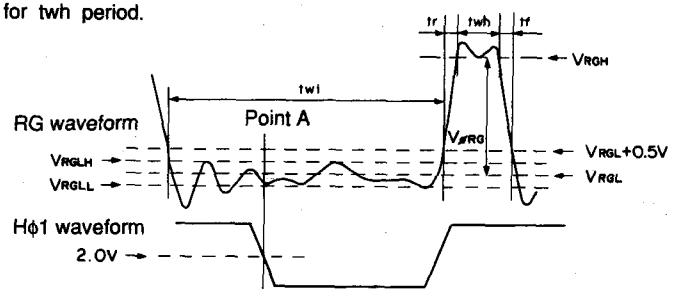
4. Reset gate clock waveform

VRGLH is the maximum value and VRGLL the minimum value of the coupling waveform of the period from Point A, in the diagram above, up to RG rise. VRGL is the mean value for VRGLH and VRGLL.

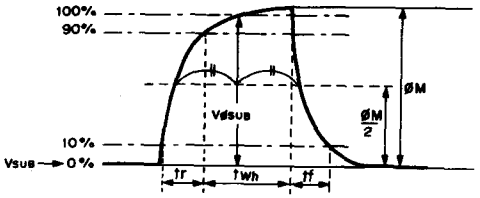
$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$

VRGH is the minimum value for twh period.

$V\phi_{RG} = V_{RGH} - V_{RGL}$



5. Substrate clock waveform



Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	V_T	1.5	1.85							0.5			0.5	µs	During read out
Vertical transfer clock	$V\phi_1, V\phi_2, V\phi_3, V\phi_4$									0.45	0.015		0.25	µs	*1
Horizontal transfer clock	Hφ	35	40		38	40			14	17	8	12	15	ns	During imaging *2
Horizontal transfer clock	Hφ1		5.6					0.014				0.012		µs	During parallel serial conversion.
Horizontal transfer clock	Hφ2					5.6		0.014				0.012		µs	During parallel serial conversion.
Reset gate clock	φRG	14	15		76	80		6.5				4.5		ns	
Substrate clock	φSUB	1.5	2.1							0.5			0.5	µs	During charge drain.

*1) When vertical transfer clock driver CXD1250 is in use. tr and tf are defined as the rising and falling time of 10% to 90% the period between VVL and VVH.

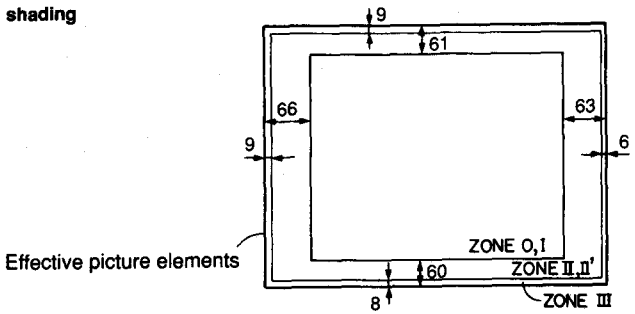
*2) Where, tr-tf is < 4ns, the waveform crosspoint voltage (Vcr) of Hφ1 and Hφ2, is taken as 2.3V<Vcr<2.7V.

Operating Characteristics

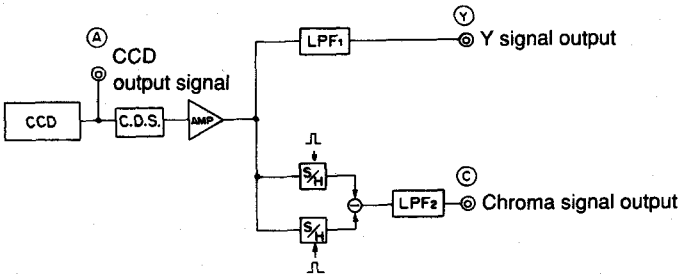
Ta = 25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	240	320		mV	1	
Saturation signal	Ysat	450			mV	2	Ta=60°C
Smear	SM		0.005	0.015	%	3	
Blooming margin		1000			times	4	
Video signal shading	SHy			20	%	5	Zone0, I
				25	%	5	Zone0, I to II, II'
Uniformity between signal channels	ΔSr			10	%	6	
	ΔSb			10	%	6	
Dark signal	Ydt			2	mV	7	Ta=60°C
Dark signal shading	ΔYdt			1	mV	8	Ta=60°C
Flicker Y	Fy			2	%	9	
Flicker R-Y	Fcr			5	%	9	
Flicker B-Y	Fcb			5	%	9	
Horizontal stripes R	Lcr			4	%	10	
Horizontal stripes G	Lcg			4	%	10	
Horizontal stripes B	Lcb			4	%	10	
Horizontal stripes W	Lcw			4	%	10	
Lag	ΔYlag			0.5	%	11	

Zone chart of Video signal shading



Testing System



Note) Adjust AMP amplifier so that total gains between A and Y and between A and C equal 1.

Test Method

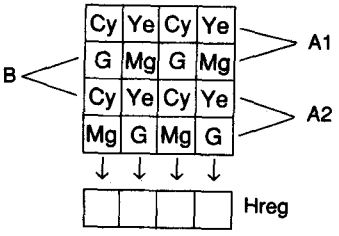
Test conditions

1) Through the following tests the substrate voltage should set to the value displayed on the device, while the device drive conditions should be kept within the range of the bias and clock voltage conditions.

2) Through the following tests defects are excluded, and unless otherwise specified the optical black level (Hence forth referred to as OPB) is set as the reference for the signal output which is taken as the Y signal output or the Chroma signal output of the testing system.

Color coding of CFA (Color Filter Array) & Composition of luminance (Y) and chrominance (C) signals.

CFA of this image sensor is shown in the Figure. This complementary CFA is used with a "field integration mode", where all of the photosites are read out during each video field. Signals from two vertically adjacent photosites, such as line A1 or A2 for field A, are summed when the image charge is transferred into the vertical storage columns. The readout line pairing is shifted down one line for field B. The sensor output signals through the horizontal shift register (H reg.) at line A1 are



Color Coding Diagram

[G+Cy], [Mg+Ye], [G+Cy], [Mg+Ye].

These signals are processed in order to compose Y and C signals. By adding the two adjacent signals at line A1, Y signal is formed as follows:

$$Y = \{(G+Cy) + (Mg+Ye)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

C signal is composed by subtracting the two adjacent signals at line A1.

$$R - Y = \{(Mg+Ye) - (G+Cy)\}$$
$$= \{2R-G\}$$

Next, the signals through H reg. at line A2 are

[Mg+Cy], [G+Ye], [Mg+Cy], [G+Ye]

Similarly, Y and C signals are composed at line A2.

$$Y = \{(G+Ye) + (Mg+Cy)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

$$-(B-Y) = \{(G+Ye) - (Mg+Cy)\}$$
$$= -\{2B-G\}$$

Accordingly, Y signal is balanced in relation to the scanning lines, and C signal takes the form of R–Y and –(B–Y) on alternate lines.
It is the same for B field.

Definition of standard imaging conditions

① Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 cd/m^2 3200K Halogen source), at F5.6 with a typical test lens, and CM-500S (t=1.0 mm) for IR cut filter.

② Standard imaging condition II: Use a light source with uniformity within 2%, color temperature of 3200K and CM-500S (t=1.0 mm) as IR cut filter. The light intensity is adjusted in accordance with the average value of Y signals (Y_A) indicated in each item.

1) Set to standard imaging condition I and measure Y signal (S) at the center of the screen.

2) Set to imaging condition II. Adjust light intensity to 10 times when Y signal output average value Y_A=150mV. Then test Y signal Min. value.

3) Set to imaging condition II. Adjust light intensity to 500 times when Y signal output average value Y_A=150mV. Stop Read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the Max. value Y_{SM} of Y signal output.

$$SM = (Y_{SM}/Y_A) \times {}^1/_{500} \times {}^1/_{10} \times 100\ (\%) \quad ({}^1/_{10}V)$$

4) Set to imaging condition II. Adjust light intensity to 1000 times when Y signal output average value Y_A=150mV. Then check that there is no blooming.

5) Video signal shading SHy
Set to standard imaging condition II. Test Y signal Max. (Y max.) and Min. (Y min.) values. Adjust light intensity to obtain a Y signal output average value (Y_A) of about 150mV.

$$SHy = (Ymax - Ymin)/Y_A \times 100\ (\%)$$

6) Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 150mV. Test the Max. (Cr max. and Cb max.) and Min. (Cr min. and Cb min.) values of C signals from R-Y and B-Y channels.

$$\Delta Sr = |\ (Cr\ max. - Cr\ min.)/Y_A\ | \times 100\ (\%)$$
$$\Delta Sb = |\ (Cb\ max. - Cb\ min.)/Y_A\ | \times 100\ (\%)$$

7) Test the average Y signal voltage when the device ambient temperature is at 60°C and light is obstructed with horizontal idle transfer level as reference.

8) Following 7, test Max. (Yd max.) and Min. (Yd min.) values of Y signal output. Only keep spot defects out of this range.

$$\Delta Ydt = Yd\ max - Yd\ min$$

9) ① Fy

Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 150 mV. Test the Y signal difference (ΔYf) between even field and odd field.

$Fy = (\Delta Yf/Y_A) \times 100$ (%)

② Fcr, Fcb

Set to standard imaging condition II. Insert R and B filter respectively, and test the C signal difference (ΔCr, ΔCb) between even field and odd field and the C signal output average value (C_{Ar}, C_{Ab}). At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

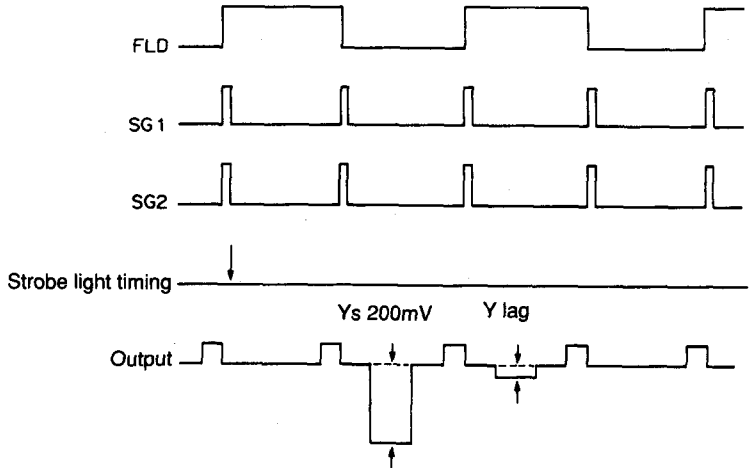
$Fci = (\Delta Ci/C_{Ai}) \times 100$ (%) (i = r, b)

10) Set to standard imaging condition II. Insert W, R, G and B filters respectively, and test the signal difference (ΔYlw, ΔYlr, ΔYlg, ΔYlb) between Y signal lines of the same field. At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

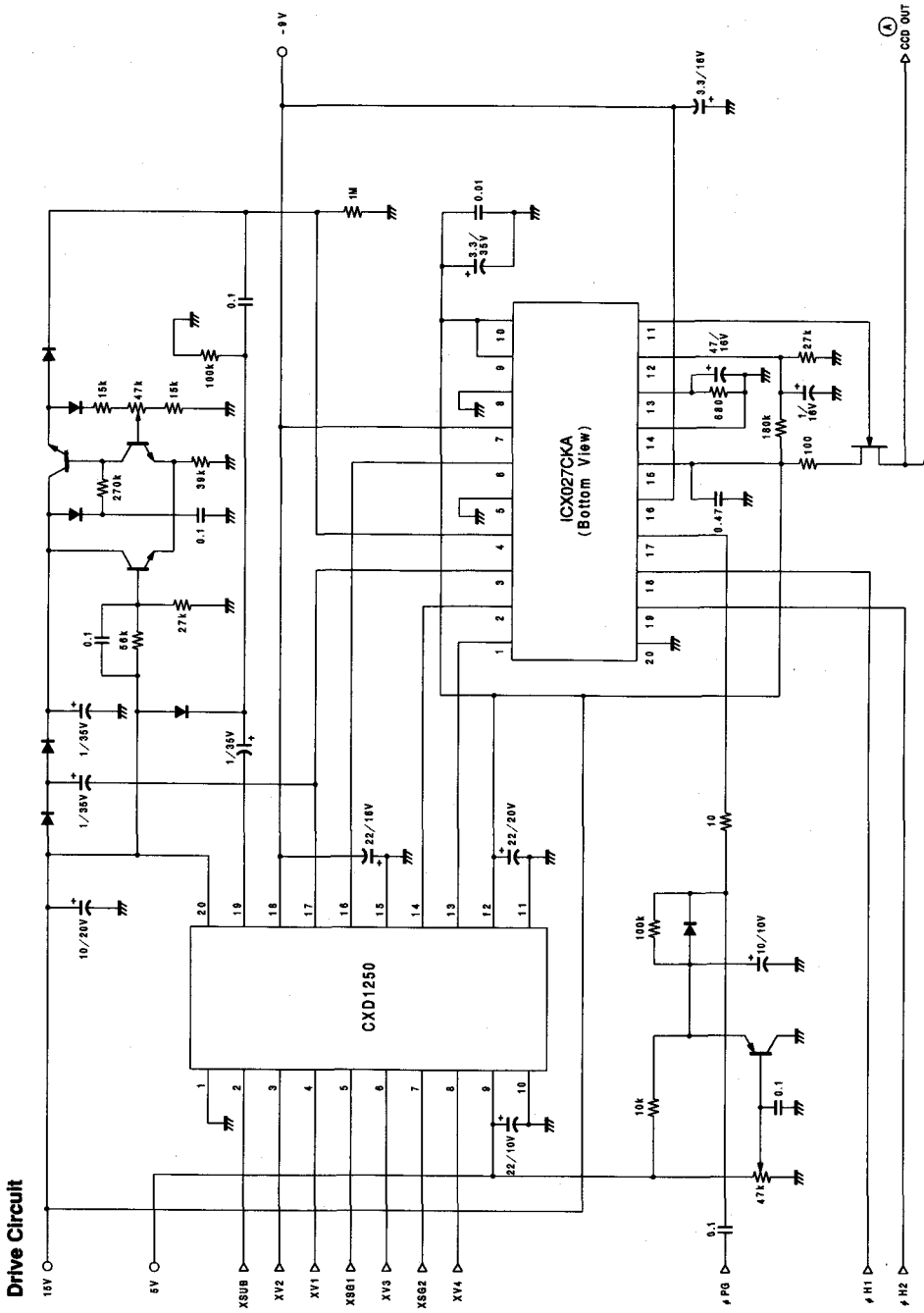
$Lci = (\Delta Yli/Y_A) \times 100$ (%) (i = w, r, g, b)

11) Light a stroboscopic tube with the following timing and test the lag.

$\Delta Ylag = (Ylag/Ys) \times 100$ (%)

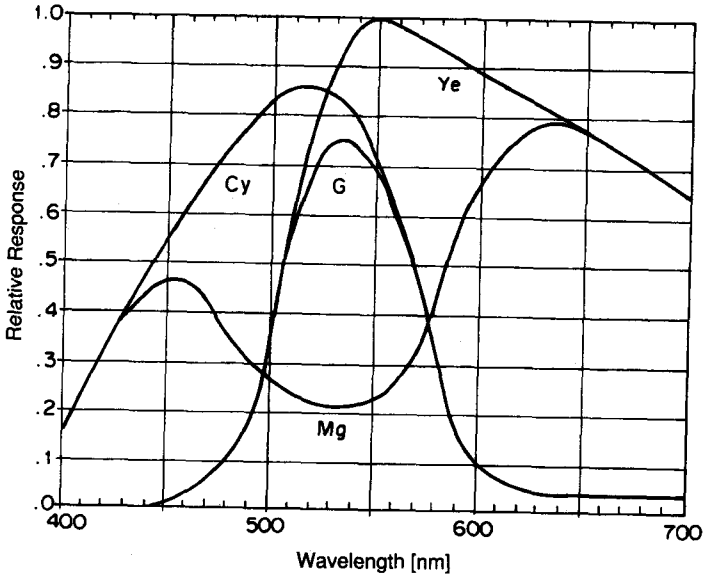


Drive Circuit

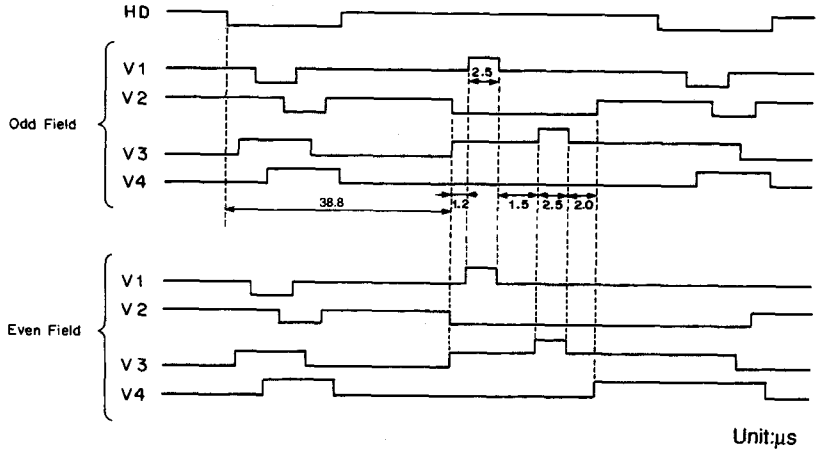


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

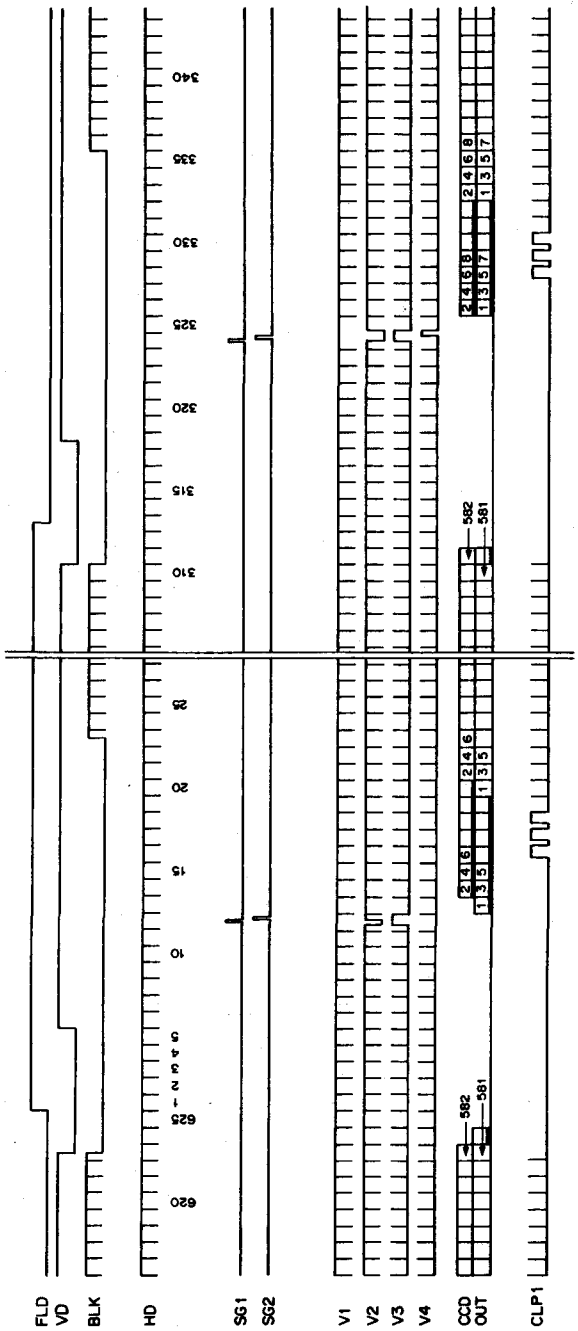
Spectral Sensitivity Characteristics
(Excluding light source characteristics, including lens characteristics)



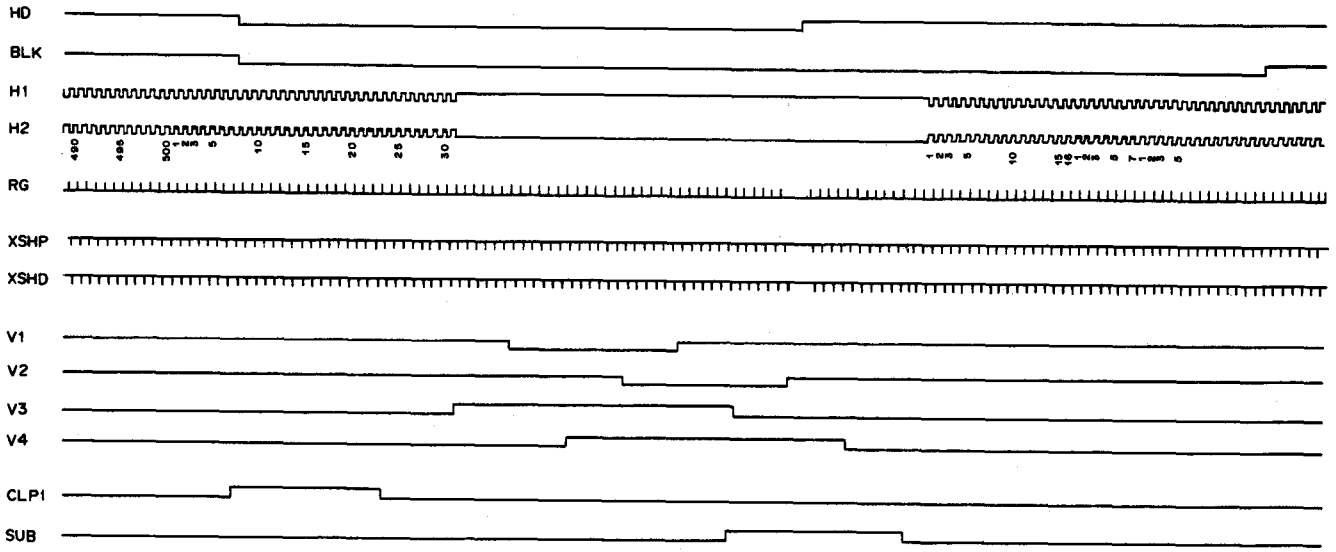
Using read out clock timing chart



Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



(During electronic shutter operation)

Handling Instructions

1) Static charge prevention
CCD image sensor are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount cool sufficiently.
c) To dismount an imaging device do not use a solder pult. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

SONY

ICX044BKA

1/3 Inch CCD Image Sensor for NTSC Color Camera

Description

The ICX044BKA is an interline transfer CCD solid-state image sensor suitable for NTSC 1/3 inch color video cameras. High sensitivity is achieved through the adoption of Ye, Cy, Mg and G complementary color mosaic filters and HAD (Hole-Accumulation Diode) sensors.

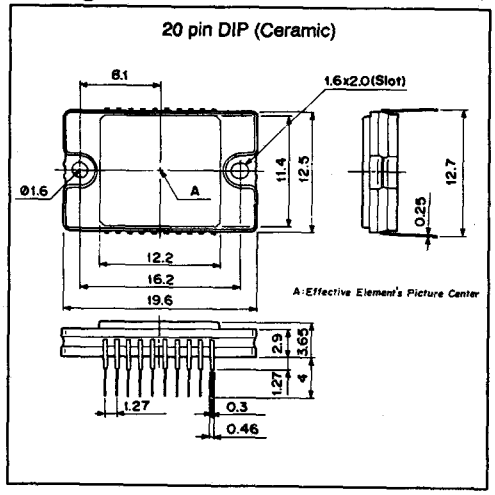
This chip features a field integration read out system and an electronic shutter with variable charge-storage time. 20 pin Cer-DIP package.

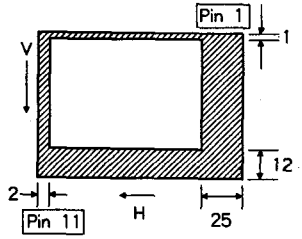
Features

- High sensitivity (+6dB compare with ICX 044AK) and low dark current
- Consecutive various speed shutter
  1/60s (Typ.), 1/100s to 1/10000s
- Low smear
- High antiblooming
- Ye, Cy, Mg, G on chip type complementary color mosaic filter.
- Horizontal register 5V drive
- Reset gate 5V drive

Package Outline

Unit : mm



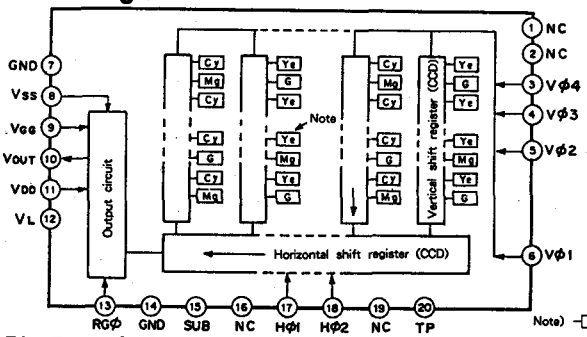


Optical black position (Top View)

Device Structure

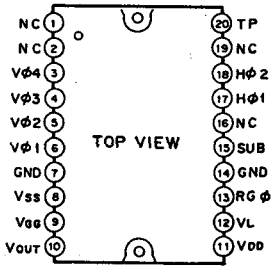
- Optical size 1/3 inch format
- Number of effective pixels
  510 (H) × 492 (V) Approx. 250k pixels
- Number of total pixels
  537 (H) × 505 (V) Approx. 270k pixels
- Interline transfer CCD image sensor
- Chip size 6.3mm (H) × 5.4mm (V)
- Unit cell size 9.6 µm (H) × 7.5 µm (V)
- Optical black Horizontal (H) direction Front 2 pixels Rear 25 pixels
  Vertical (V) direction Front 12 pixels Rear 1 pixels
- Number of dummy bits Horizontal 16
  Vertical 1 (even field only)
- Substrate material silicon

Block Diagram



Pin Configuration

(Top View)



Pin Description

No.	Symbol	Description		No.	Symbol	Description
1	NC		11	V_{DD}	Output amplifier drain supply	
2	NC		12	V_L	Protective transistor bias	
3	V φ 4	Vertical register transfer clock	13	RG φ	Reset gate clock	
4	V φ 3	Vertical register transfer clock	14	GND	GND	
5	V φ 2	Vertical register transfer clock	15	SUB	Substrate (Overflow drain)	
6	V φ 1	Vertical register transfer clock	16	NC		
7	GND	GND	17	H φ 1	Horizontal register transfer clock	
8	Vss	Output amplifier source	18	H φ 2	Horizontal register transfer clock	
9	V_{GG}	Output amplifier gate bias	19	NC		
10	V_{OUT}	Signal output	20	TP	Input bias	

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB-GND		−0.3 to +55	V	
Supply voltage	V_{DD}, V_{OUT}, Vss, TP − GND	−0.3 to +18	V	
	V_{DD}, V_{OUT}, Vss, TP − SUB	−55 to +10	V	
Clock input voltage	V φ 1, V φ 2, V φ 3, V φ 4, H φ 1, H φ 2 − GND	−15 to +20	V	
	V φ 1, V φ 2, V φ 3, V φ 4, H φ 1, H φ 2 − SUB	to +10	V	
Voltage difference between vertical clock input pins		to+15	V	*
Voltage difference between horizontal clock input pins		to+17	V	
H φ 1, H φ 2 − V φ 4		−17 to +17	V	
RG, V_{GG} − GND		−10 to +15	V	
RG, V_{GG} − SUB		−55 to +10	V	
V_L − SUB		−65 to +0.3	V	
Beside GND, SUB-V_L		−0.3 to +30	V	
Storage temperature		−30 to +80	℃	
Operating temperature		−10 to +60	℃	

* +27V (Max.) when clock width<10 μs, duty factor<0.1%.

Bias Conditions

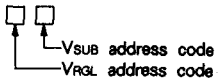
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD}	14.55	15.0	15.45	V	
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	Vss	Ground through 680 Ω resistor				± 5%
Substrate voltage adjustment range	V_{SUB}	9.0		18.5	V	*1
Fluctuation range after substrate voltage adjustment	Δ V_{SUB}	–3		+3	%	
Reset gate clock voltage adjustment range	V_{RGL}	1.0		4.0	V	*1
Fluctuation range after reset gate clock voltage adjustment	Δ V_{RGL}	–3		+3	%	
Protective transistor bias	V_L	*2				
Input bias	TP	14.55	15.0	15.45	V	

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		3		mA	
Input current	I_{IN1}			1	μA	*3
Input current	I_{IN2}			10	μA	*4

*** 1)** Substrate voltage (V_{SUB}) • reset gate clock voltage (V_{RGL}) setting value display.
Setting values of substrate voltage and reset gate clock voltage are displayed at the back of the device through a code address. Adjust substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) to the displayed voltage. Fluctuation range after adjustment is ± 3%.

V_{SUB} code address–1 digit display
V_{RGL} code address–1 digit display



Code addresses and actual numerical values correspond to each other as follows.

V_{RGL} address code	1	2	3	4	5	6	7
Numerical value	1.0	1.5	2.0	2.5	3.0	3.5	4.0

V_{SUB} address code	E	f	G	h	J	K	L	m	N	P	Q	R	S	T	U	V	W	X	Y	Z
Numerical value	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5

<Example> "5L" → V_{RGL}=3.0V
V_{SUB}=12.0V

*** 2)** V_L setting is the V_{VL} voltage of the vertical transfer clock waveform.

* 3) 1. Current to each pin when 18V is applied to V_{DD}, V_{OUT}, Vss, SUB, TP pins, while pins that are not tested are grounded.
2. Current to each pins when 20V is applied sequentially to $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $H\phi_1$ and $H\phi_2$, while pins that are not tested are grounded. However, 20V is applied to SUB.
3. Current to each pins when 15V is applied sequentially to pins RG and V_{GG}, while pins that are not tested are grounded. However, 15V is applied to SUB.
4. Current to V_L pin when it is grounded, while 30V is applied to all pins except pins that are not tested. However, GND and SUB pins are kept open.

* 4) Current to SUB pin when 55V is applied to SUB pin, while pins that are not tested are grounded.

Clock Voltage Conditions

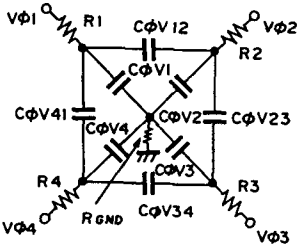
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Read out clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2} V_{VH3}, V_{VH4}	− 0.2	0	0.1	V	2	V_{VH}= (V_{VH1}+V_{VH2}) /2
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	− 9.6	− 9.0	− 8.5	V	2	V_{VL}= (V_{VL3}+V_{VL4}) /2
	$V\phi_V$	8.3	9.0	9.7	V	2	$V\phi_V$=V_{VHn} − V_{VLn} (n=1 to 4)
	|V_{VH1} − V_{VH2}|			0.1	V	2	
	V_{VH3} − V_{VH}	− 0.25		0.1	V	2	
	V_{VH4} − V_{VH}	− 0.25		0.1	V	2	
	V_{VHH}			0.5	V	2	High level coupling
	V_{VHL}			0.5	V	2	High level coupling
	V_{VLH}			0.5	V	2	Low level coupling
	V_{VLL}			0.5	V	2	Low level coupling
Horizontal transfer clock voltage	$V\phi_H$	4.75	5.0	5.25	V	3	
	V_{HL}	− 0.05	0	0.05	V	3	
Reset gate clock voltage	$V\phi_{RG}$	4.5	5.0	5.5	V	4	*
	V_{RGLH} − V_{RGLL}			0.8	V	4	Low level coupling
Substrate clock voltage	$V\phi_{SUB}$	23.0	24.0	25.0	V	5	

* No adjustment of reset gate clock voltage is necessary when reset gate clock is driven as indicated below. In this case, reset gate clock voltage set point displayed on back of image sensor has no meaning.

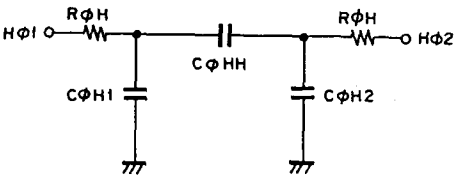
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Reset gate clock voltage	V_{RGL}	− 0.1	0	0.1	V	4	
	$V\phi_{RG}$	8.5	9.0	9.5	V	4	

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi_{V1}$, $C\phi_{V3}$		820		pF	
	$C\phi_{V2}$, $C\phi_{V4}$		1000		pF	
Capacitance between vertical transfer clocks	$C\phi_{V12}$, $C\phi_{V34}$		680		pF	
	$C\phi_{V23}$, $C\phi_{V41}$		470		pF	
Capacitance between horizontal transfer clock and GND	$C\phi_{H1}$, $C\phi_{H2}$		40		pF	
Capacitance between horizontal transfer clocks	$C\phi_{HH}$		40		pF	
Capacitance between reset gate clock and GND	$C\phi_{RG}$		5		pF	
Capacitance between substrate clock and GND	$C\phi_{SUB}$		270		pF	
Vertical transfer clock serial resistor	R_1, R_2, R_3, R_4		80		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock serial resistor	$R\phi_H$		20		Ω	



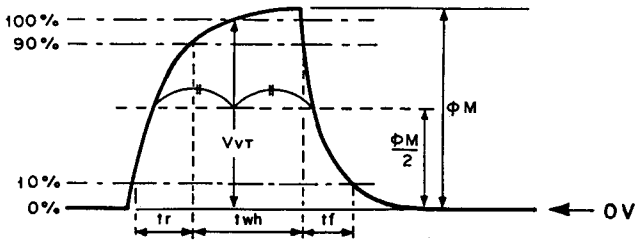
Vertical transfer clock equivalent circuit



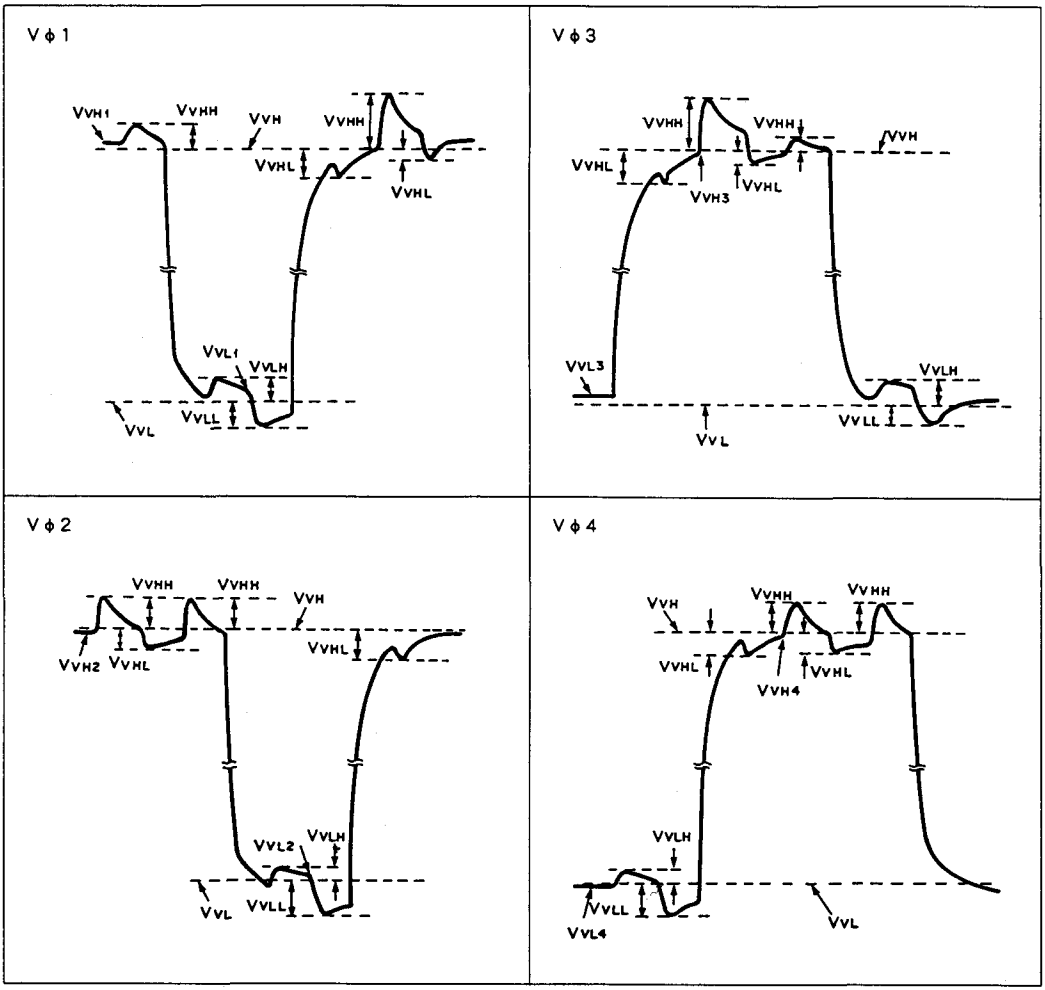
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

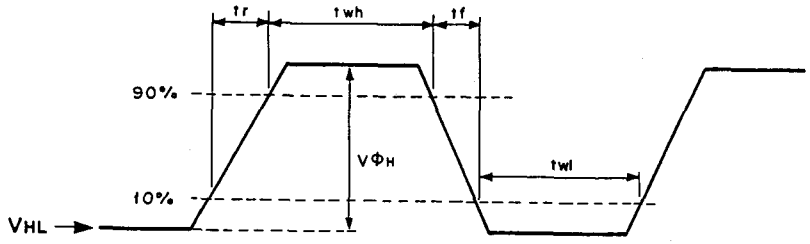
(1) Read out clock waveform



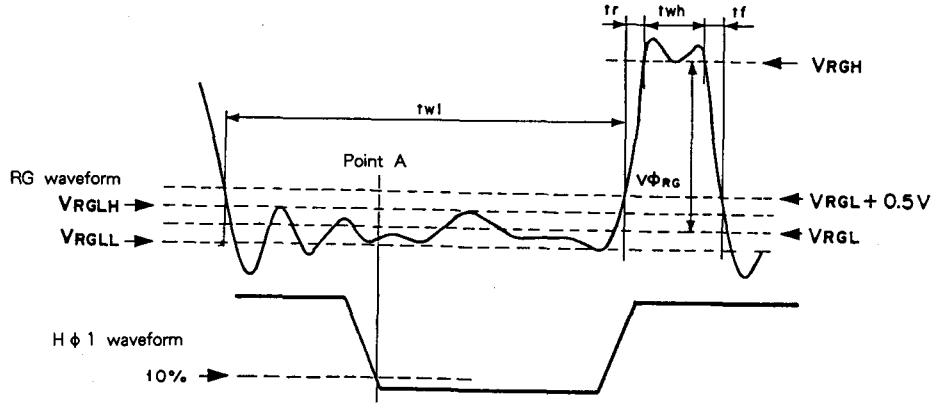
(2) Vertical transfer clock waveform



(3) Horizontal transfer clock waveform diagram



(4) Reset gate clock waveform diagram



VRGLH is the maximum value and VRGLL the minimum value of the coupling waveform in the period from Point A in the diagram above to RG rise.

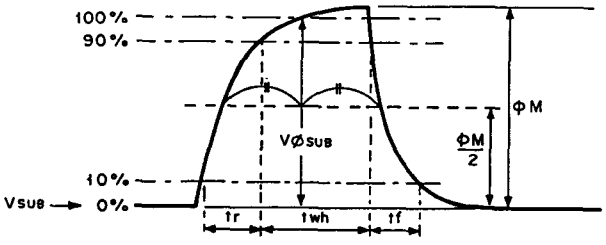
VRGL is the mean value for VRGLH and VRGLL.

$$V_{RGL} = (V_{RGLH} + V_{RGLL}) / 2$$

VRGH is the minimum value for twh period.

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

(5) Substrate clock waveform



Clock Switching Characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	V_T	2.3	2.5						0.5			0.5		µs	During read out
Vertical transfer clock	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$										0.015		0.25	µs	*1
Horizontal transfer clock	$H\phi$	37	41		38	42			12	15	*2	1.0	15	ns	During imaging
Horizontal transfer clock	$H\phi_1$		5.6						0.012			0.012		µs	During parallel serial conversion.
Horizontal transfer clock	$H\phi_2$					5.6			0.012			0.012		µs	
Reset gate clock	ϕ_{RG}	11	15		75	79			6.5			4.5		ns	
Substrate clock	ϕ_{SUB}	1.5	2.0							0.5			0.5	µs	During charge drain.

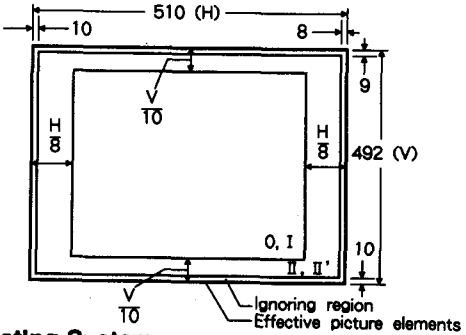
* 1) When vertical transfer clock driver CXD1250 is in use.
* 2) tf ≧ tr–2 ns

Image Sensor Characteristics

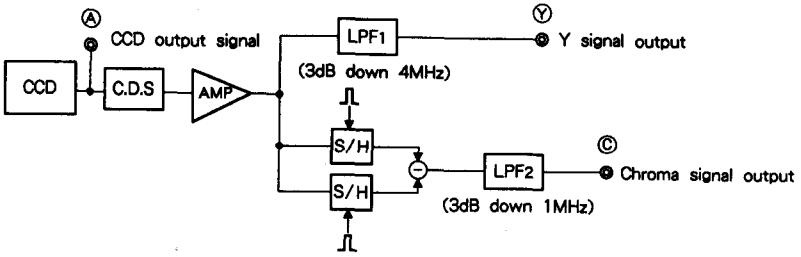
(Ta=25℃)

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	400	480		mV	1	
Saturation signal	Ysat	600			mV	2	Ta=60℃
Smear	Sm		0.007	0.012	%	3	
Video signal shading	SHy			20	%	4	Zone 0, I
				25	%	4	Zone 0 to II'
Uniformity between signal channels	Δ Sr			10	%	5	
	Δ Sb			10	%	5	
Dark signal	Ydt			2	mV	6	Ta=60℃
Dark signal shading	Δ Ydt			1	mV	7	Ta=60℃
Flicker Y	Fy			2	%	8	
Flicker R − Y	Fcr			5	%	8	
Flicker B − Y	Fcb			5	%	8	
Horizontal stripes R	Lcr			3.5	%	9	
Horizontal stripes G	Lcg			3.5	%	9	
Horizontal stripes B	Lcb			3.5	%	9	
Horizontal stripes W	Lcw			3.5	%	9	
Lag	Lag			0.5	%	10	

Zone Chart of Video Signal Shading



Testing System



Note) Adjust AMP gain so that total gains between Ⓐ and Ⓨ and between Ⓐ and Ⓒ equal 1.

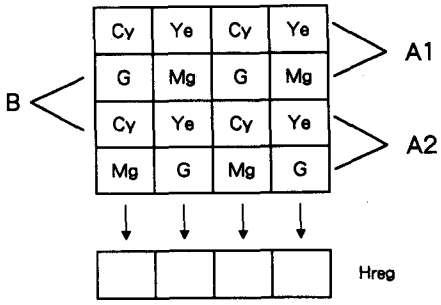
Image Sensor Characteristics Test Method

◎ Test conditions

① Through the following tests the substrate voltage and reset gate clock voltage are set to the value displayed on the device, while the device drive conditions are at the typical value of the bias and clock voltage conditions.

② Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OB) is set as the reference for the signal output which is taken as the Y signal output or the chroma signal output of the testing system.

◎ Color coding of CFA (Color Filter Array) & Composition of luminance (Y) and chrominance (C) signals



Color Coding Diagram

CFA of this image sensor is shown in the Figure. This complementary CFA is used with a "field integration mode", where all of the photosites are read out during each video field. Signals from two vertically adjacent photosites, such as line A1 or A2 for field A, are summed when the image charge is transferred into the vertical storage columns.
The read out line pairing is shifted down one line for field B. The sensor output signals through the horizontal register (H reg.) at line A1 are [G+Cy], [Mg+Ye], [G+Cy], [Mg+Ye].

These signals are processed in order to compose Y and C signals. By adding the two adjacent signals at line A1, Y signal is formed as follows:

$$Y = \{ (G+Cy) + (Mg+Ye) \} \times 1/2$$
$$= 1/2 \{ 2B+3G+2R \}$$

C signal is composed by subtracting the two adjacent signals at line A1.

$$R - Y = \{ (Mg+Ye) - (G+Cy) \}$$
$$= \{ 2R - G \}$$

Next, the signals through H reg. at line A2 are

[Mg+Cy], [G+Ye], [Mg+Cy], [G+Ye]

Similarly, Y and C signals are composed at line A2.

$$Y = \{ (G+Ye) + (Mg+Cy) \} \times 1/2$$
$$= 1/2 \{ 2B+3G+2R \}$$
$$-(B - Y) = \{ (G+Ye) - (Mg+Cy) \}$$
$$= -\{ 2B - G \}$$

Accordingly, Y signal is balanced in relation to the scanning lines, and C signal takes the form of R − Y and − (B − Y) on alternate lines.
It is the same for B field.

◎ Definition of standard imaging conditions

① Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 cd/m^2, color temperature 3200K Halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t=1.0mm) as IR cut filter and image at F5.6.

② Standard imaging condition II: Image a light source (color temperature of 3200K) which uniformity of brightness is within 2% at all angles. Use a testing standard lens with CM500S (t=1.0mm) as IR cut filter. The light intensity is adjusted to the value indicated in each testing item by lens diaphragm.

1. Sensitivity
   Set to standard image condition I. After selecting the electronic shutter mode at a 1/250s. shutter speed, measure the Y signal (Ys) at the center of the screen and substitute in the following formula.

   $$S = Ys \times \frac{250}{60}$$

2. Saturation signal
   Set to standard imaging condition II. Adjust light intensity to 10 times that of Y signal output average value (Y_A=180mV), then test Y signal minimum value.

3. Smear
   Set to standard imaging condition II. Adjust light intensity to 500 times that of Y signal output average value (Y_A=180mV). Stop read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the maximum value YSm of Y signal output.

   $$Sm = \frac{YSm}{Y_A} \times \frac{1}{500} \times \frac{1}{10} \times 100\ (\%)\ (1/10V)$$

4. Video signal shading
   Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A=180mV) with lens diaphragm at F5.6 to F8. Then test maximum (Ymax) and minimum (Ymin) values of Y signal.

   $$SHy = (Ymax - Ymin) / Y_A \times 100\ (\%)$$

5. Video signal between channels uniformity
   Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A=180mV). Then test maximum (Crmax, Cbmax) and minimum (Crmin, Cbmin) values of chroma signals from R − Y and B − Y channels.

   $$\Delta Sr = |(Crmax - Crmin) / Y_A| \times 100\ (\%)$$
   $$\Delta Sb = |(Cbmax - Cbmin) / Y_A| \times 100\ (\%)$$

6. Dark signal
   Test Y signal output average value Ydt when the device ambient temperature is at 60 °C and light is obstructed with horizontal idle transfer level as reference.

7. Dark signal shading
   Following 6, test maximum (Ydmax) and minimum (Ydmin) values of dark signal output.

   $$\Delta Ydt = Ydmax - Ydmin$$

8. Flicker

① Fy

Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A=180mV). Then test the Y signal difference (Δ Yf) between even field and odd field.

$$Fy = (\Delta Yf / Y_A) \times 100\ (\%)$$

② Fcr, Fcb

Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A=180mV). Then insert R or B filter, and test the C signal difference (Δ Cr, Δ Cb) between even field and odd field and the C signal output average value (CAr, CAb).

$$Fci = (\Delta Ci / CAi) \times 100\ (\%)\ \ (i=r, b)$$

9. Lateral stripe

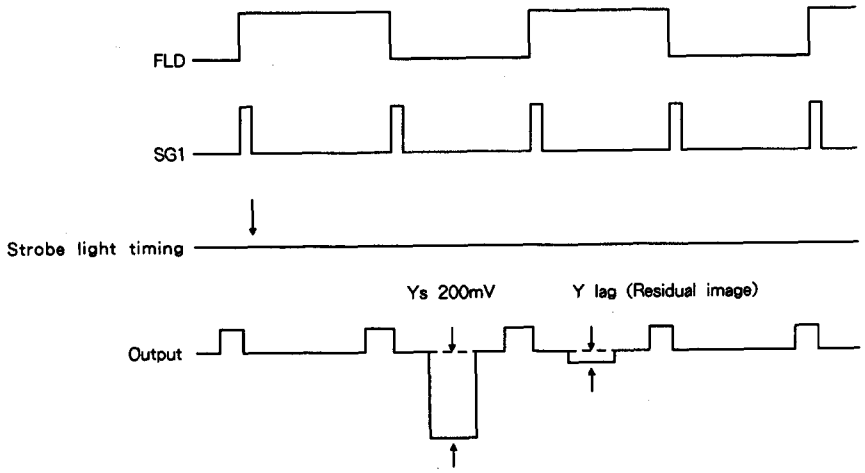
Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A=180mV). Then insert R, G and B filters respectively, and test the signal difference (Δ Yiw, Δ Yir, Δ Yig, Δ Yib) between Y signal lines of the same field.

$$Lci = (\Delta Yli / Y_A) \times 100\ (\%)\ \ (i=w, r, g, b)$$

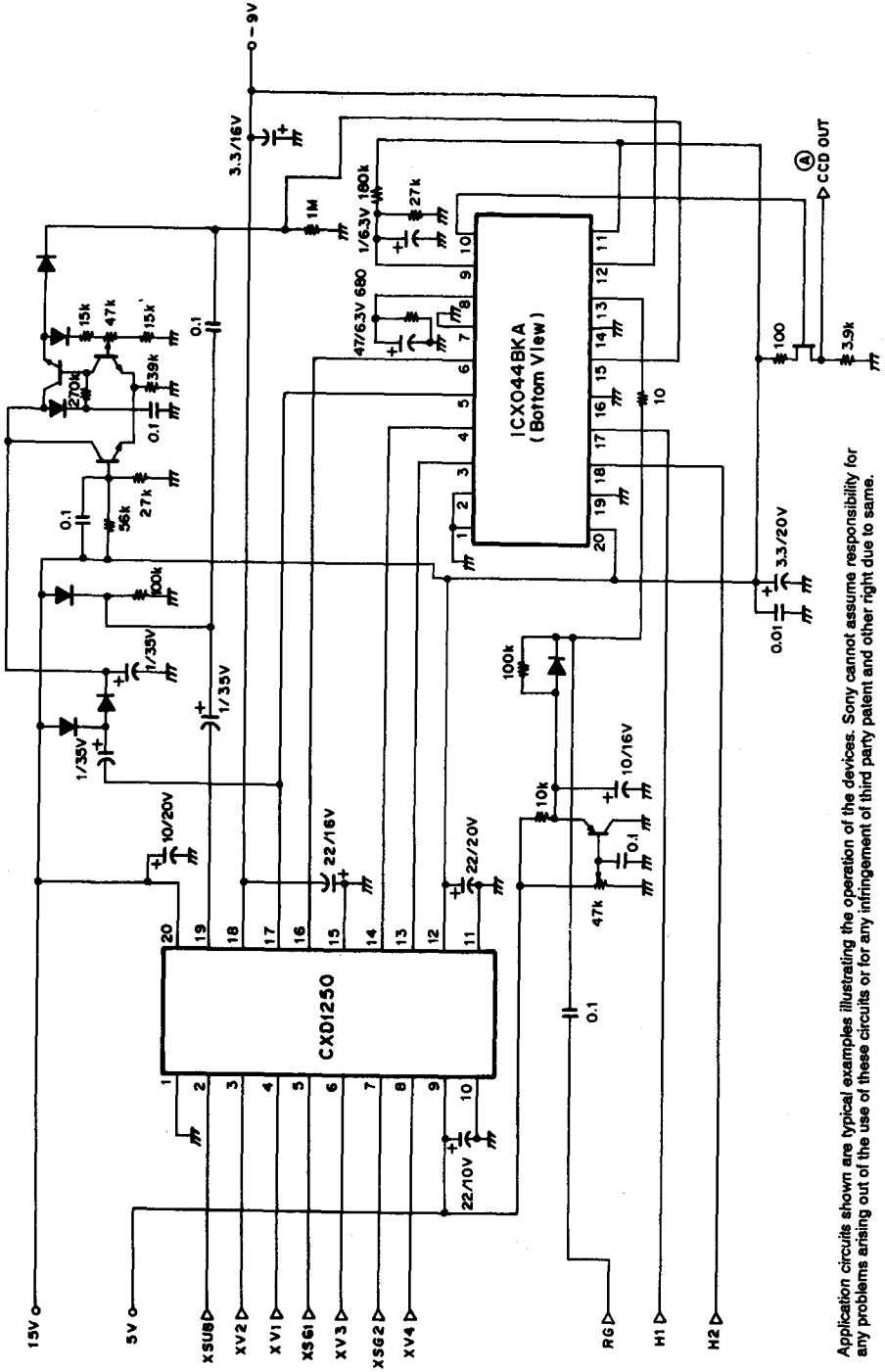
10. Residual image

Adjust Y signal output value (Ys) by strobe light to 200mV. Then light a stroboscopic tube with the following timing and test the residual image (Ylag).

$$Lag = (Ylag / Ys) \times 100\ (\%)$$



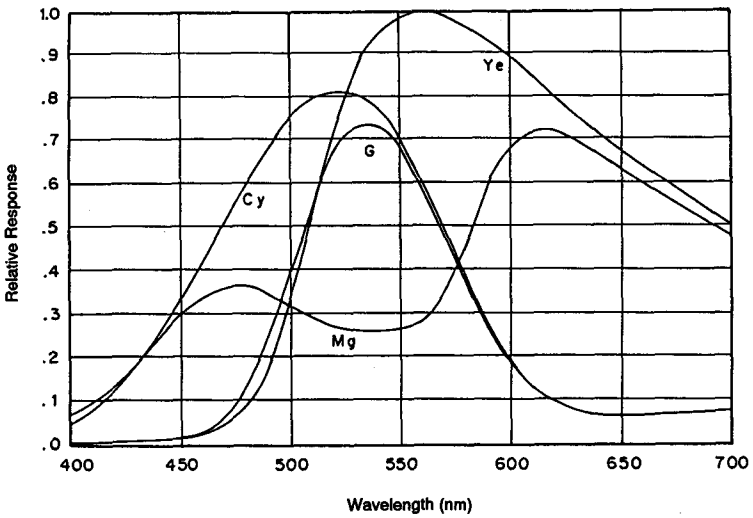
Drive Circuit



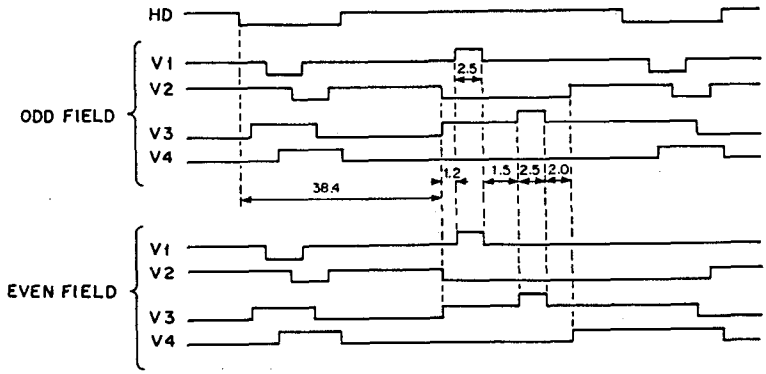
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Spectral Sensitivity Characteristics

(Excluding light source characteristics, including lens characteristics)

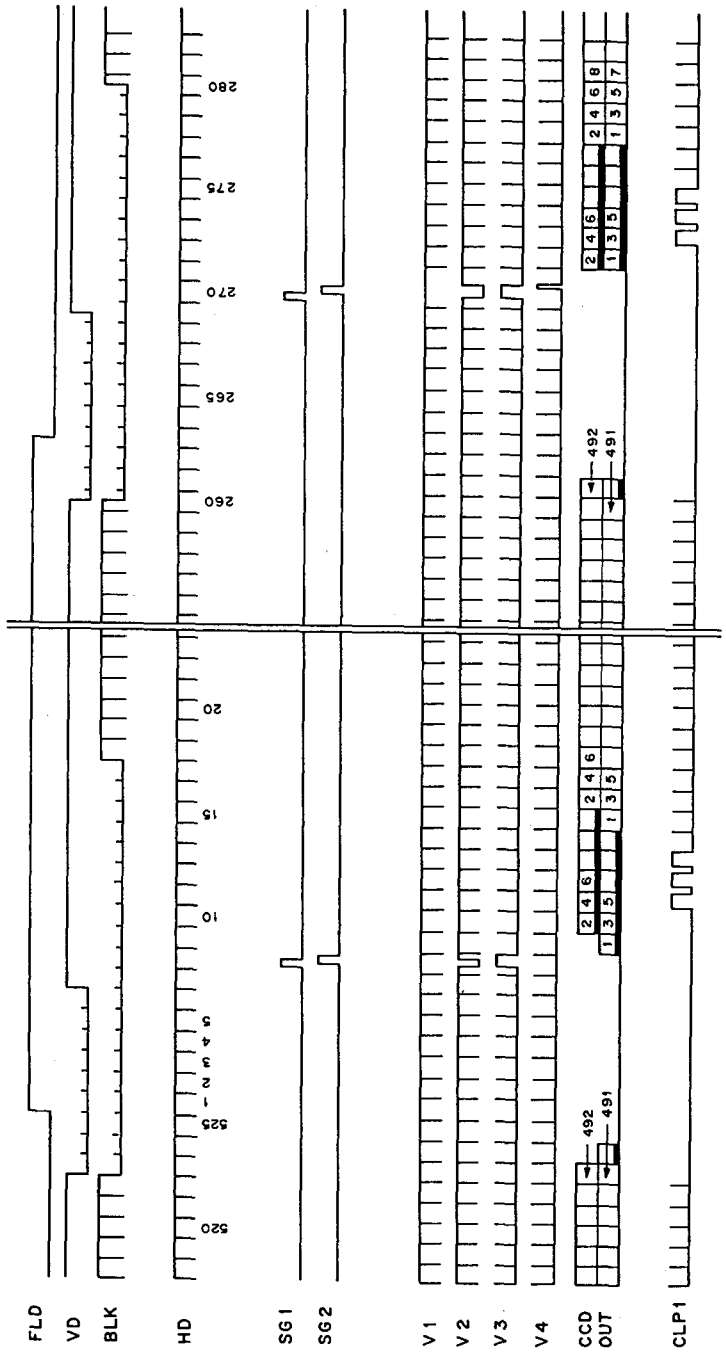


Sensor Read Out Clock Timing Chart

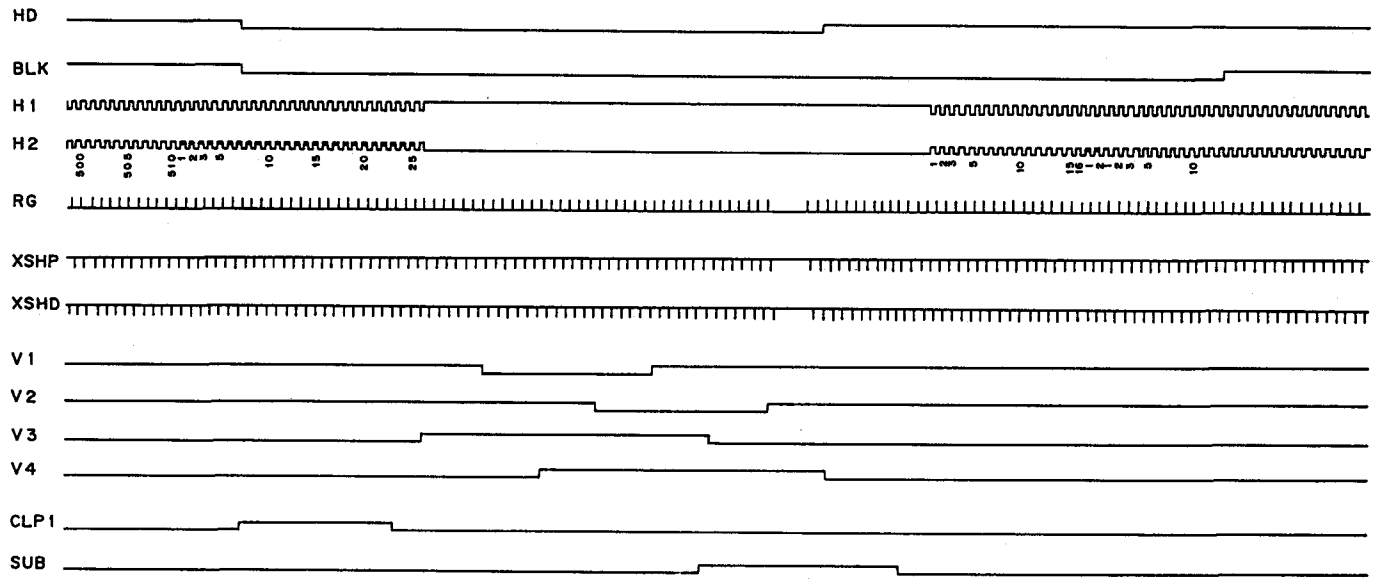


Unit : µs

Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



(During electronic shutter operation)

Handling Instructions

1) Static charge prevention
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensor.
   e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
   a) Make sure the package temperature does not exceed 80 °C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an imaging device do not use a solder suction equipment. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
   a) Operate in clean environments (around class 1000 will be appropriate).
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

SONY

ICX045BKA

1/3 inch CCD Image Sensor for PAL Color Camera

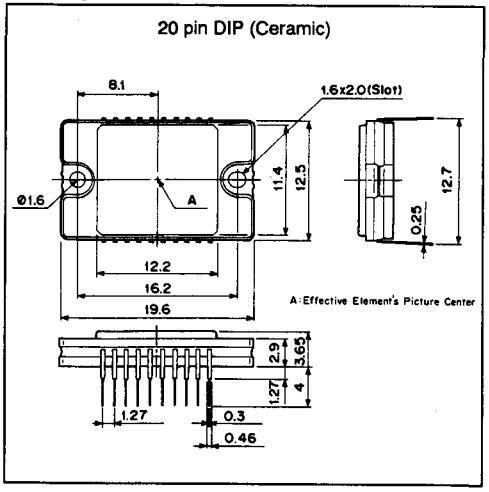
Description

The ICX045BKA is an interline transfer CCD solid-state image sensor suitable for PAL 1/3 inch color video cameras. High sensitivity is achieved through the adoption of Ye, Cy, Mg and G complementary color mosaic filters and HAD (Hole-Accumulation Diode) sensors.

This chip features a field integration read out system and an electronic shutter with variable charge-storage time. 20 pin Cer-DIP package.

Package Outline

Unit : mm

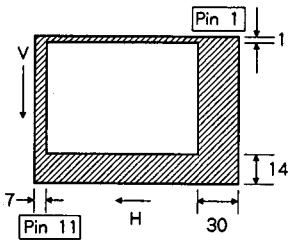


Features

- High sensitivity (+6dB compare with ICX045AK) and low dark current
- Consecutive various speed shutter 1/50s. (Typ.), 1/100s to 1/10000s
- Low smear
- High antiblooming
- Ye, Cy, Mg, G on chip type complementary color mosaic filter.
- Horizontal register 5V drive
- Reset gate 5V drive

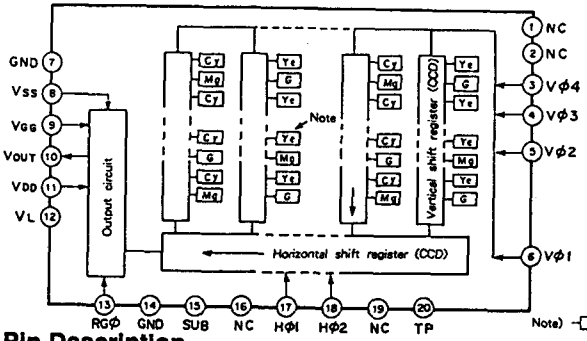
Device Structure

- Optical size 1/3 inch format
- Number of effective pixels
  500 (H) × 582 (V) Approx. 290k pixels
- Number of total pixels
  537 (H) × 597 (V) Approx. 320k pixels
- Interline transfer CCD image sensor
- Chip size 6.3mm (H) × 5.4mm (V)
- Unit cell size 9.8 μm (H) × 6.3 μm (V)
- Optical black Horizontal (H) direction Front 7 pixels Rear 30 pixels
  Vertical (V) direction Front 14 pixels Rear 1 pixels
- Number of dummy bits Horizontal 16
  Vertical 1 (even field only)
- Substrate material silicon



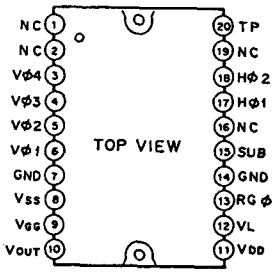
Optical black position (Top View)

Block Diagram



Pin Configuration

(Top View)



Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	NC		11	V_{DD}	Output amplifier drain supply
2	NC		12	V_L	Protective transistor bias
3	V φ 4	Vertical register transfer clock	13	RG φ	Reset gate clock
4	V φ 3	Vertical register transfer clock	14	GND	GND
5	V φ 2	Vertical register transfer clock	15	SUB	Substrate (Overflow drain)
6	V φ 1	Vertical register transfer clock	16	NC	
7	GND	GND	17	H φ 1	Horizontal register transfer clock
8	Vss	Output amplifier source	18	H φ 2	Horizontal register transfer clock
9	V_{GG}	Output amplifier gate bias	19	NC	
10	V_{OUT}	Signal output	20	TP	Input bias

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB-GND		−0.3 to +55	V	
Supply voltage	V_{DD}, V_{OUT}, Vss, TP − GND	−0.3 to +18	V	
	V_{DD}, V_{OUT}, Vss, TP − SUB	−55 to +10	V	
Clock input voltage	V φ 1, V φ 2, V φ 3, V φ 4, H φ 1, H φ 2 − GND	−15 to +20	V	
	V φ 1, V φ 2, V φ 3, V φ 4, H φ 1, H φ 2 − SUB	to +10	V	
Voltage difference between vertical clock input pins		to+15	V	*
Voltage difference between horizontal clock input pins		to+17	V	
H φ 1, H φ 2 − V φ 4		−17 to +17	V	
RG, V_{GG} − GND		−10 to +15	V	
RG, V_{GG} − SUB		−55 to +10	V	
V_L − SUB		−65 to +0.3	V	
Beside GND, SUB-V_L		−0.3 to +30	V	
Storage temperature		−30 to +80	℃	
Operating temperature		−10 to +60	℃	

* +27V (Max.) when clock width<10 μs, duty factor<0.1%.

Bias Conditions

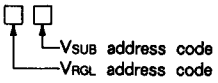
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD}	14.55	15.0	15.45	V	
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	Vss	Ground through 680 Ω resistor				± 5%
Substrate voltage adjustment range	V_{SUB}	9.0		18.5	V	*1
Fluctuation range after substrate voltage adjustment	Δ V_{SUB}	–3		+3	%	
Reset gate clock voltage adjustment range	V_{RGL}	1.0		4.0	V	*1
Fluctuation range after reset gate clock voltage adjustment	Δ V_{RGL}	–3		+3	%	
Protective transistor bias	V_L	*2				
Input bias	TP	14.55	15.0	15.45	V	

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		3		mA	
Input current	I_{IN1}			1	μA	*3
Input current	I_{IN2}			10	μA	*4

*** 1)** Substrate voltage (V_{SUB}) • reset gate clock voltage (V_{RGL}) setting value display.
Setting values of substrate voltage and reset gate clock voltage are displayed at the back of the device through a code address. Adjust substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) to the displayed voltage. Fluctuation range after adjustment is ± 3%.

V_{SUB} code address–1 digit display
V_{RGL} code address–1 digit display



Code addresses and actual numerical values correspond to each other as follows.

V_{RGL} address code	1	2	3	4	5	6	7
Numerical value	1.0	1.5	2.0	2.5	3.0	3.5	4.0

V_{SUB} address code	E	f	G	h	J	K	L	m	N	P	Q	R	S	T	U	V	W	X	Y	Z
Numerical value	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5

<Example> "5L" → V_{RGL}=3.0V
V_{SUB}=12.0V

*** 2)** V_L setting is the V_{VL} voltage of the vertical transfer clock waveform.

* 3) 1. Current to each pin when 18V is applied to V_{DD}, V_{OUT}, Vss, SUB, TP pins, while pins that are not tested are grounded.
2. Current to each pins when 20V is applied sequentially to V ϕ 1, V ϕ 2, V ϕ 3, V ϕ 4, H ϕ 1 and H ϕ 2, while pins that are not tested are grounded. However, 20V is applied to SUB.
3. Current to each pins when 15V is applied sequentially to pins RG and V_{GG}, while pins that are not tested are grounded. However, 15V is applied to SUB.
4. Current to V_L pin when it is grounded, while 30V is applied to all pins except pins that are not tested. However, GND and SUB pins are kept open.

* 4) Current to SUB pin when 55V is applied to SUB pin, while pins that are not tested are grounded.

Clock Voltage Conditions

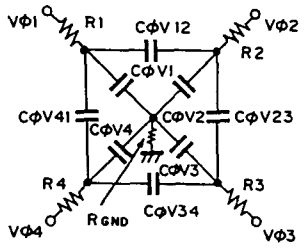
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Read out clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2} V_{VH3}, V_{VH4}	− 0.2	0	0.1	V	2	V_{VH}= (V_{VH1}+V_{VH2}) /2
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	− 9.6	− 9.0	− 8.5	V	2	V_{VL}= (V_{VL3}+V_{VL4}) /2
	V ϕ v	8.3	9.0	9.7	V	2	V ϕ v=V_{VHn} − V_{VLn} (n=1 to 4)
	|V_{VH1} − V_{VH2}|			0.1	V	2	
	V_{VH3} − V_{VH}	− 0.25		0.1	V	2	
	V_{VH4} − V_{VH}	− 0.25		0.1	V	2	
	V_{VHH}			0.5	V	2	High level coupling
	V_{VHL}			0.5	V	2	High level coupling
	V_{VLH}			0.5	V	2	Low level coupling
	V_{VLL}			0.5	V	2	Low level coupling
Horizontal transfer clock voltage	V ϕ H	4.75	5.0	5.25	V	3	
	V_{HL}	− 0.05	0	0.05	V	3	
Reset gate clock voltage	V ϕ RG	4.5	5.0	5.5	V	4	*
	V_{RGLH} − V_{RGLL}			0.8	V	4	Low level coupling
Substrate clock voltage	V ϕ SUB	23.0	24.0	25.0	V	5	

* No adjustment of reset gate clock voltage is necessary when reset gate clock is driven as indicated below. In this case, reset gate clock voltage set point displayed on back of image sensor has no meaning.

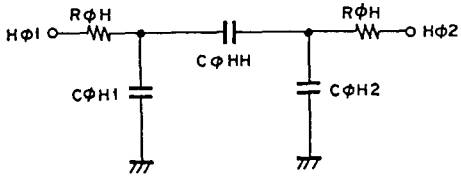
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Reset gate clock voltage	V_{RGL}	− 0.1	0	0.1	V	4	
	V ϕ RG	8.5	9.0	9.5	V	4	

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi_{V1}$, $C\phi_{V3}$		820		pF	
	$C\phi_{V2}$, $C\phi_{V4}$		1000		pF	
Capacitance between vertical transfer clocks	$C\phi_{V12}$, $C\phi_{V34}$		680		pF	
	$C\phi_{V23}$, $C\phi_{V41}$		470		pF	
Capacitance between horizontal transfer clock and GND	$C\phi_{H1}$, $C\phi_{H2}$		40		pF	
Capacitance between horizontal transfer clocks	$C\phi_{HH}$		40		pF	
Capacitance between reset gate clock and GND	$C\phi_{RG}$		5		pF	
Capacitance between substrate clock and GND	$C\phi_{SUB}$		270		pF	
Vertical transfer clock serial resistor	R_1, R_2, R_3, R_4		80		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock serial resistor	$R\phi_H$		20		Ω	



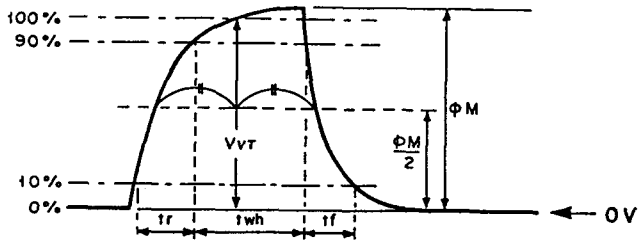
Vertical transfer clock equivalent circuit



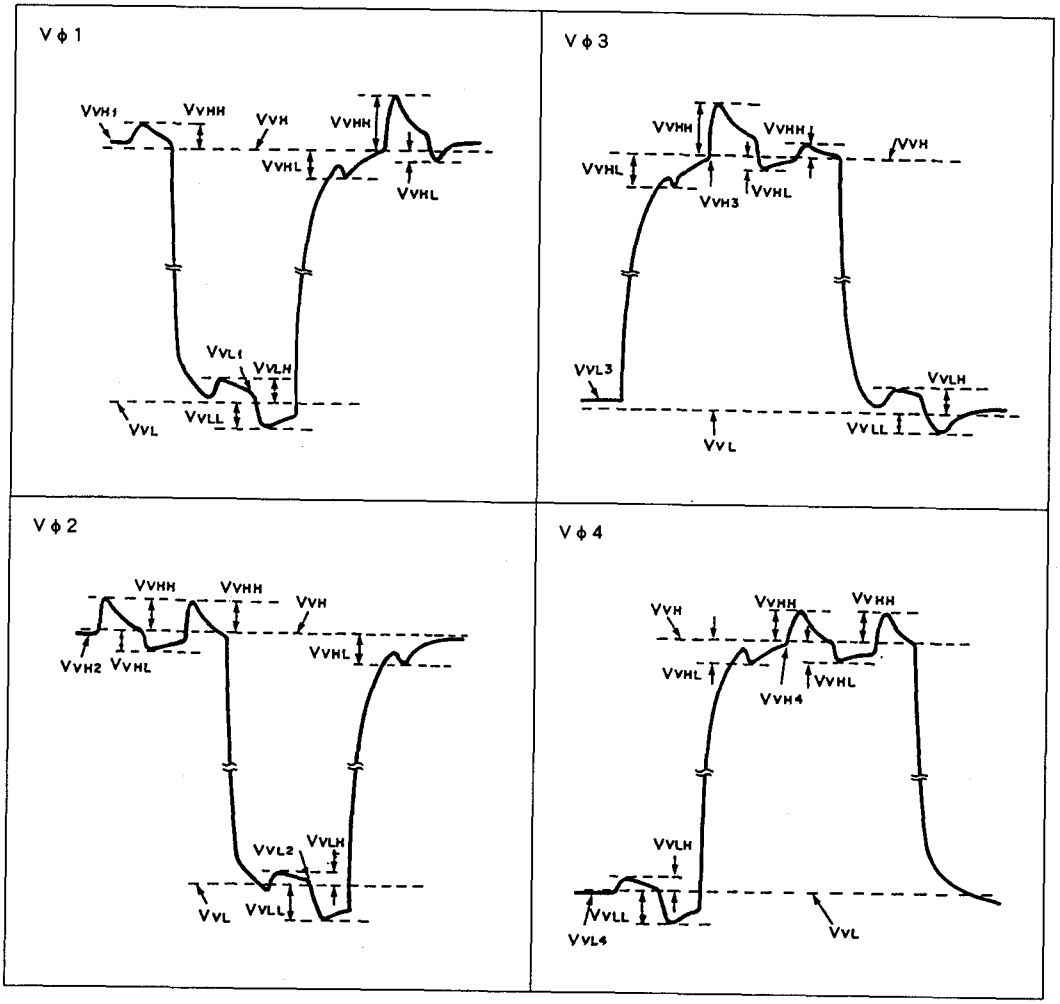
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

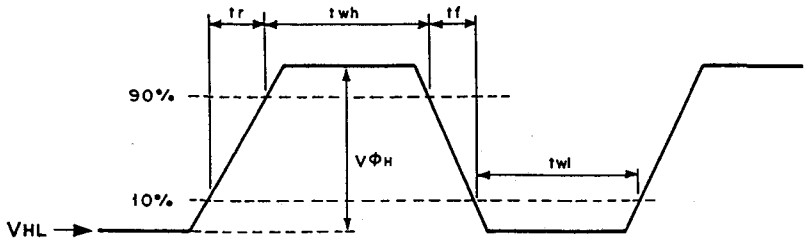
(1) Read out clock waveform



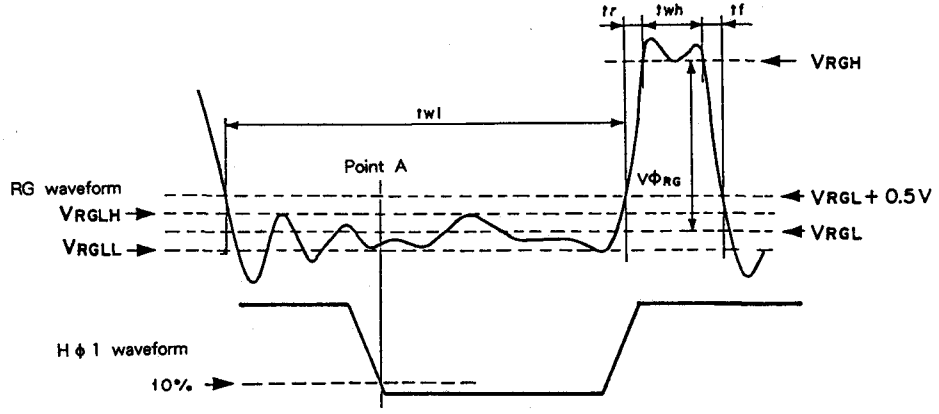
(2) Vertical transfer clock waveform



(3) Horizontal transfer clock waveform diagram



(4) Reset gate clock waveform diagram



V_{RGLH} is the maximum value and V_{RGLL} the minimum value of the coupling waveform in the period from Point A in the diagram above to RG rise.

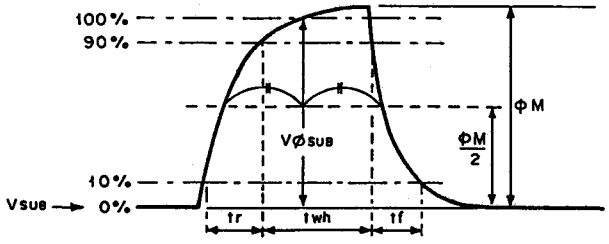
V_{RGL} is the mean value for V_{RGLH} and V_{RGLL}.

$$V_{RGL} = (V_{RGLH} + V_{RGLL}) / 2$$

V_{RGH} is the minimum value for twh period.

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

(5) Substrate clock waveform



Clock Switching Characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	V_T	2.3	2.5						0.5			0.5		µs	During read out
Vertical transfer clock	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$										0.015		0.25	µs	*1
Horizontal transfer clock	$H\phi$	37	41		38	42			12	15	*2	10	15	ns	During imaging
Horizontal transfer clock	$H\phi_1$		5.6						0.012			0.012		µs	During parallel serial conversion.
Horizontal transfer clock	$H\phi_2$					5.6			0.012			0.012		µs	
Reset gate clock	ϕ_{RG}	11	15		75	79			6.5			4.5		ns	
Substrate clock	ϕ_{SUB}	1.5	2.0							0.5			0.5	µs	During charge drain.

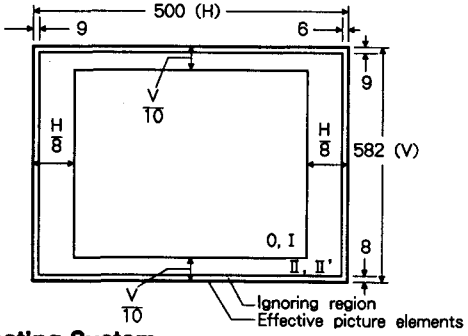
* 1) When vertical transfer clock driver CXD1250 is in use.
* 2) tf ≦ tr–2 ns

Image Sensor Characteristics

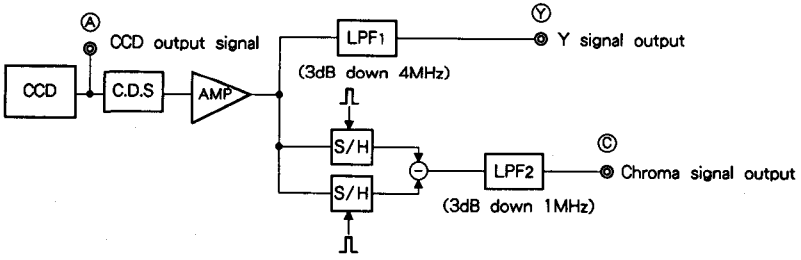
(Ta=25℃)

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	340	450		mV	1	
Saturation signal	Ysat	540			mV	2	Ta=60℃
Smear	Sm		0.007	0.012	%	3	
Video signal shading	SHy			20	%	4	Zone 0, I
				25	%	4	Zone 0 to II'
Uniformity between signal channels	Δ Sr			10	%	5	
	Δ Sb			10	%	5	
Dark signal	Ydt			2	mV	6	Ta=60℃
Dark signal shading	Δ Ydt			1	mV	7	Ta=60℃
Flicker Y	Fy			2	%	8	
Flicker R – Y	Fcr			5	%	8	
Flicker B – Y	Fcb			5	%	8	
Horizontal stripes R	Lcr			3.5	%	9	
Horizontal stripes G	Lcg			3.5	%	9	
Horizontal stripes B	Lcb			3.5	%	9	
Horizontal stripes W	Lcw			3.5	%	9	
Lag	Lag			0.5	%	10	

Zone Chart of Video Signal Shading



Testing System



Note) Adjust AMP gain so that total gains between Ⓐ and Ⓨ and between Ⓐ and Ⓒ equal 1.

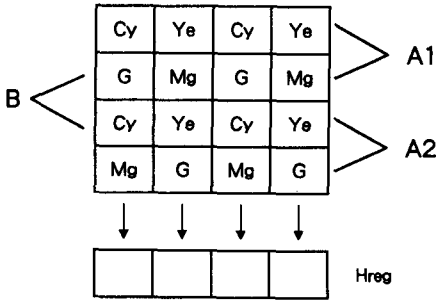
Image Sensor Characteristics Test Method

◎ Test conditions

① Through the following tests the substrate voltage and reset gate clock voltage are set to the value displayed on the device, while the device drive conditions are at the typical value of the bias and clock voltage conditions.

② Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OB) is set as the reference for the signal output which is taken as the Y signal output or the chroma signal output of the testing system.

◎ Color coding of CFA (Color Filter Array) & Composition of luminance (Y) and chrominance (C) signals



Color Coding Diagram

CFA of this image sensor is shown in the Figure. This complementary CFA is used with a "field integration mode", where all of the photosites are read out during each video field. Signals from two vertically adjacent photosites, such as line A1 or A2 for field A, are summed when the image charge is transferred into the vertical storage columns.
The read out line pairing is shifted down one line for field B. The sensor output signals through the horizontal register (H reg.) at line A1 are [G+Cy], [Mg+Ye], [G+Cy], [Mg+Ye].

These signals are processed in order to compose Y and C signals. By adding the two adjacent signals at line A1, Y signal is formed as follows:

$$Y = \{ (G+Cy) + (Mg+Ye) \} \times 1/2$$
$$= 1/2 \{ 2B+3G+2R \}$$

C signal is composed by subtracting the two adjacent signals at line A1.

$$R - Y = \{ (Mg+Ye) - (G+Cy) \}$$
$$= \{ 2R - G \}$$

Next, the signals through H reg. at line A2 are

[Mg+Cy], [G+Ye], [Mg+Cy], [G+Ye]

Similarly, Y and C signals are composed at line A2.

$$Y = \{ (G+Ye) + (Mg+Cy) \} \times 1/2$$
$$= 1/2 \{ 2B+3G+2R \}$$
$$-(B - Y) = \{ (G+Ye) - (Mg+Cy) \}$$
$$= -\{ 2B - G \}$$

Accordingly, Y signal is balanced in relation to the scanning lines, and C signal takes the form of R − Y and − (B − Y) on alternate lines.
It is the same for B field.

◎ Definition of standard imaging conditions

① Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 cd/m², color temperature 3200K Halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t=1.0mm) as IR cut filter and image at F5.6.

② Standard imaging condition II: Image a light source (color temperature of 3200K) which uniformity of brightness is within 2% at all angles. Use a testing standard lens with CM500S (t=1.0mm) as IR cut filter. The light intensity is adjusted to the value indicated in each testing item by lens diaphragm.

1. Sensitivity
   Set to standard image condition I. After selecting the electronic shutter mode at a 1/250 sec. shutter speed, measure the Y signal (Ys) at the center of the screen and substitute in the following formula.

   $$S = Ys \times \frac{250}{50}$$

2. Saturation signal
   Set to standard imaging condition II. Adjust light intensity to 10 times that of Y signal output average value (Y_A=180mV), then test Y signal minimum value.

3. Smear
   Set to standard imaging condition II. Adjust light intensity to 500 times that of Y signal output average value (Y_A=180mV). Stop read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the maximum value YSm of Y signal output.

   $$Sm = \frac{YSm}{Y_A} \times \frac{1}{500} \times \frac{1}{10} \times 100\ (\%)\ (1/10V)$$

4. Video signal shading
   Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A=180mV) with lens diaphragm at F5.6 to F8. Then test maximum (Ymax) and minimum (Ymin) values of Y signal.

   $$SHy = (Ymax - Ymin) / Y_A \times 100\ (\%)$$

5. Video signal between channels uniformity
   Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A=180mV). Then test maximum (Crmax, Cbmax) and minimum (Crmin, Cbmin) values of chroma signals from R − Y and B − Y channels.

   $$\Delta Sr = |(Crmax - Crmin) / Y_A| \times 100\ (\%)$$
   $$\Delta Sb = |(Cbmax - Cbmin) / Y_A| \times 100\ (\%)$$

6. Dark signal
   Test Y signal output average value Ydt when the device ambient temperature is at 60 °C and light is obstructed with horizontal idle transfer level as reference.

7. Dark signal shading
   Following 6, test maximum (Ydmax) and minimum (Ydmin) values of dark signal output.

   $$\Delta Ydt = Ydmax - Ydmin$$

8. Flicker

① Fy

Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A=180mV). Then test the Y signal difference (Δ Yf) between even field and odd field.

$Fy = (\Delta Yf / Y_A) \times 100\ (\%)$

② Fcr, Fcb

Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A=180mV). Then insert R or B filter, and test the C signal difference (Δ Cr, Δ Cb) between even field and odd field and the C signal output average value (CAr, CAb).

$Fci = (\Delta Ci / CAi) \times 100\ (\%)$ (i=r, b)

9. Lateral stripe

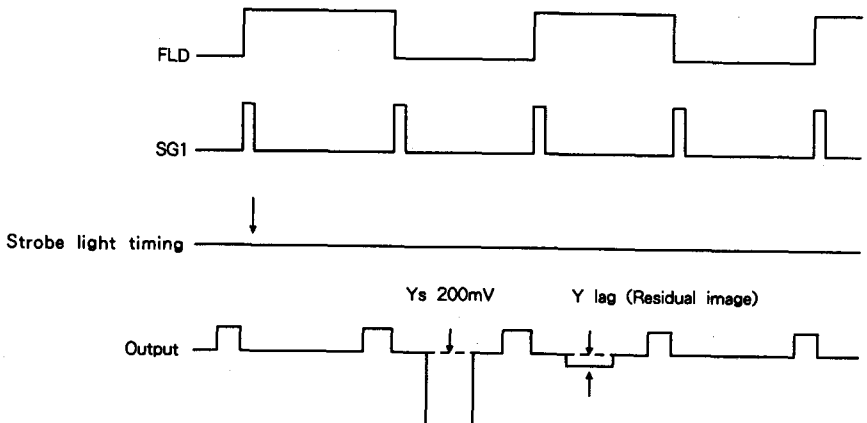
Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A=180mV). Then insert R, G and B filters respectively, and test the signal difference (Δ Yiw, Δ Yir, Δ Yig, Δ Yib) between Y signal lines of the same field.

$Lci = (\Delta Yli / Y_A) \times 100\ (\%)$ (i=w, r, g, b)

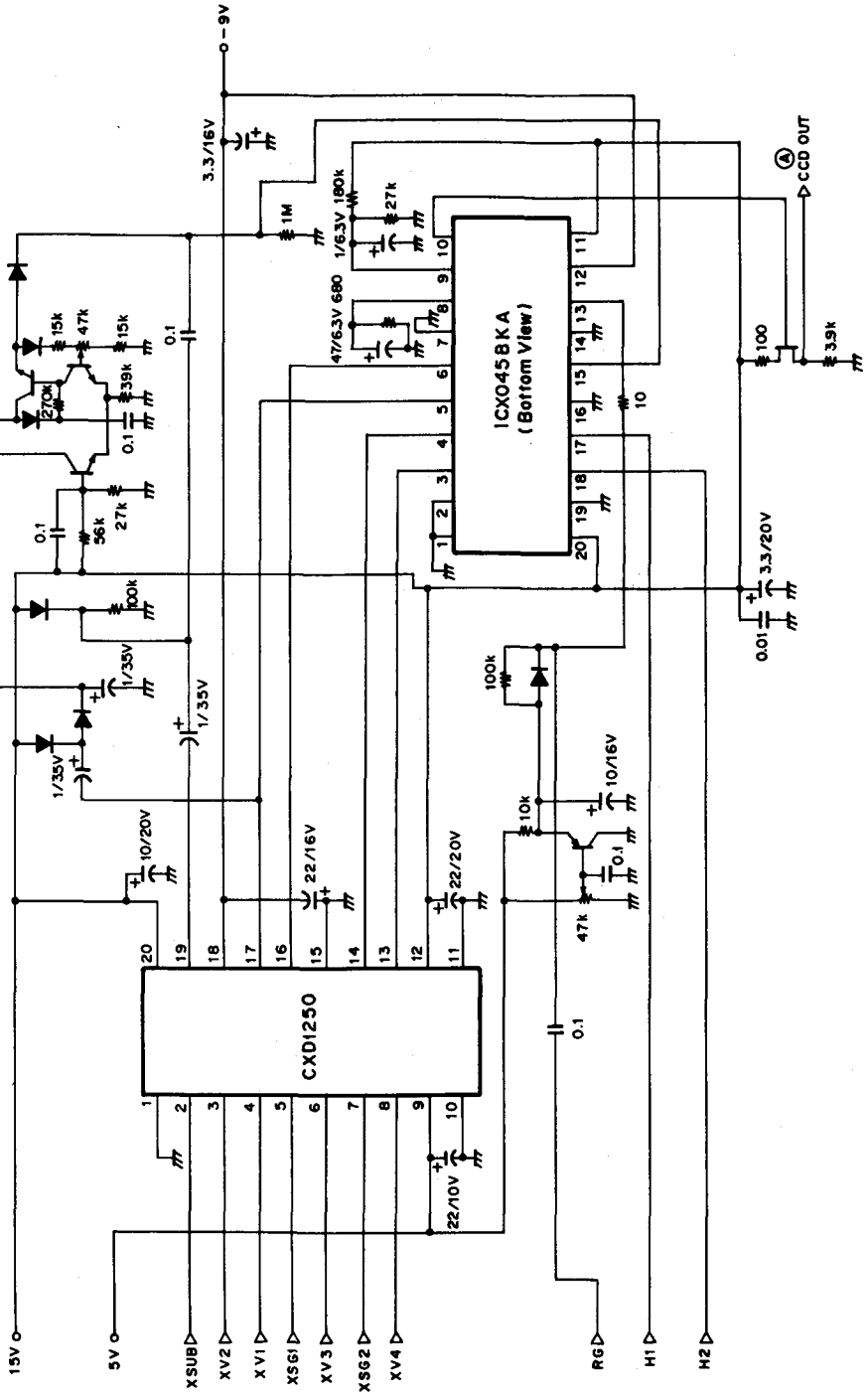
10. Residual image

Adjust Y signal output value (Ys) by strobe light to 200mV. Then light a stroboscopic tube with the following timing and test the residual image (Ylag).

Lag = (Ylag/Ys) × 100 (%)

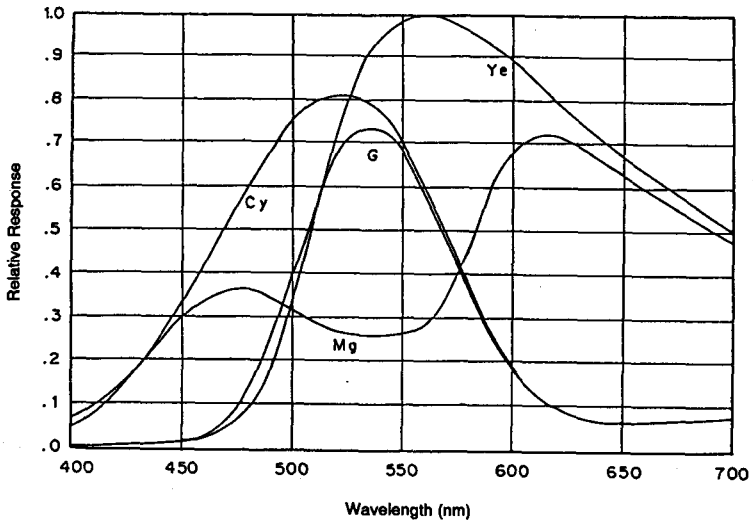


Drive Circuit

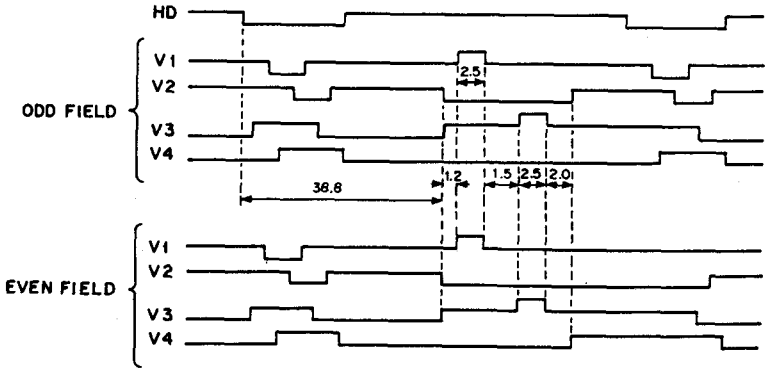


Spectral Sensitivity Characteristics

(Excluding light source characteristics, including lens characteristics)

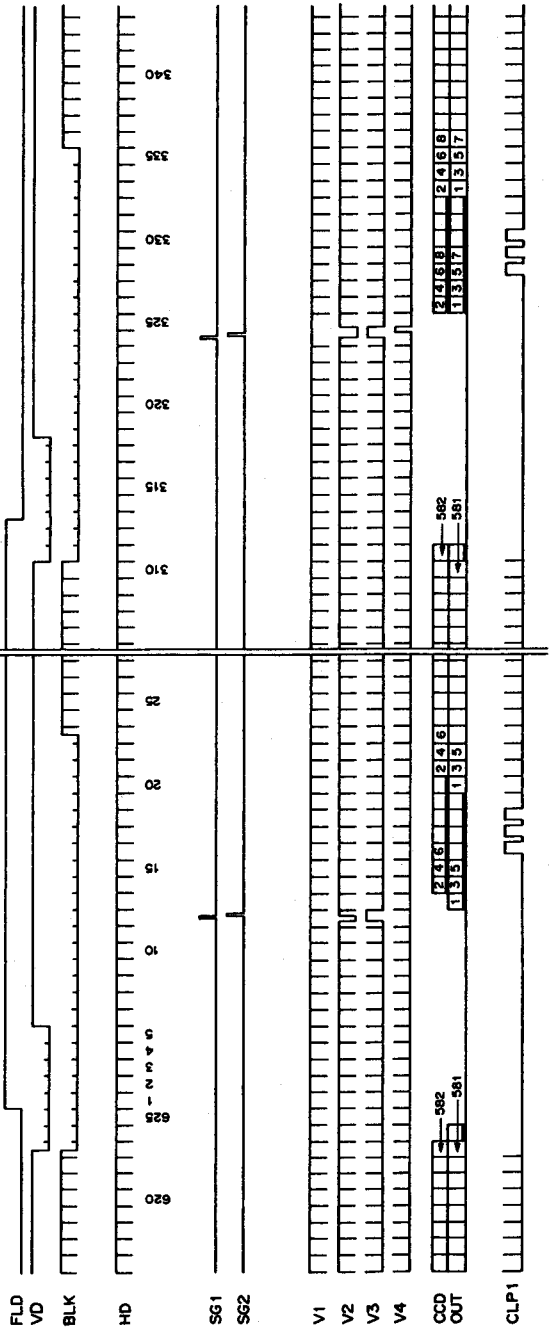


Sensor Read Out Clock Timing Chart

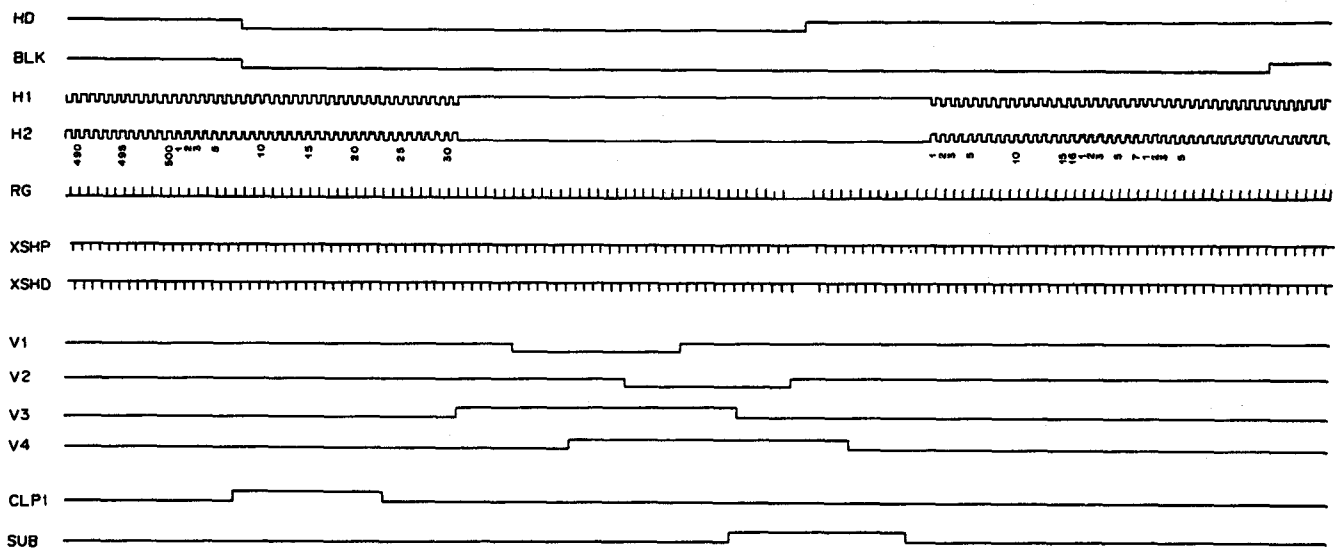


Unit : µs

Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



(During electronic shutter operation)

Handling Instructions

1) Static charge prevention
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensor.
   e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
   a) Make sure the package temperature does not exceed 80 °C .
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an imaging device do not use a solder suction equipment. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
   a) Operate in clean environments (around class 1000 will be appropriate).
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

CCD Imaging Blocks for Color Camera

Description

IU022AK-30A/40A and IU024AK-30A/40A are solid state imaging blocks developed for color video cameras. They incorporate an image correction optical filter (Optical crystal low pass filter, infrared cut filter) indispensable for solid state imaging devices.
These blocks can easily be attached to the rear of a lens or the mount of an interchangeable lens to provide a lightweight, compact imaging system.

Pin Configuration (Top View)

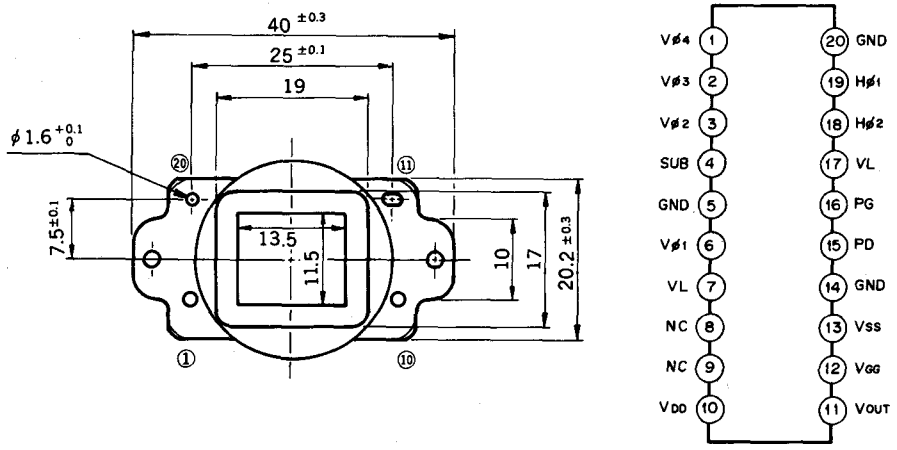


Fig. 1

Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	$V_{\phi 4}$	Vertical register transfer clock input	11	V_{OUT}	Signal output
2	$V_{\phi 3}$	Vertical register transfer clock input	12	V_{GG}	Output amplifier gate bias
3	$V_{\phi 2}$	Vertical register transfer clock input	13	V_{SS}	Output amplifier source bias
4	SUB	Substrate	14	GND	GND
5	GND	GND	15	PD	Precharge drain bias
6	$V_{\phi 1}$	Vertical register transfer clock input	16	PG	Output reset clock input
7	VL	Protected transistor bias	17	VL	Protected transistor bias
8	NC	Non connection	18	$H_{\phi 2}$	Horizontal register transfer clock input
9	NC	Non connection	19	$H_{\phi 1}$	Horizontal register transfer clock input
10	V_{DD}	Supply voltage	20	GND	GND

Package Outline (Unit : mm)

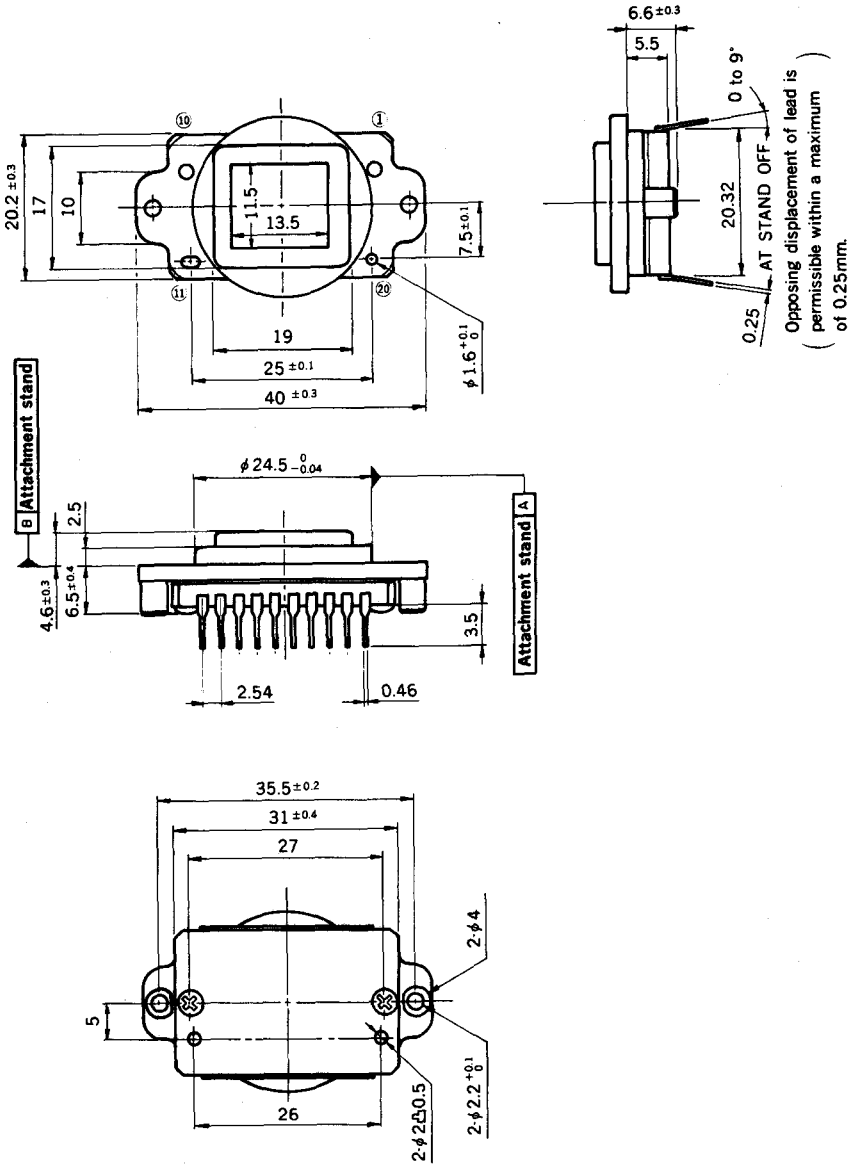


Fig. 2

Configuration and Optical Characteristics

Item	Ratings	Unit	Remark
Appearance, size, attachment.	See the Package Outline (Fig. 2)		
Optical axis	Within the ϕ11.1 circle with the Ref. A center are the effective elements.	mm	Fig. 2 Standard location A
Image rotation	Within ±1	deg	ϕ1.6 spot
Back focus	1.74±0.3	mm	(In AIR) Fig. 2 Standard surface B
Tilt	60	μm	Fig. 2 Standard surface B
Optical thickness	6.6	mm	BK-7 equivalent (including optical filter assembly and optical parts of CCD)
Optical filter	Four-layer laminated type		
Spectral sensitivity characteristics	See Fig. 3		
Weight	14	g	

Note) See the specifications of ICX022AK-3/4 and ICX024K-3/4 for imaging characteristics, electrical characteristics and absolute maximum ratings.

Spectral sensitivity characteristics example

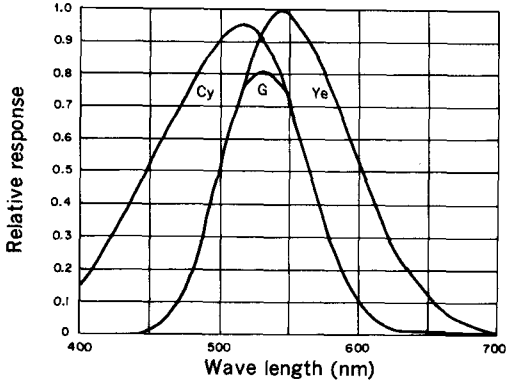


Fig. 3

Environmental Characteristics

Item	Condition	Requirements
Vibration	7G, 10 to 30Hz, 300sec sweep, each 15min for x, y, z directions	The above structure satisfies optical characteristics.
Impact	80G, in 6directions	
Low temperature durability	−30°C, 240 hours	
High temperature durability	80°C, 240 hours	
Heat cycle	−30°C to 25°C to 80°C 30min to 5min to 30min 10cycles	
High temperature and high humidity durability	60°C, 95%, 240hours	

CCD Image Sensor (Black/White)

2) CCD Image Sensor (Black/White)

Type	Functions				Page
	Optical size	TV System	Effective pixels	Features	
ICX022BL-3	2/3 inches	EIA	768H×493V	Variable speed electronic shutter equipped	165
ICX024BL-3		CCIR	756H×581V		179
ICX026BLA	1/2 inch	EIA	510H×492V	Variable speed electronic shutter equipped	193
ICX038ALA			768H×494V		206
ICX027BLA	1/2 inch	CCIR	500H×582V	Variable speed electronic shutter equipped	222
ICX039ALA			752H×582V		235
ICX044ALA	1/3 inch	EIA	510H×492V	Variable speed electronic shutter equipped	251
ICX045ALA		CCIR	500H×582V		267

SONY®

ICX022BL-3

Interline-type CCD Image Sensor

Description

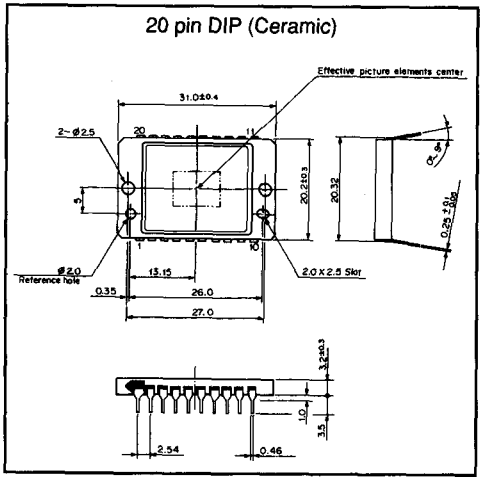
ICX022BL-3 is an interline-type CCD image sensor designed for B/W video cameras using the CCIR system. With 768 effective pixels horizontally and 493 vertically the image size stands at 2/3 inches.

The adaption of HAD (Hole Accumulation Diode) sensors as photo sensor elements greatly reduces dark current.

Field integration read out method allows for high dynamic resolution. Electric charges are swept through the substrate to provide the electronic shutter function with a variable charge storage time.

Package Outline

Unit: mm

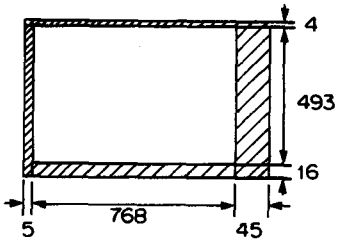


Features

- Image size: 2/3 inches (8.8 mm(H) × 6.6 mm(V))
- Effective pixels: 768 (H) × 493 (V)
- Effective optical black
  - Horizontal: Front 5 pixels
    Back 45 pixels
  - Vertical: Front 16 pixels
    Back 4 pixels
- High resolution, high sensitivity and low noise
- Low lag and low smear
- Low dark current
- Anti-blooming function
- No figure distortion or microphonic noise
- γ characteristics: 1

Element Structure

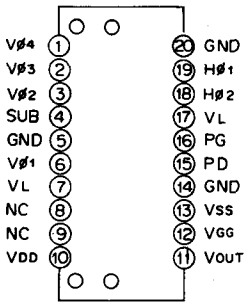
- Interline type CCD image sensor
- Chip size: 10.0 mm(H) × 8.2 mm(V)
- Unit cell size: 11.0 µm(H) × 13.0 µm(V)
- Dummy bits: horizontal 22-bits, vertical 1-bit (even fields only)
- HAD-Sensor (Hole Accumulation Diode-Sensor)
- High sensitivity output amplifier
- Black film on aluminium (On chip)
- N type substrate P-well structure



Optical black configuration

E90233-YA

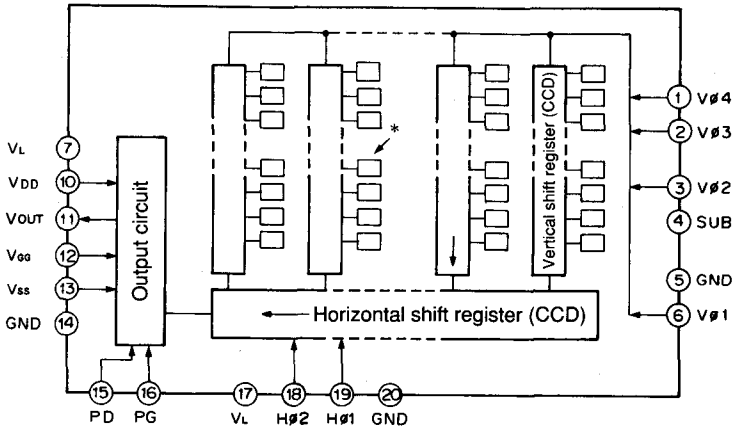
Pin Configuration



Pin Description

Pins No.	Symbol	Description	Pins No.	Symbol	Description
1	$V\phi_4$	Vertical register transfer clock	11	V_{OUT}	Signal output
2	$V\phi_3$	Vertical register transfer clock	12	V_{GG}	Output amplifier gate
3	$V\phi_2$	Vertical register transfer clock	13	V_{SS}	Output amplifier source
4	SUB	Substrate (OFD) bias	14	GND	GND
5	GND	GND	15	PD	Pre-charge drain bias
6	$V\phi_1$	Vertical register transfer clock	16	PG	Output reset clock
7	V_L	Protective transistor bias	17	V_L	Protective transistor bias
8	NC		18	$H\phi_2$	Horizontal register transfer clock
9	NC		19	$H\phi_1$	Horizontal register transfer clock
10	V_{DD}	Output amplifier drain supply	20	GND	GND

Imaging Device Function Block



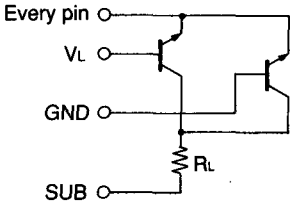
*Note) —□ : Photo sensor

Absolute Maximum Ratings

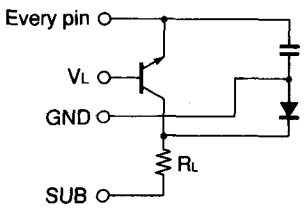
Item	Ratings	Unit	Remarks
SUB - GND	-0.3 to +55	V	
V_{DD}, PD, V_{OUT}, V_{SS} - GND	-0.3 to +20	V	
V_{DD}, PD, V_{OUT}, V_{SS} - SUB	-55 to +10	V	Note 1
Horizontal and vertical transfer clock inputs — GND	-15 to +20	V	
Horizontal and vertical transfer clock inputs — SUB	-65 to +10	V	Note 1
Potential difference between vertical transfer clock inputs	+15	V	Note 2
Potential difference between horizontal transfer clock inputs	+17	V	
$H\phi_1$, $H\phi_2$ - $V\phi_4$	-17 to +17	V	
PG, V_{GG} - GND	-10 to +15	V	Note 1
PG, V_{GG} - SUB	-55 to +10	V	
V_L - SUB	-65 to +0.3	V	
Pins other than GND, SUB and V_L - V_L	-0.3 to +27	V	
Storage temperature	-30 to +80	°C	
Operation guarantee ambient temperature	-10 to +55	°C	

Note) 1. This image sensor consists of an N substrate P-Well structure where a protection transistor is connected to each pin accordingly. If a voltage exceeding 10 V is applied to pins other than V_L against the SUB pin, a punch through current will flow. Since a series resistance R_L is located between each pin and SUB, the device will withstand destruction through any rush voltage over 10 V. The series resistance R_L must be more than 1 kΩ between Vp-p and SUB, more than 500 Ω between V_{OUT} and SUB and more than 5 kΩ between V_{SS} or PD and SUB. The series resistance between other pins (except V_L and GND) and SUB must be more than 5kΩ.

1) V_{DD}, PD, V_{OUT} and Vss pins



2) Pins other than 1) (except V_L and GND)



Equivalent circuit

2. In case of clock width <10 µs and clock duty factor <0.1%, up to 27 V is guaranteed.

Electrical Characteristics

Bias conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage of output circuit	V_{DD}	14.55	15.0	15.45	V	Note 1
	V_{PD}	14.55	15.0	15.45	V	Note 1
	V_{GG}	1.6	2.0	2.4	V	
	V_{SS}	Ground with a 390 Ω resistance				±5%
Substrate voltage adjustable range	V_{SUB}	9		19	V	Note 2
Regulation range after substrate voltage adjustment	V_{SUB}	−3		3	%	
Protection transistor bias	V_L	To be the vertical transfer clock low-level clamp bias				

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output circuit current	I_{DD}		5.0		mA	Note 3
Input current	I_{IN1}			1	μA	Note 4
	I_{IN2}			10	μA	Note 5

Note) 1. V_{PD} and V_{DD} must have the same voltage.

2. Indication of the substrate voltage (V_{SUB}) set value:
The set value is indicated on the rear of the imaging device by a code. Adjust to obtain the indicated voltage at the SUB pin.
V_{SUB} code – Two digit indication

The integral code correspond to the following actual values:

Integral codes	9	A	B	C	D	E	F	G	H	I	J
Numerical value	9	10	11	12	13	14	15	16	17	18	19

EX.) F5 → 15.5 (V)

3. Ground V_{SS} with a 390 Ω resistance.

4. 1) Current flowing to the ground when a voltage of 20 V is applied to V_{DD}, PD, V_{OUT}, V_{SS} and SUB pins. Test ground all the pins other than those under test.
2) Current flowing to the ground when a voltage of 20 V is applied to $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $H\phi_1$ and $H\phi_2$ pins in the order. Apply pin a voltage of 20 V to the SUB pins and ground pins other than those under test.
3) Current flowing to the ground when a voltage of 15 V is applied to PG and V_{GG} pins in the order. Apply a voltage of 15 V to the SUB pin and ground pins other than those under test.
4) Current flowing to the ground when V_L pin is grounded, GND and SUB pins are open and a voltage of 27 V is applied to other pins.

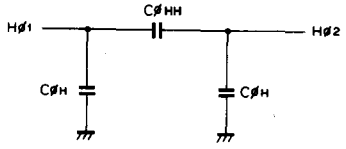
5. Current flowing to the ground when a voltage of 55 V is applied to the SUB pin. In this case ground pins other than those under test.

Clock Voltage Conditions
Clock voltage

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Read clock voltage	V_{VT}	13.0		15.0	V	Note 1
Vertical transfer clock voltage	V_{VHH}			1.3	V	Note 2
	V_{VH}	-0.5		0.7	V	
	$V_{\phi V}$	8.0			V	
	V_{VLL}	-10.5			V	
Horizontal transfer clock voltage	V_{HHH}			5.2	V	Note 3
	V_{HL}	-3.0		-1.7	V	
	$V_{\phi H}$	5.2		8.0	V	
	V_{HLL}	-3.0			V	
Output reset clock voltage	V_{PGL}		0		V	Note 4
	$V_{\phi PG}$	7.0		13.0	V	
Substrate clock voltage	$V_{\phi SUB}$	23.0		27.0	V	Note 5

Clock capacitance

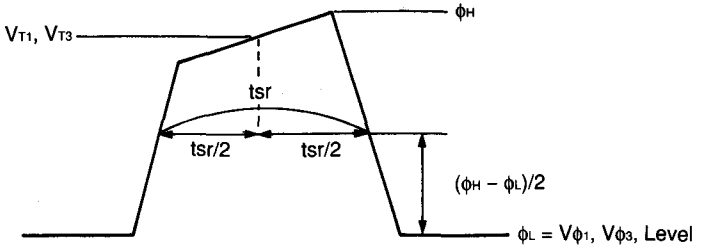
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Vertical transfer clock - GND	$C_{\phi V}$		5000		pF	
Capacitance between vertical transfer clocks	$C_{\phi VV}$		1500		pF	
Horizontal transfer clock - GND	$C_{\phi H}$		180		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Output reset clock - GND	$C_{\phi PG}$		10		pF	
Substrate clock - GND	$C_{\phi SUB}$		500		pF	



Equivalent circuit of horizontal transfer clock capacitance

Note) 1. Read clock voltage

1) The symbol "ϕ_L" expresses the voltage level while the read clock "V_T" of the vertical transfer clocks ("$V\phi_1$" and "$V\phi_3$") is set. The maximum value in the read clock waveform is expressed as "ϕ_H".
2) The period in which the voltage level becomes ($\phi_H - \phi_L$)/2 is expressed as "tsr". The voltage levels at "tsr/2" are expressed as "V_{T1}" (at $V\phi_1$) and "V_{T3}" (at $V\phi_3$). The smaller of "V_{T1}" and "V_{T3}" is defined as the read clock voltage "V_{VT}".



Read clock wave length

2. Vertical clock voltage

T = 559 ns (with a horizontal driving frequency of 14.32MHz)

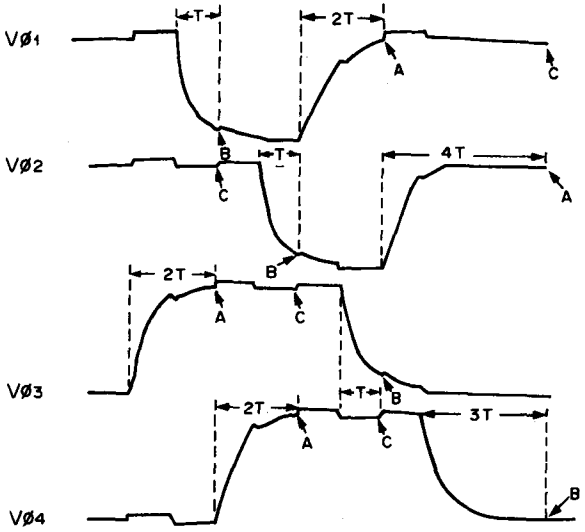
1) Definition of the vertical transfer clock amplitude
Level 2T after the rising edge of "$V\phi_3$" is expressed as "V_{3A}".
Level T after the falling edge of "$V\phi_1$" is expressed as "V_{1B}".
Level 2T after the rising edge of "$V\phi_4$" is expressed as "V_{4A}".
Level T after the falling edge of "$V\phi_2$" is expressed as "V_{2B}".
Level 2T after the rising edge of "$V\phi_1$" is expressed as "V_{1A}".
Level T after the falling edge of "$V\phi_3$" is expressed as "V_{3B}".
Level 4T after the rising edge of "$V\phi_2$" is expressed as "V_{2A}".
Level 3T after the falling edge of "$V\phi_4$" is expressed as "V_{4B}".

$V\phi_2$ Level T after the falling edge of "$V\phi_1$" is expressed as "V_{2C}".
$V\phi_3$ Level T after the falling edge of "$V\phi_2$" is expressed as "V_{3C}".
$V\phi_4$ Level T after the falling edge of "$V\phi_3$" is expressed as "V_{4C}".
$V\phi_1$ Level 3T after the falling edge of "$V\phi_4$" is expressed as "V_{1C}".

$\Delta 31 = (V_{3A} + V_{2C}) / 2 - V_{1B}$
$\Delta 42 = (V_{4A} + V_{3C}) / 2 - V_{2B}$
$\Delta 13 = (V_{1A} + V_{4C}) / 2 - V_{3B}$
$\Delta 24 = (V_{2A} + V_{1C}) / 2 - V_{4B}$

The minimum value of these is defined as the vertical transfer clock amplitude "$V\phi_V$".

2) The maximum value from V_{1A}, V_{2A}, V_{3A}, and V_{4A}, is defined as the high level V_{VH} of the clock.
3) The minimum level in a waveform which includes the vertical clock coupling is expressed as "V_{VLL}". "V_{VHH}" expresses the maximum level except in the period where read clock V_T is applied (in $V\phi_1$ and $V\phi_3$ only).



Vertical transfer clock waveform
T = 559ns (with a horizontal driving frequency of 14.32 MHz)

3. Horizontal transfer clock voltage

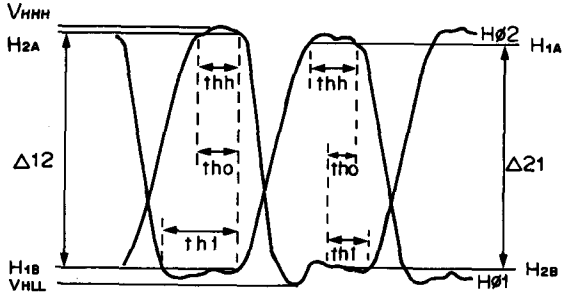
1) For the horizontal transfer clocks "Hφ1" and "Hφ2", the low-level period is expressed as "thl" and the high-level period is expressed as "thh". The symbol "tho" expresses the overlap period of "thl" and "thh".

2) The low level at which "thl", "thh" and "tho" satisfy the following time duration is expressed as "H_{1B}" and "H_{2B}".
And the high level is expressed as "H_{1A}" and "H_{2A}"

thl ≧ 10ns, thh ≧ 10ns, tho ≧ 5ns

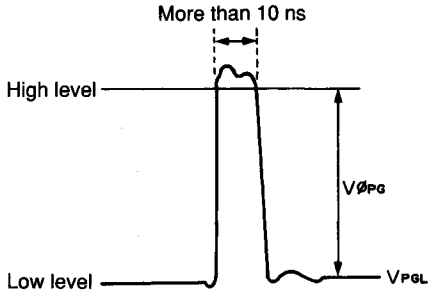
$\Delta 21 = H_{1A} - H_{2B}$
$\Delta 12 = H_{2A} - H_{1B}$

3) The minimum level in the waveform which contains the coupling of the horizontal transfer clocks "Hφ1" and "Hφ2" is expressed as "V_{HLL}" and the maximum level is expressed as "V_{HHH}".



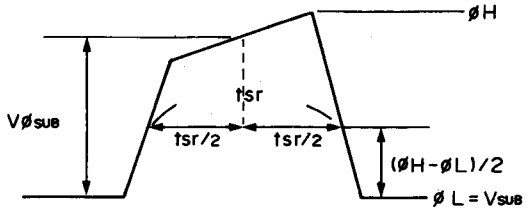
Horizontal transfer clock waveform

4. Output reset clock voltage
   1) The low level of the output reset clock is to be the GND in the circuit.
   2) The amplitude of the output reset PG clock "$V\phi_{PG}$" is defined as the maximum value of the amplitude which provides a high level period over 10 ns.



Waveform of PG clock

5. Substrate clock voltage
   1) Substrate voltage is expressed as ϕ_L and the maximum value of the substrate clock waveform as ϕ_H.
   2) The period during which voltage level reaches (ϕ_H – ϕ_L)/2 is expressed as tsr. The difference of voltage level with ϕ_L at tsr/2 is defined as substrate clock voltage $V\phi_{SUB}$.



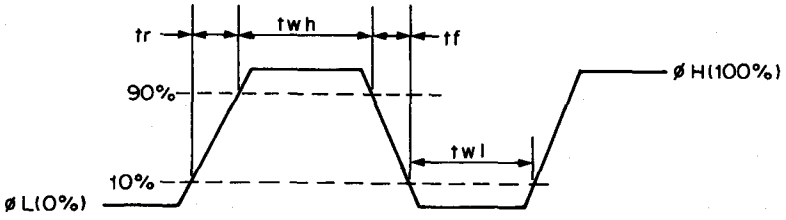
Substrate clock waveform

Driving Clock Waveform Conditions

1) Definition of ϕ_H (100%) and ϕ_L (0%)
   (1) For the horizontal transfer clocks ($H\phi_1$, $H\phi_2$), output reset clock ($PG\phi$) and vertical transfer clocks ($V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$), the maximum value in the clock waveform which includes no coupling is expressed as "ϕ_H" and the minimum value is expressed as "ϕ_L".
   (2) For the read clock (V_T), the maximum value in the clock waveform is expressed as "ϕ_H"."ϕ_L" expresses the voltage level while the read clock (V_T) of the vertical transfer clocks ($V\phi_1$, $V\phi_3$) is applied.
   (3) For the substrate clock ($SUB\phi$), the maximum value in the clock waveform is expressed as "ϕ_H" and the substrate voltage (V_{SUB}) as "ϕ_L".
2) Standard driving clock conditions (Typ.)

Horizontal drive frequency: 14.32MHz

Clock (Symbol)	twh	twl	tr	tf	Unit	Remarks
$H\phi_1$	18	33.7	10	8	ns	Imaging period
$H\phi_2$	18	33.7	10	8		
$H\phi_1$	4.9		0.01	0.01	µs	Parallel-serial converting period
$H\phi_2$		4.9	0.01	0.01		
ϕ_{PG}	12	53.7	2	2	ns	
$V\phi_1/V\phi_2$	61.6	1.6	0.1	0.1	µs	Imaging period
$V\phi_3/V\phi_4$	2.8	60.45	0.05	0.1		
V_T	2.4		0.2	0.1		Reading period
$SUB\phi$	1.0		0.08	0.1	µs	Electron sweep-off period



Clock waveform

Imaging Characteristics

(For the testing circuit, see P.11)
Ta=25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Testing method	Remarks
Sensitivity	Sg	220	300		mV	1	
Output saturation signal of sensor	Vsat	600			mV	2	During reading field
Smear	Smr		0.005	0.015	%	3	
Video signal shading	Svg			25	%	4	
Dark signal output	Vdt			2	mV	5	Ta=55°C
Dark signal shading	ΔVdt			1	mV	6	Ta=55°C

Note) Saturation signal and blooming margin are guaranteed only when the substrate voltage has been set to the voltage indicated on the back of the imaging device.

Test Methods

Conditions

1) The conditions required to drive the device through the following tests are converted by the bias conditions and the clock voltage conditions.
2) Blemish are excluded from the following tests and the signal output is based on the optical black level unless otherwise specified. The value obtained at the output test point becomes the test value.

Standard imaging conditions

1) Shoot the PTB-100 pattern box (luminance 706 Nit, color temperature 3200 K) with no pattern, using a FUJINON H6 × 12.5D (F1.4) lens at F8. Use the CM-500S (1.0 mmt) filter to cut off infrared rays.
2) Shoot a light source (color temperature 3200 K) which provides a uniform brightness within 2% over the whole screen.
   For infrared cut-off filter, use the CM-500S (1.0 mmt).

1. Set the standard imaging condition 1) and test signal voltages (Sg) the center of the screen.

2. Set to standard imaging condition 2) and adjust the light intensity to about ten times the intensity obtained at a signal voltage of 200 mV. Then obtain the minimum value of the signal voltage over the whole screen.

3. Set to standard imaging condition and adjust the light intensity to about 1000 times the intensity obtained at a signal voltage of 200 mV. At that time make sure there is no blooming and the vertical resistor is not saturated.

4. Set to standard imaging condition 2) and adjust the light intensity so that the signal voltage (V_{SG}) becomes 200 mV. Then, turn V_T off and obtain the maximum value of the signal output "V_{SM}" after stopping the horizontal resistor 50 H at the effective picture element.

$$Smr = \frac{V_{SM}}{V_{SG}} \times \frac{1}{50} \times \frac{1}{10} \times 100\ (\%)$$

(Converted into 1/10 V system)

5. Set to standard imaging condition 2) and test the signal voltage to obtain maximum (V_G max) and minimum (V_G min) values.
The light intensity is adjusted so that the average value of the signal voltage (V_G average) becomes about 200 mV.

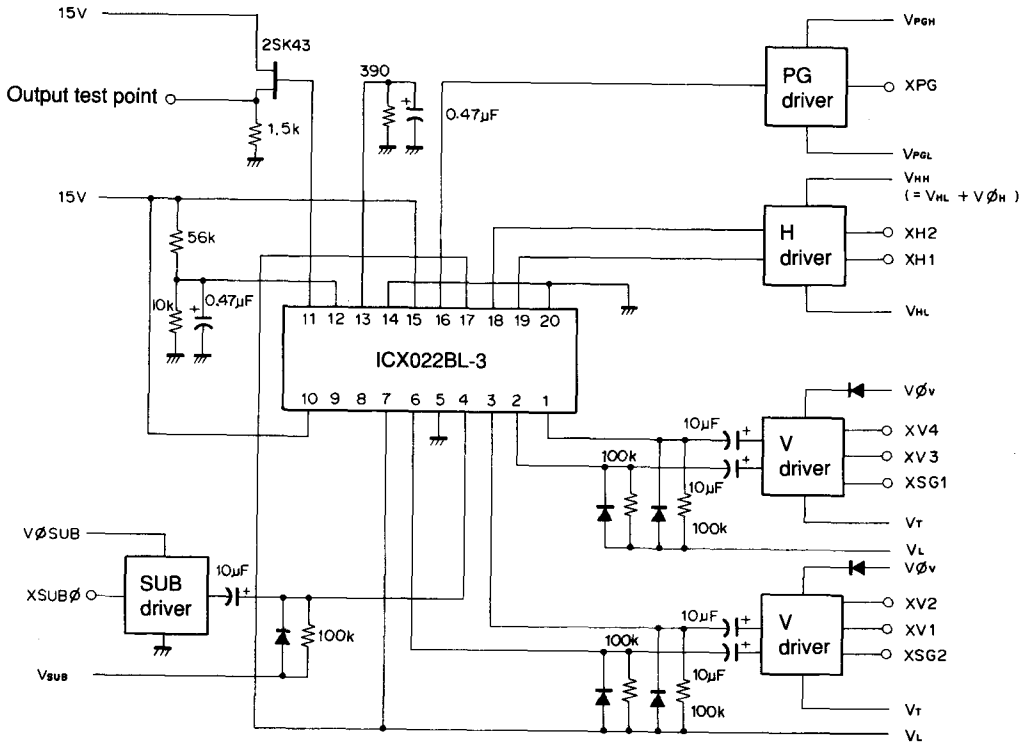
$$Svg = \frac{V_G\,max - V_G\,min}{V_G\ average} \times 100\ (\%)$$

6. Measure the mean voltage of the dark current signal based on the horizontal free-transfer level in a light-shaded condition with an ambient temperature of 55°C.

7. Following measurement 6, test the dark current signal voltage to obtain the maximum (Vd max) and minimum (Vd min) values. Spot defects are ignored in this test.

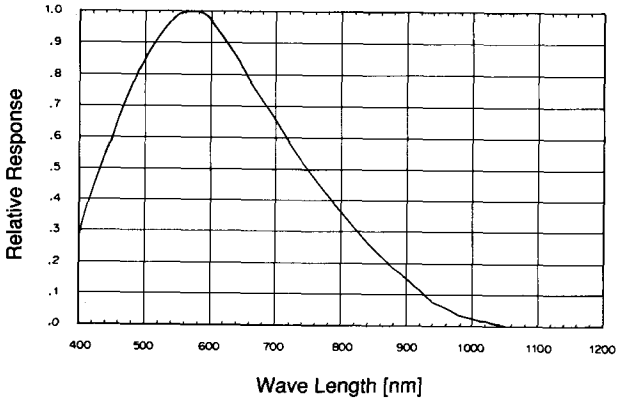
ΔVdt = (Vd max − Vd min)

Electrical Characteristics Test Circuit

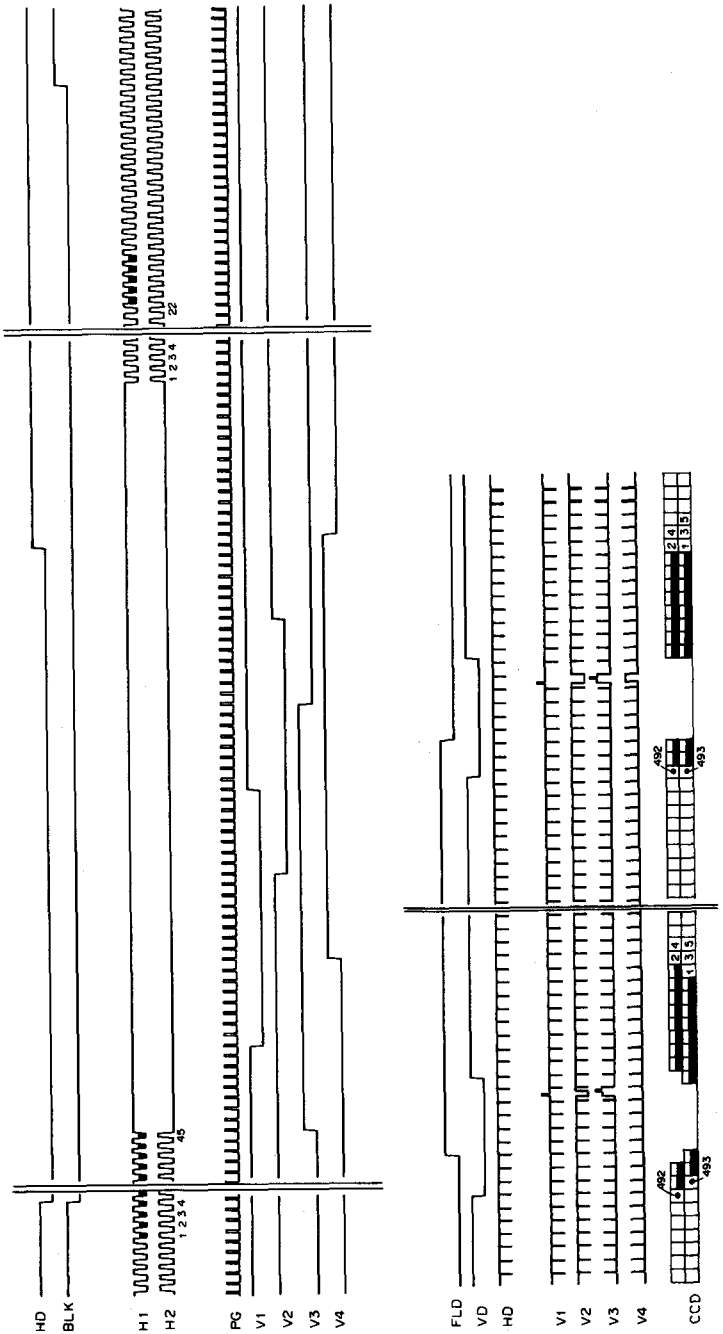


Spectrum Sensitivity Characteristics

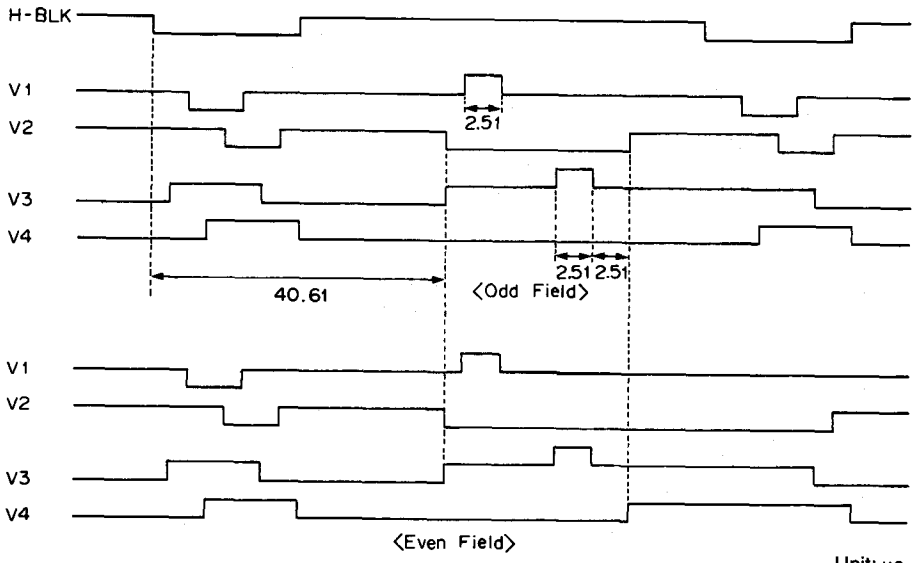
- Typical example, excluding illuminant characteristics



Driving Pulse Timing Chart

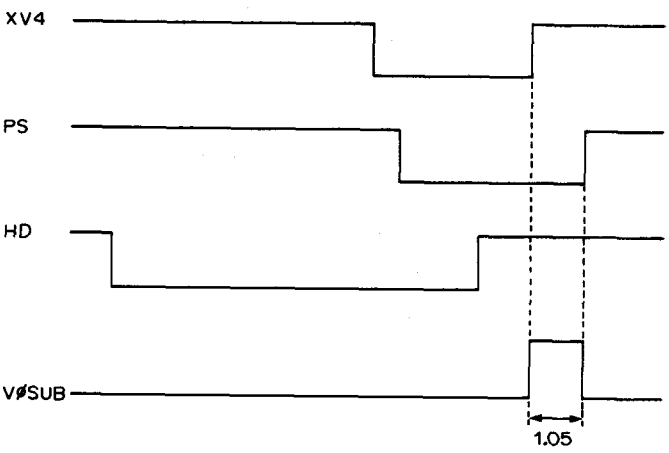


Sensor Read Clock Timing Chart



Unit: µs

Charge Drain Clock Timing Chart



Unit: µs

Handling Instructions

1) Static charge prevention
CCD image sensor are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount cool sufficiently.
c) To dismount an imaging device do not use a solder pult. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

7) Defect compensation ROM
This is shipped in its own case in pair with the CCD image sensor. Pair with the CCD image sensor bearing the same serial number during mounting. When the CCD image sensor has no defect as there is no serial number. Pair with a ROM without serial number that only has system data input.

Interline-type CCD Image Sensor

Description

ICX024BL-3 is an interline-type CCD image sensor for B/W video cameras designed for the CCIR system.

Effective pixels number 756 horizontally and 581 vertically.

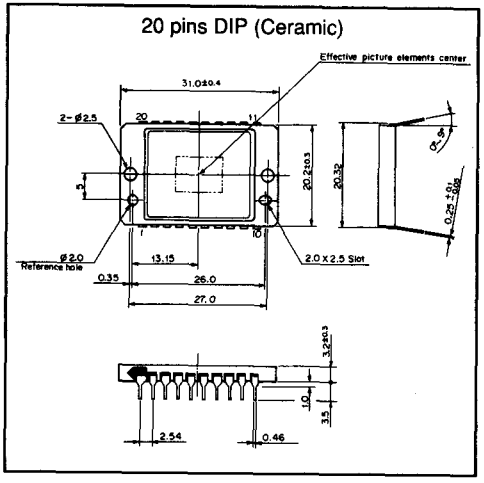
Field integration read out method ensures high dynamic resolution.

Features

- Image size: 2/3 inches (8.8 mm(H) × 6.6 mm(V))
- Effective pixels: 756 (H) × 581 (V)
- Effective optical black
  Horizontal: Front 5 pixels
  Back 55 pixels
  Vertical: Front 19 pixels
  Back 6 pixels
- High resolution, high sensitivity and low noise.
- Low lag and low smear
- Low dark current
- Anti-blooming function
- Electronic shutter function
- Neither figure distortion nor microphonic noise.
- γ characteristics: 1

Package Outline

Unit: mm



Element Structure

- Interline type CCD image sensor
- Chip size: 10.0 mm(H) × 8.2 mm(V)
- Unit cell size: 11.0 μm(H) × 11.0 μm(V)
- Dummy bits: horizontal 22-bits, vertical 1-bit (even field only)
- HAD (Hole Accumulation Diode) Sensor

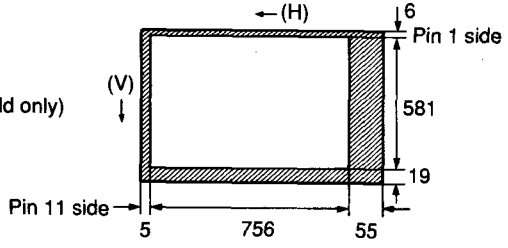
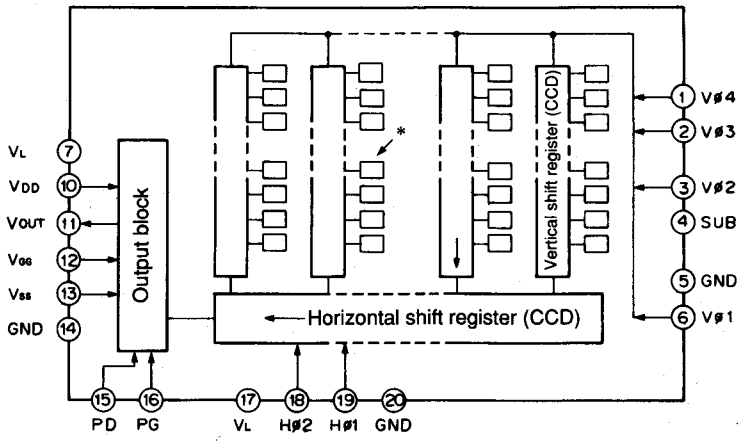


Fig. 1 Optical black configuration

Imaging Device Function Block and Pin Configuration



*Note) —□—: Photo sensor

Pin Description

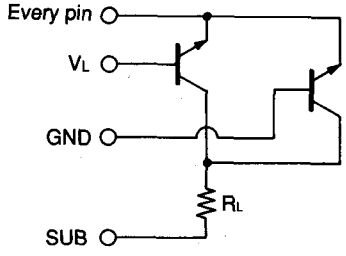
No.	Symbol	Description	No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	11	VOUT	Signal output
2	Vφ3	Vertical register transfer clock	12	VGG	Output amplifier gate
3	Vφ2	Vertical register transfer clock	13	VSS	Output amplifier source
4	SUB	Substrate (OFD) bias	14	GND	GND
5	GND	GND	15	PD	Pre-charge drain bias
6	Vφ1	Vertical register transfer clock	16	PG	Output reset clock
7	VL	Protective transistor bias	17	VL	Protective transistor bias
8	NC		18	Hφ2	Horizontal register transfer clock
9	NC		19	Hφ1	Horizontal register transfer clock
10	VDD	Output amplifier drain supply	20	GND	GND

Absolute Maximum Ratings

Item	Ratings	Unit	Remarks
Between SUB and GND	−0.3 to +5.5	V	
Between each of V_{DD}, PD, V_{OUT}, V_{SS} and GND	−0.3 to +20	V	
Between each of V_{DD}, PD, V_{OUT}, V_{SS} and SUB	−55 to +10	V	Note 1
Between each of Horizontal and vertical transfer clock inputs and GND	−15 to +20	V	
Between each of Horizontal and vertical transfer clock inputs and SUB	−65 to +10	V	Note 1
Potential difference between vertical transfer clock inputs	15	V	Note 2
Potential difference between horizontal transfer clock inputs	17	V	
Between each of $H\phi_1$, $H\phi_2$ and $V\phi_4$	−17 to +17	V	
Between each of PG, V_{GG} and GND	−10 to +15	V	
Between each of PG, V_{GG} and SUB	−55 to +10	V	Note 1
Between V_L and SUB	−65 to +0.3	V	
Between pins other than GND, SUB, V_L and V_L	−0.3 to +27	V	
Storage temperature	−30 to +80	°C	
Guarantee operational ambient temperature	−10 to +55	°C	

Note) 1. This image sensor consists of an N-type substrate P-Well structure where a protective transistor is connected to each pin accordingly. If a voltage exceeding 10 V is applied to pins other than V_L against the SUB pin, a punch through current will flow. Since a series resistance R_L is located between each pin and SUB, the device will withstand destruction through any rush voltage over 10 V. The series resistance R_L must be more than 1 kΩ between V_{DD} and SUB, more than 500 Ω between V_{OUT} and SUB and more than 5 kΩ between V_{SS} or PD and SUB. The series resistance between other pins (except V_L and GND) and SUB must be more than 5kΩ.

1) V_{DD}, PD, V_{OUT} and Vss pins



2) Pins other than 1) (except V_L and GND)

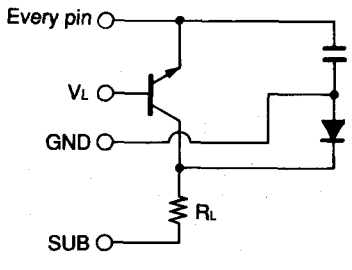


Fig. 2 Equivalent circuits

2. In case clock width is as follows: <10 µs and clock duty factor <0.1%, up to 27 V is guaranteed.

Electrical Characteristics
Bias conditions

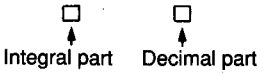
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage of output circuit	V_{DD}	14.55	15.0	15.45	V	Note 1
	V_{PD}	14.55	15.0	15.45	V	Note 1
	V_{GG}	1.6	2.0	2.4	V	
	V_{SS}	Ground with a 390 Ω resistance				±5%
Substrate voltage adjustable range	V_{SUB}	9		19	V	Note 2
Regulation range after substrate voltage adjustment	V_{SUB}	-3		3	%	
Protective transistor bias	V_L	To be the vertical transfer clock low-level clamp bias				

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output circuit current	I_{DD}		5.0		mA	Note 3
Input current	I_{IN1}			1	μA	Note 4
	I_{IN2}			10	μA	Note 5

Note) 1. V_{PD} and V_{DD} must have the same voltage.

2. Indication of the substrate voltage (V_{SUB}) set value:
The set value is indicated on the rear of the imaging device by a code. Adjust to obtain the indicated voltage at the SUB pin.
V_{SUB} code - Two digits indication



The integral code corresponds to the following actual values:

Integral codes	9	A	B	C	D	E	F	G	H	I	J
Numerical value	9	10	11	12	13	14	15	16	17	18	19

EX.) F5 → 15.5 (V)

3. Ground V_{SS} with a 390 Ω resistance

4. 1) Current flowing to the ground when a voltage of 20 V is applied to V_{DD}, PD, V_{OUT}, V_{SS} and SUB pins. Ground all pins other than those under test.
2) Current flowing to the ground when a voltage of 20 V is applied to $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $H\phi_1$ and $H\phi_2$ pins in the order. Apply a voltage of 20 V to the SUB pins and ground pins other than those under test.
3) Current flowing to the ground when a voltage of 15 V is applied to PG and V_{GG} pins in the order. Apply a voltage of 15 V to the SUB pin and ground pins other than those under test.
4) Current flowing to the ground when V_L pin is grounded, GND and SUB pins are open and a voltage of 27 V is applied to other pins.

5. Current flowing to the ground when a voltage of 55 V is applied to the SUB pin. In this case ground pins other than those under test.

Clock Voltage Conditions
Clock voltage

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Read clock voltage	V_{VT}	13.0		15.0	V	Note 1
Vertical transfer clock voltage	V_{VHH}			1.3	V	Note 2
	V_{VH}	-0.5		0.7	V	
	$V_{\phi V}$	8.0			V	
	V_{VLL}	-10.5			V	
Horizontal transfer clock voltage	V_{HHH}			5.2	V	Note 3
	V_{HL}	-3.0		-1.7	V	
	$V_{\phi H}$	5.2		8.0	V	
	V_{HLL}	-3.0			V	
Output reset clock voltage	V_{PGL}		0		V	Note 4
	$V_{\phi PG}$	7.0		13.0	V	
Substrate clock voltage	$V_{\phi SUB}$	23.0		27.0	V	Note 5

Clock capacitance

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V}$		5000		pF	
Capacitance between vertical transfer clocks	$C_{\phi VV}$		1500		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H}$		180		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Capacitance between output reset clock and GND	$C_{\phi PG}$		10		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		500		pF	

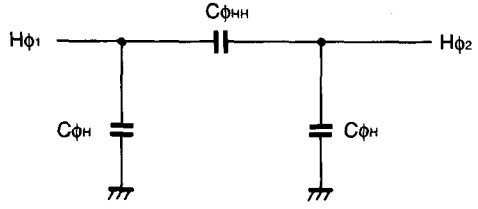


Fig. 4 Equivalent circuit of horizontal transfer clock capacitance

Note) 1. Read clock voltage

1) The symbol "ϕ_L" expresses the voltage level while the read clock "V_T" of the vertical transfer clocks ("$V\phi_1$" and "$V\phi_2$") is set. The maximum value in the read clock waveform is expressed as "ϕ_H".
2) The period in which the voltage level becomes ($\phi_H - \phi_L$)/2 is expressed as "tsr". The voltage levels at "tsr/2" are expressed as "V_{T1}" (at $V\phi_1$) and "V_{T3}" (at $V\phi_3$). The smaller of "V_{T1}" and "V_{T3}" is defined as the read clock voltage "V_{VT}".

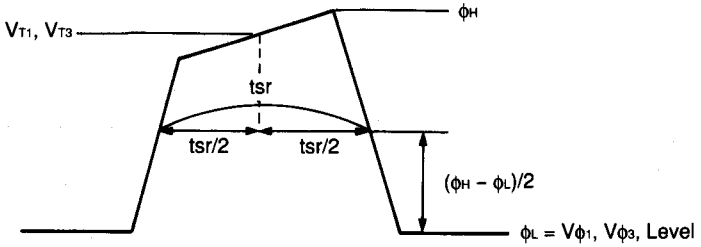


Fig. 5 Read clock wave form

2. Vertical clock voltage (Refer to Fig. 6)

T = 564 ns (with a horizontal driving frequency of 14.19MHz)

1) Definition of the vertical transfer clock amplitude

Level 2T after the rising edge of "$V\phi_3$" is expressed as "V_{3A}".
Level T after the falling edge of "$V\phi_1$" is expressed as "V_{1B}".
Level 2T after the rising edge of "$V\phi_4$" is expressed as "V_{4A}".
Level T after the falling edge of "$V\phi_2$" is expressed as "V_{2B}".
Level 2T after the rising edge of "$V\phi_1$" is expressed as "V_{1A}".
Level T after the falling edge of "$V\phi_3$" is expressed as "V_{3B}".
Level 4T after the rising edge of "$V\phi_2$" is expressed as "V_{2A}".
Level 3T after the falling edge of "$V\phi_4$" is expressed as "V_{4B}".

$V\phi_2$ Level T after the falling edge of "$V\phi_1$" is expressed as "V_{2C}".
$V\phi_3$ Level T after the falling edge of "$V\phi_2$" is expressed as "V_{3C}".
$V\phi_4$ Level T after the falling edge of "$V\phi_3$" is expressed as "V_{4C}".
$V\phi_1$ Level 3T after the falling edge of "$V\phi_4$" is expressed as "V_{1C}".

$\Delta 31 = (V_{3A} + V_{2C}) / 2 - V_{1B}$
$\Delta 42 = (V_{4A} + V_{3C}) / 2 - V_{2B}$
$\Delta 13 = (V_{1A} + V_{4C}) / 2 - V_{3B}$
$\Delta 24 = (V_{2A} + V_{1C}) / 2 - V_{4B}$

The minimum value of these is defined as the vertical transfer clock amplitude "$V\phi_V$".

2) The maximum value among V_{1A}, V_{2A}, V_{3A}, and V_{4A}, is defined as the high level V_{VH} of the clock.
3) The minimum level in a waveform which includes the vertical clock coupling is expressed as "V_{VLL}". "V_{VHH}" expresses the maximum level except in the period where read clock V_T is applied (in $V\phi_1$ and $V\phi_3$ only).

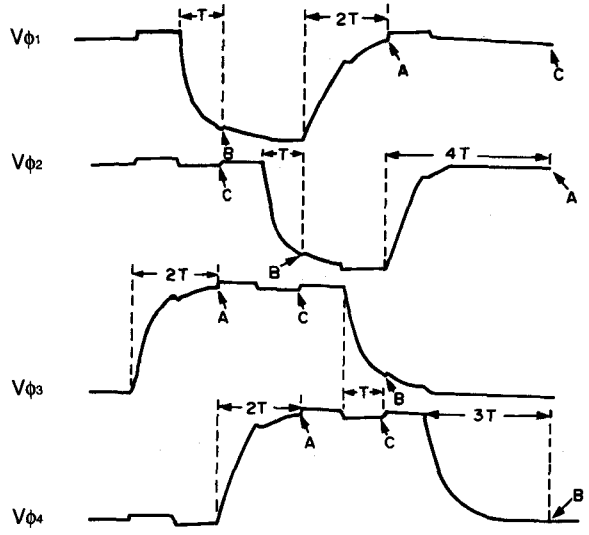


Fig. 6 Vertical transfer clock waveform

3. Horizontal transfer clock voltage
   1) For the horizontal transfer clocks "Hφ1" and "Hφ2", the low-level period is expressed as "thl" and the high-level period is expressed as "thh". The symbol "tho" expresses the overlap period of "thl" and "thh".

   2) The low level at which "thl", "thh" and "tho" satisfy the following time duration is expressed as "H_{1B}" and "H_{2B}".
   And the high level is expressed as "H_{1A}" and "H_{2A}"

      thl ≥ 10 ns, thh ≥ 10 ns, tho ≥ 5 ns

      $\Delta 21 = H_{1A} - H_{2B}$
      $\Delta 12 = H_{2A} - H_{1B}$

   3) The minimum level in the waveform which contains the coupling of the horizontal transfer clocks "Hφ1" and "Hφ2" is expressed as "V_{HLL}" and the minimum level is expressed as "V_{HHH}".

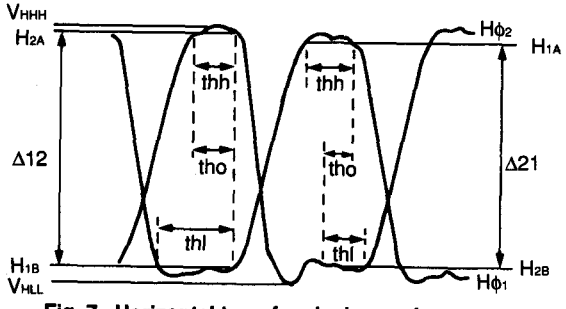


Fig. 7 Horizontal transfer clock waveform

4. Output reset clock voltage
   1) The low level of the output reset clock is to be the GND in the circuit.
   2) The amplitude of the output reset PG clock "$V\phi_{PG}$" is defined as the maximum value of the amplitude which provides a high level period over 10 ns.

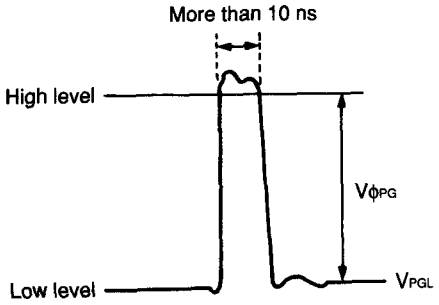


Fig. 8 PG clock waveform

5. Substrate clock voltage
   1) Substrate voltage is expressed as ϕ_L and the maximum value of the substrate clock waveform as ϕ_H.
   2) The period during which voltage level reaches $(\phi_H - \phi_L)/2$ is expressed as tsr. The difference of voltage level with ϕ_L at tsr/2 is defined as substrate clock voltage $V\phi_{SUB}$.

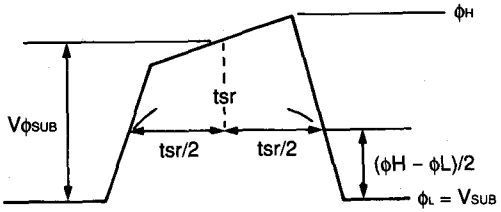


Fig. 9 Substrate clock waveform

Driving Clock Waveform Conditions

1) Definition of ϕ_H (100%) and ϕ_L (0%)
   (1) For the horizontal transfer clocks ($H\phi_1$, $H\phi_2$), output reset clock ($PG\phi$) and vertical transfer clocks ($V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$), the maximum value in the clock waveform which includes no coupling is expressed as "ϕ_H" and the minimum value is expressed as "ϕ_L".
   (2) For the read clock (V_T), the maximum value in the clock waveform is expressed as "ϕ_H"."ϕ_L" expresses the voltage level while the read clock (V_T) of the vertical transfer clocks ($V\phi_1$, $V\phi_3$) is applied.
   (3) For the substrate clock ($SUB\phi$), the maximum value in the clock waveform is expressed as "ϕ_H" and the substrate voltage (V_{SUB}) as "ϕ_L".
2) Standard driving clock waveform conditions (Typ.)

Horizontal drive frequency: 14.19MHz

Clock (Symbol)	twh	twl	tr	tf	Unit	Remarks
$H\phi_1$	18	33.7	10	8	ns	Imaging period
$H\phi_2$	18	33.7	10	8		
$H\phi_1$	4.9		0.10	0.01	µs	Parallel-serial converting period
$H\phi_2$		4.9	0.10	0.01		
ϕ_{PG}	12	53.7	2	2	ns	
$V\phi_1/V\phi_2$	61.6	1.6	0.1	0.1	µs	Imaging period
$V\phi_3/V\phi_4$	2.8	60.45	0.05	0.1		
$V\phi_T$	2.4		0.2	0.1		Reading period
SUBϕ	1.0		0.08	0.1	µs	Electron sweep-off period

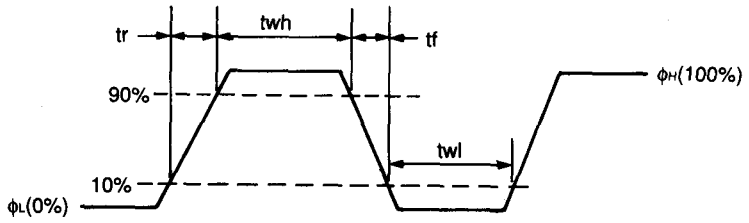


Fig. 10 Clock waveform

Imaging Characteristics

(For the testing circuit, see Fig. 11.)
Ta=25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Testing method	Remarks
Sensitivity	Sg	200	300		mV	1	
Output saturation signal	Vsat	500			mV	2	Note
Blooming margin		800			times	3	Note
Smear	Smr		0.005	0.012	%	4	
Video signal shading	Svg			20	%	5	
Dark signal output	Vdt			2	mV	6	Ta=55°C
Dark signal shading	ΔVdt			1	mV	7	Ta=55°C

Note) Saturation signal and blooming margin are guaranteed only when the substrate voltage has been set to the voltage indicated on the back of the imaging device.

Test Methods

Conditions

1) The conditions required to drive the device through out the following tests should be within the range of bias conditions and clock voltage conditions. The test circuit shown in Fig. 11 is used for evaluating and testing the characteristics.
2) Blemishes are excluded in the following tests and the signal output is based on the optical black level unless otherwise specified. The value obtained at the output test point becomes the test value.

Standard imaging conditions

1) Shoot the PTB-100 pattern box (luminance 706 Nit, color temperature 3200K) with no pattern, using a FUJINON H6 × 12.5D (F1.4) lens at F8. Use the CM-500S (1.0 mmt) filter to cut off infrared rays.
2) Shoot a light source (color temperature 3200K) which provides a uniform brightness within 2% over the whole screen.

1. Set the standard imaging condition 1) and test signal voltage (Sg) at the center of the screen.

2. Set to standard imaging condition 2) and adjust the light intensity to about eight times the intensity obtained at a signal voltage of 200 mV. Them obtain the minimum value of the signal voltage over the whole screen.

3. Set to imaging condition 2) and adjust the light intensity to about 800 times the intensity obtained at a signal voltage of 200 mV. At that time make sure there is no blooming and the vertical resistor is not saturated.

4. Set to standard imaging condition 2) and adjust the light intensity so that the signal voltage (V_{SG}) becomes 200 mV. Then, turn V_T off and obtain the maximum value of the signal voltage "V_{SM}" after stopping the horizontal resistor 50 H at the effective picture element.

$$Smr = \frac{V_{SM}}{V_{SG}} \times \frac{1}{50} \times \frac{1}{10} \times 100\ (\%)$$

(Converted into 1/10 V system)

5. Set to standard imaging condition 2) and test the signal voltage to obtain maximum (V_{SG} max) and minimum (V_{SG} min) values.
The light intensity is adjusted so that the average value of the signal voltage (V_{SG} average) becomes about 200 mV.

$$Svg = \frac{V_{SG}\,max - V_{SG}\,min}{V_{SG}\ average} \times 100\ (\%)$$

6. Measure the mean voltage of the dark current signal based on the horizontal free-transfer level in a light-shaded condition with an ambient temperature of 55°C.

7. Following measurement 6, test the dark current signal voltage to obtain the maximum (Vdmax) and minimum (Vdmin) values. Spot blemishes are ignored in this test.

Electrical Characteristics Test Circuit

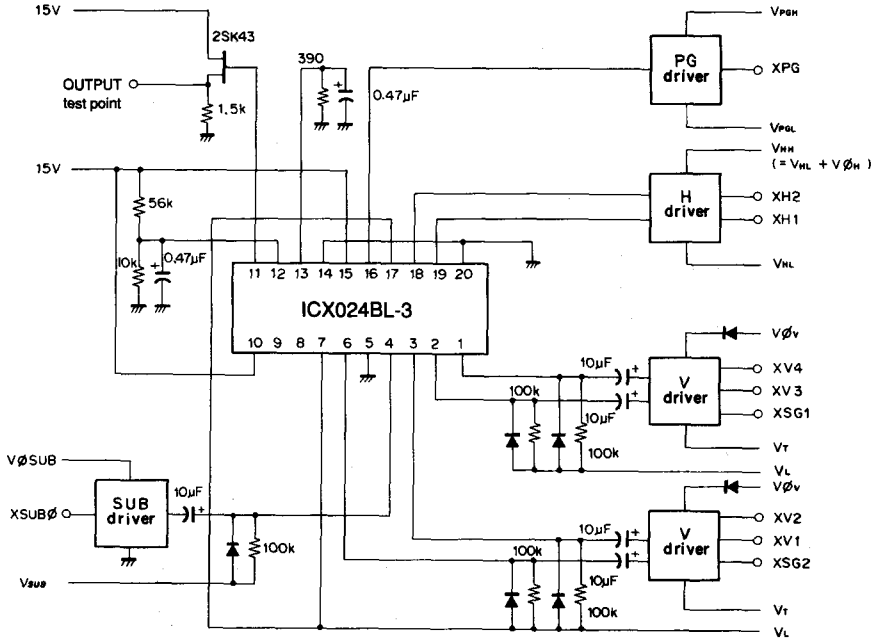
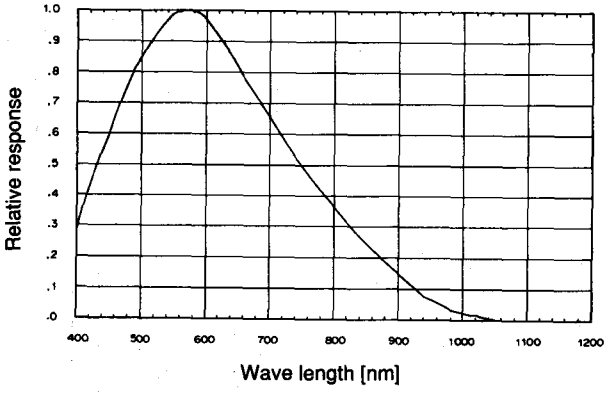


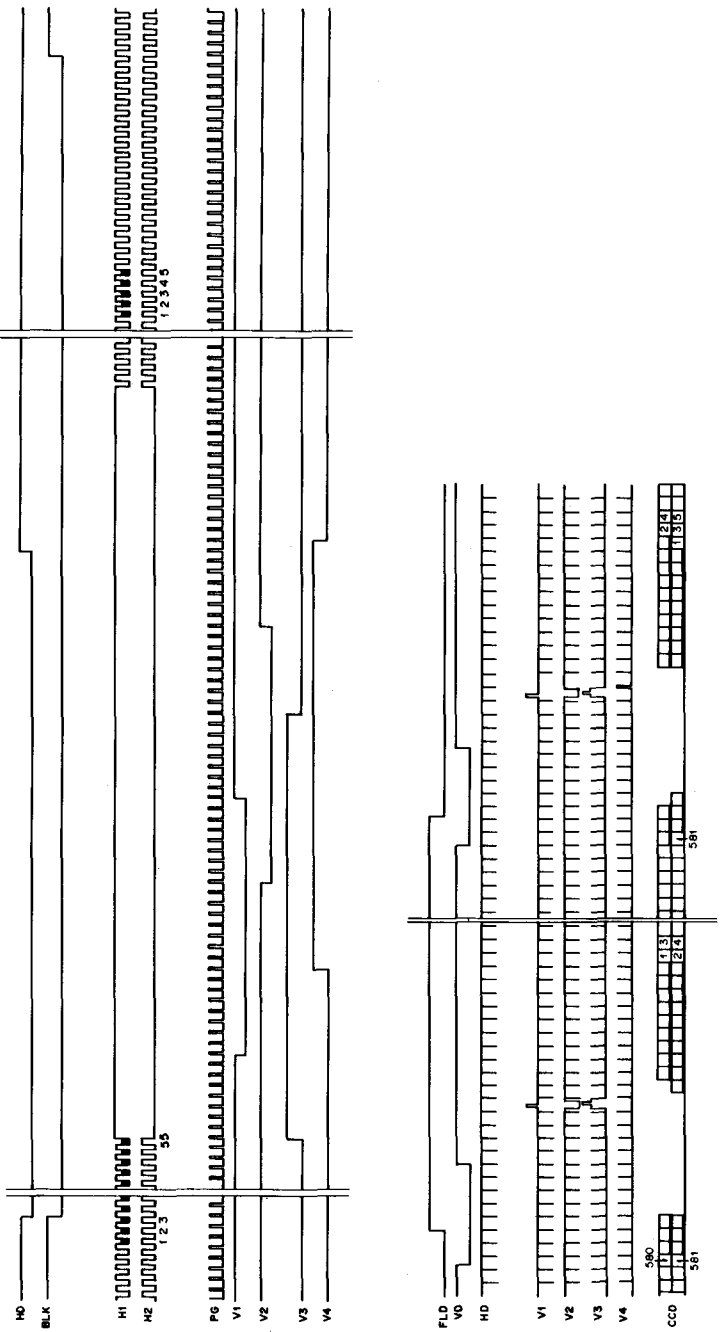
Fig. 11

Spectrum Sensitivity Characteristics (Typical example, excluding illuminant characteristics)

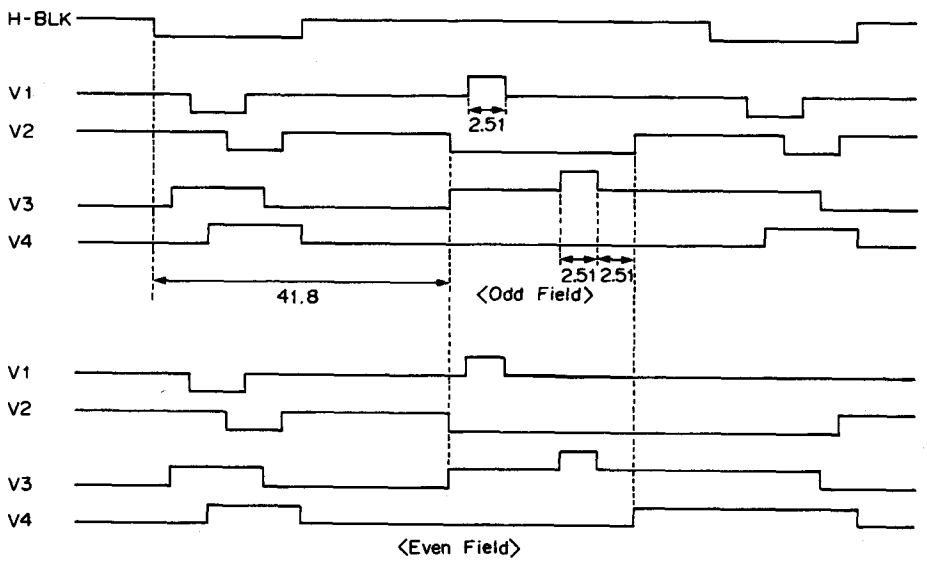
With a Fujinon lens H6 × 12.5D



Driving Pulse Timing Chart

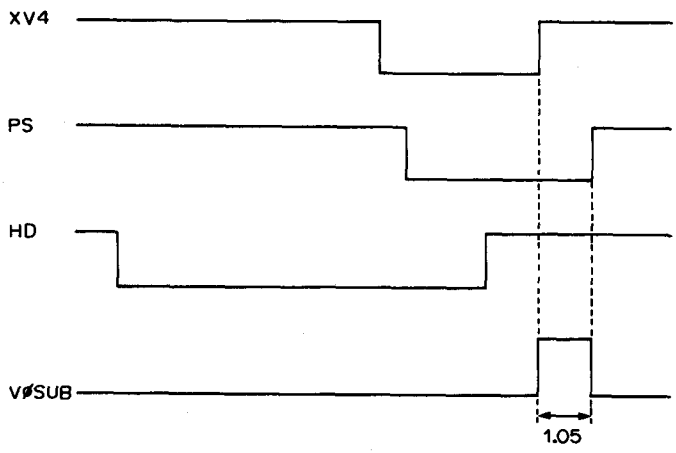


Sensor Read Out Clock Timing Chart



Unit: µs

Charge Drain Clock Timing Chart In Shutter Mode



Unit: µs

Handling Instructions

1. On electric screening
   To prevent damage to the CCD image sensor by static electricity, handle as follows.
   a) Either handle the device with bare hands, or use antistatic gloves and clothes. Conductive shoes are also required.
   b) Use a ground lead when directly touching the device.
   c) Cover the floor and working table with a conductive mat or equivalent to avoid static electricity.
   d) Discharge using ionized air is recommended.
   e) To ship the mounted boards, use cartons with antistatic properties.

2. On soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder-dipping of DIP in a mounting furnace may break glass. Use a grounded 30 W soldering iron at each pin for less than 2 seconds. When adjusting or removing soldered parts, let the CCD cool sufficiently.
   c) Do not use any solder-aspirating equipment to remove the imaging device. Should an electric solder-aspiration device be used, use only a device of the zero-cross type control system and be sure to ground the controller.

3. On contamination
   a) Keep the operation room clean (Class 1000 will be expected).
   b) Do not touch the glass surface and avoid contact with foreign objects. Blow off any dust from the surface with a blower. (Ionized air is recommended to blow off any object sticking through static electricity.)
   c) Wipe off grass spots with an applicator moistened with ethanol. Be careful not to scratch the surface.
   d) To eliminate contamination, store the device in an exclusive case. During transportation minimize the difference in temperatures between locations to avoid moisture condensation.
   e) When a protection tape has been affixed for shipment, remove it just before use after applying appropriate antistatic measures. Do no reuse the removed tape.

4. Do not subject the device to light sources for extended periods. If a color element is subjected to strong light ray for an extended period, the color filter will be discolored. (Store the device in a dark place.)

5. Usage or storage of the device in high temperature or high humidity may seriously affect the performance.

6. The CCD image sensor is a high-precision optical part, that should not be subjected to mechanical shocks.

7. System data write complete ROM (with flow compensation address included)
   System data write complete ROM in equal quantity as ICX024BL-3 is attached.
   Analog those ROM with address for flow compensation have serial No. stuck on.
   Use in conjunction with ICX024BL-3 pairing the same serial No..

SONY®

ICX026BLA

1/2 inch CCD Image Sensor for EIA B/W Camera

Description

The ICX026BLA is an interline transfer CCD solid-state imager suitable for EIA 1/2 inch B/W video cameras. High sensitiveness is achieved through the adoption of HAD (Hole Accumulation Diode) sensors.

This chip features a field integration read out system, an electronic shutter with variable charge storage time and 20pin Cer-DIP package.

Features

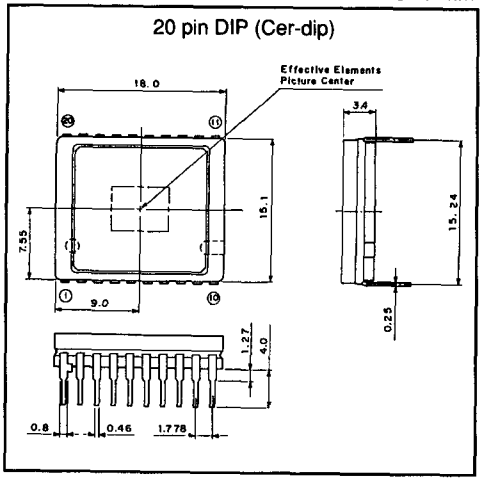
- High sensitivity (+6 dB compare with ICX026AL)
- Optical size 1/2 inch format
- Field integration read out system
- Low dark current
- Horizontal register 5V drive
- High antiblooming
- Low smear
- Variable speed electronic shutter

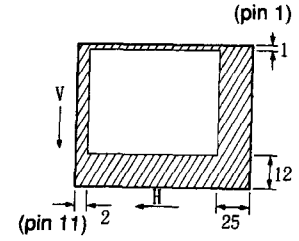
Device Structure

- Number of effective pixels 510 (H) × 492 (V)
- Number of total pixels 537 (H) × 505 (V)
- Interline transfer CCD image sensor
- Chip size 7.84 mm (H) × 6.40 mm (V)
- Unit cell size 12.7 µm (H) × 9.8 µm (V)
- Optical black
  - Horizontal (H) direction Front 2 pixels Rear 25 pixels
  - Vertical (V) direction Front 12 pixels Rear 1 pixels
- Number of dummy bits
  - Horizontal 16
  - Vertical 1 (even field only)
- Substrate material silicon

Package Outline

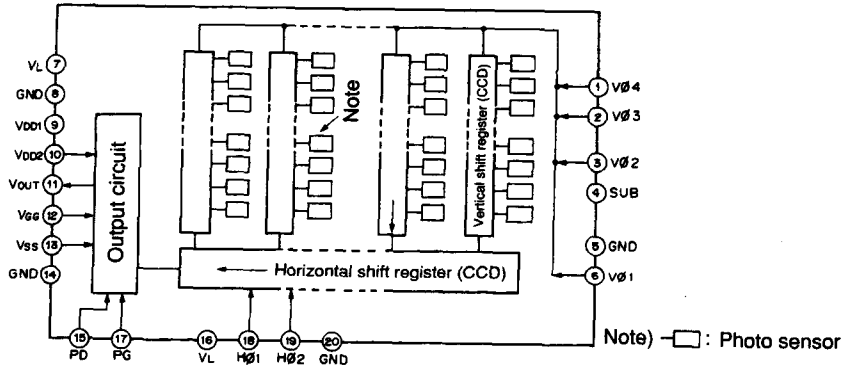
Unit: mm





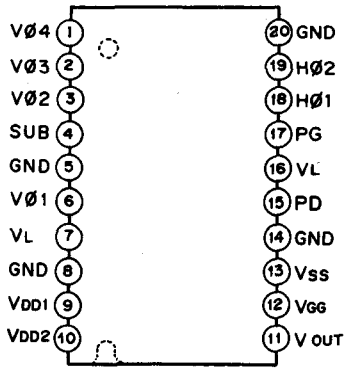
Optical black position (Top View)

Block Diagram



E91632-YA

Pin Configuration (Top View)



Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	11	VOUT	Signal output
2	Vφ3	Vertical register transfer clock	12	VGG	Output amplifier gate bias
3	Vφ2	Vertical register transfer clock	13	VSS	Output amplifier source
4	SUB	Substrate (Overflow drain)	14	GND	GND
5	GND	GND	15	PD	Precharge drain bias
6	Vφ1	Vertical register transfer clock	16	VL	Protective transistor bias
7	VL	Protective transistor bias	17	PG	Precharge gate clock
8	GND	GND	18	Hφ1	Horizontal register transfer clock
9	VDD1	Output amplifier drain supply	19	Hφ2	Horizontal register transfer clock
10	VDD2	Output amplifier drain supply	20	GND	GND

Absolute Maximum Ratings

• Substrate voltage	SUB – GND	−0.3 to +55	V
• Supply voltage	VDD1, VDD2, PD, VOUT, VSS – GND	−0.3 to +18	V
	VDD1, VDD2, PD, VOUT, VSS – SUB	−55 to +10	V
• Clock input voltage	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – GND	−15 to +20	V
	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – SUB	−65 to +10	V
• Voltage difference between vertical clock input pins		15	V*
• Voltage difference between horizontal clock input pins		17	V
• Hφ1, Hφ2 – Vφ4		−17 to +17	V
• PG, VGG – GND		−10 to +15	V
• PG, VGG – SUB		−55 to +10	V
• VL – SUB		−65 to +0.3	V
• Beside GND, SUB, VL – VL		−0.3 to +30	V
• Storage temperature		−30 to +80	°C
• Operating temperature		−10 to +55	°C

***Note)** +27 V (Max.) when clock width < 10 μs, duty factor < 0.1%

Bias Conditions

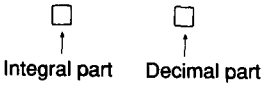
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD1}, V_{DD2}	14.55	15.0	15.45	V	V_{DD1} = V_{DD2}
Precharge drain voltage	V_{PD}	14.55	15.0	15.45	V	V_{PD} = V_{DD1} = V_{DD2}
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	V_{SS}	Ground through 680 Ω resistor				±5%
Substrate voltage adjustment range	V_{SUB}	7		19	V	*1
Fluctuation range after substrate voltage adjustment	V_{SUB}	-3		+3	%	
Protective transistor bias	V_L	*2				

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		2.5		mA	I_{DD} = I_{DD1} + I_{DD2}
Input current	I_{IN1}			1	μA	*3
Input current	I_{IN2}			10	μA	*4

Note) *1. Substrate voltage (V_{SUB}) setting value display.
Substrate voltage setting value is displayed at the back of the device through a code address. Adjust so as to obtain the displayed voltage at SUB pin.

V_{SUB} code address – two digits display



The relation between code address of integral part and actual numerical values.

Code address of integral part	7	8	9	A	B	C	D	E	F	G	H	I	J
Numerical Value	7	8	9	10	11	12	13	14	15	16	17	18	19

<Example> F5 → 15.5 (V)

*2. V_L setting is V_{VL} of the vertical transfer clock waveform.

*3. 1) Current to earth when 18V is applied to pins V_{DD1}, V_{DD2}, V_{OUT}, V_{SS} and SUB pin. However, pins that are not tested are grounded.
2) Current to earth when 20V is sequentially applied to pins Vφ1, Vφ2, Vφ3, Vφ4, Hφ1 and Hφ2. However, 20V is applied to SUB while pins that are not tested are grounded.
3) Current to earth when 15V is sequentially applied to pins PG and V_{GG}. However, 15V is applied to SUB while pins that are not tested are grounded.

*4. 1) Current to earth when 55V is applied to SUB pin. Pins that are not tested are grounded.
2) Current to earth when V_L is grounded, GND and SUB are open and 30V is applied to other pins.

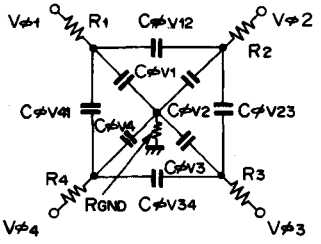
Clock Voltage Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	No.	Remarks
Read out clock voltage	V_{VT}	14.3	15.0	15.7	V	2,6	*1
Vertical transfer clock voltage *2	V_{VH1},V_{VH2},V_{VH3},V_{VH4}	−0.2	0	0.2	V	1,2,3,6	V_{VH}=(V_{VH1}+V_{VH2})/2
	V_{VL1},V_{VL2},V_{VL3},V_{VL4}	−9.6	−9.0	−8.3	V	1,2,3,6	V_{VL}=(V_{VL3}+V_{VL4})/2
	$V_{\phi V}$	8.1	9.0	9.8	V	1,2,3,6	$V_{\phi V}$=V_{VHn}-V_{VLn} (n=1 to 4)
	$\lvert V_{VH1} - V_{VH2} \rvert$			0.2	V	3,6	
	$V_{VH3} - V_{VH}$	−0.4		0.1	V	2,3,6	
	$V_{VH4} - V_{VH}$	−0.4		0.1	V	1,3,6	
	V_{VHH}			0.8	V	1,2,3,6	High level coupling
	V_{VHL}			1.0	V	1,2,3,6	High level coupling
	V_{VLH}			0.8	V	1,2,3,6	Low level coupling
	V_{VLL}			0.8	V	1,2,3,6	Low level coupling
Horizontal transfer clock voltage	$V_{\phi H}$	4.7	5.0	5.3	V	18,19	*3
	V_{HL}	−0.05	0	0.05	V	18,19	
Precharge gate clock voltage	$V_{\phi PG}$	8.0		11.5	V	17	*4
	V_{PGL}	−0.1	0	0.1	V	17	
Substrate clock voltage	$V_{\phi SUB}$	23.0	32.0	34.0	V	4	*5

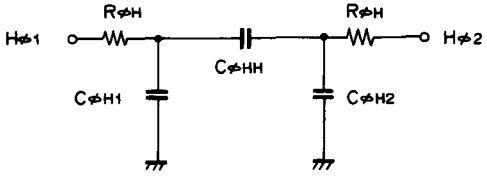
Note) *1. See Fig. 1.
*2. See Fig. 2.
*3. See Fig. 3.
*4. See Fig. 3.
*5. See Fig. 4.

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$, $C_{\phi V3}$		1000		pF	
Capacitance between vertical transfer clock and GND	$C_{\phi V2}$, $C_{\phi V4}$		1200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$, $C_{\phi V34}$		1200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V23}$, $C_{\phi V41}$		750		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, $C_{\phi H2}$		70		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Capacitance between precharge gate clock and GND	$C_{\phi PG}$		8		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		400		pF	
Vertical transfer clock serial resistor	R_1,R_2,R_3,R_4		33		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock serial resistor	$R_{\phi H}$		10		Ω	



Vertical transfer clock equivalent circuit



Horizontal trasfer clock equivalent circuit

Drive Clock Waveform Conditions

1. Read out clock waveform

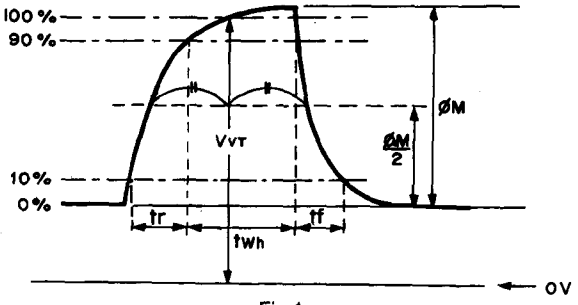


Fig.1

2. Vertical transfer clock waveform

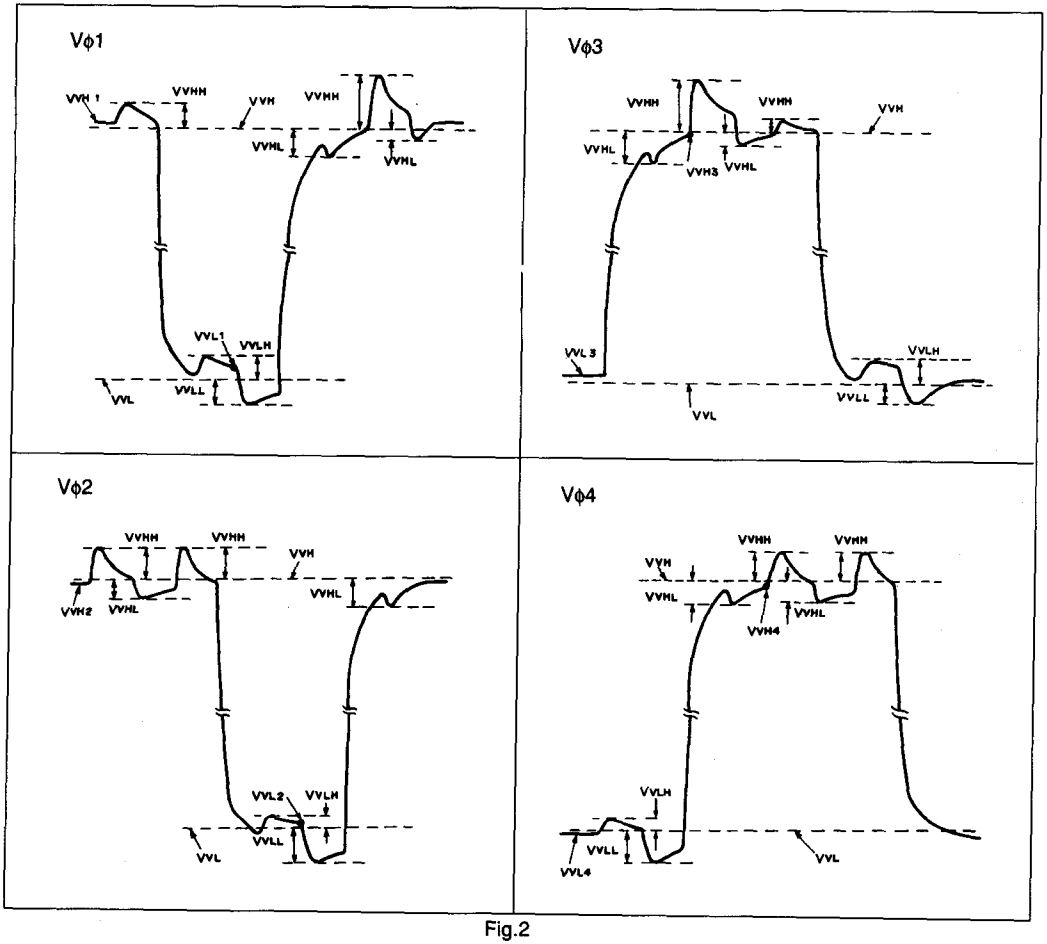


Fig.2

3. Horizontal transfer clock waveform/Precharge gate clock waveform

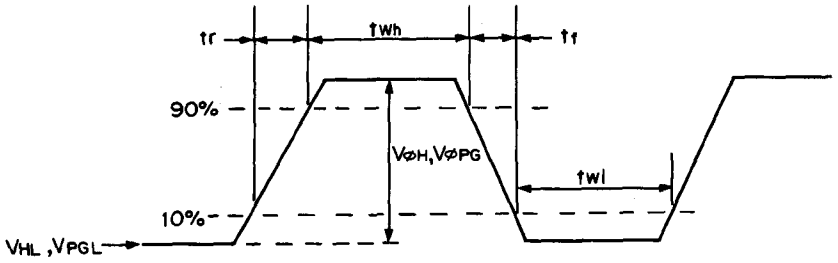


Fig. 3

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max	Min.	Typ.	Max	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	V_T	1.5	1.85							0.5			0.5	µs	During read out
Vertical transfer clock	Vφ1,Vφ2,Vφ3,Vφ4									0.45	0.015		0.25	µs	*
Horizontal transfer clock	Hφ	37	41		38	42			12	15		10	15	ns	During imaging
Horizontal transfer clock	Hφ1		5.6						0.012			0.01		µs	During parallel serial conversion.
Horizontal transfer clock	Hφ2					5.6			0.012			0.01		µs	During parallel serial conversion.
Precharge gate clock	φPG	15	17		75	81			4			3		ns	
Substrate clock	φSUB	1.5	2.1							0.5			0.5	µs	During charge drain.

*Note) When vertical transfer clock driver CXD1250 is in use.

4. Substrate clock waveform

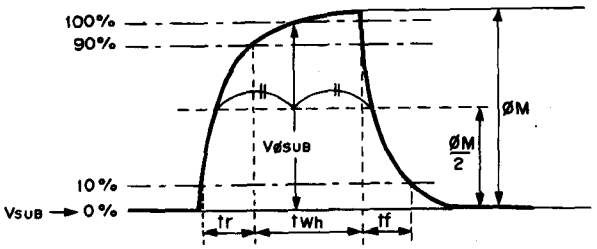


Fig. 4

Operating Characteristics

Ta = 25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	240	320		mV	1	
Saturation signal	Vsat	500			mV	2	Ta=55°C
Smear	SM		0.007	0.015	%	3	
Blooming margin		1000			times	4	
Video signal shading	SH			20	%	5	Zone 0, I
				25	%	5	Zone 0 to II'
Dark signal	Vdt			2	mV	6	Ta=55°C
Dark signal shading	ΔVdt			1	mV	7	Ta=55°C
Flicker	F			2	%	8	
Lag	ΔVlag			0.5	%	9	

Test Method

Test conditions

①Through the following tests the substrate voltage should set to the value displayed on the device, while the device drive conditions should be kept within the range of the bias and clock voltage conditions.

②Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OPB) is set as the reference. The values obtained at A point in the figure of the Drive Circuit are utilized.

Definition of standard imaging conditions

①Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 cd/m^2 3200K Halogen source), at F8 with a typical test lens, and CM-500S (t=1.0 mm) for IR cut filter.

②Standard imaging condition II: Use a light source with uniformity within 2%, color temperature of 3200K and CM-500S (t=1.0 mm) as IR cut filter. The light intensity is adjusted in accordance with the average signals (V_A) indicated in each item.

1. Set to standard imaging condition I and measure signal output (S) at the center of the screen.

2. Set to standard imaging condition II. Adjust light intensity to 10 times when the average signal V_A=150mV. Then test signal Min. Value.

3. Set to standard imaging condition II. Adjust light intensity to 500 times when the average signal V_A=150mV. Stop Read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the Max. value V_{SM} of signal output.

   $SM = (V_{SM}/V_A) \times 1/500 \times 1/10 \times 100$ (%) ($1/10$V)

4. Set to standard imaging condition II. Adjust light intensity to 1000 times when the average signal V_A=150mV. Then check that there is no blooming.

5. Video signal shading SH
   Set to standard imaging condition II. Test signal Max. (Vmax) and Min. (Vmin) values. Adjust light intensity to obtain an average signal (V_A) of about 150mV.

   $SH = (Vmax - Vmin)/V_A \times 100$ (%)

6. Test the average signal when the device ambient temperature is at 55°C and light is obstructed with horizontal idle transfer level as reference.

7. Following test 6, test Max. (Vd max) and Min. (Vd min) of signal output. Only keep spot defects out of this range.

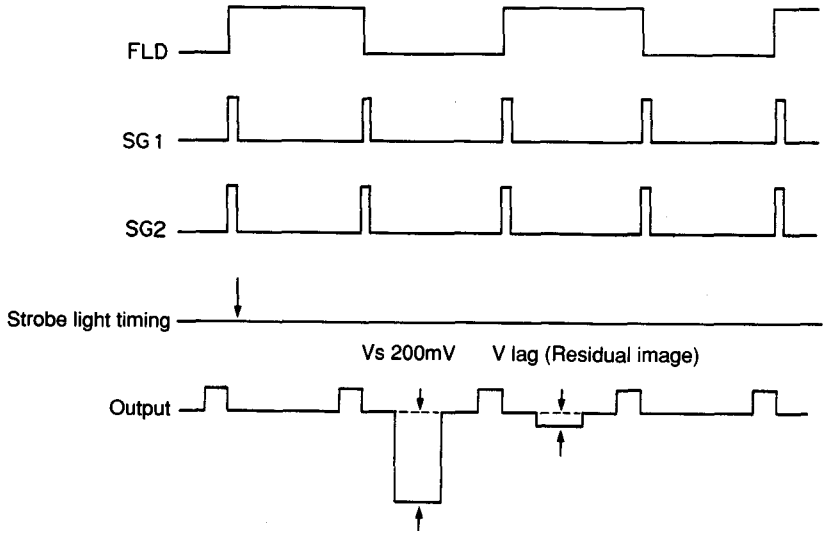
   $\Delta Vdt = Vd\ max - Vd\ min$

8. Set to imaging condition II. Test the output signal difference (ΔVf) between even and odd field. At that time, adjust light intensity to obtain an average signal (V_A) of about 150 mV.

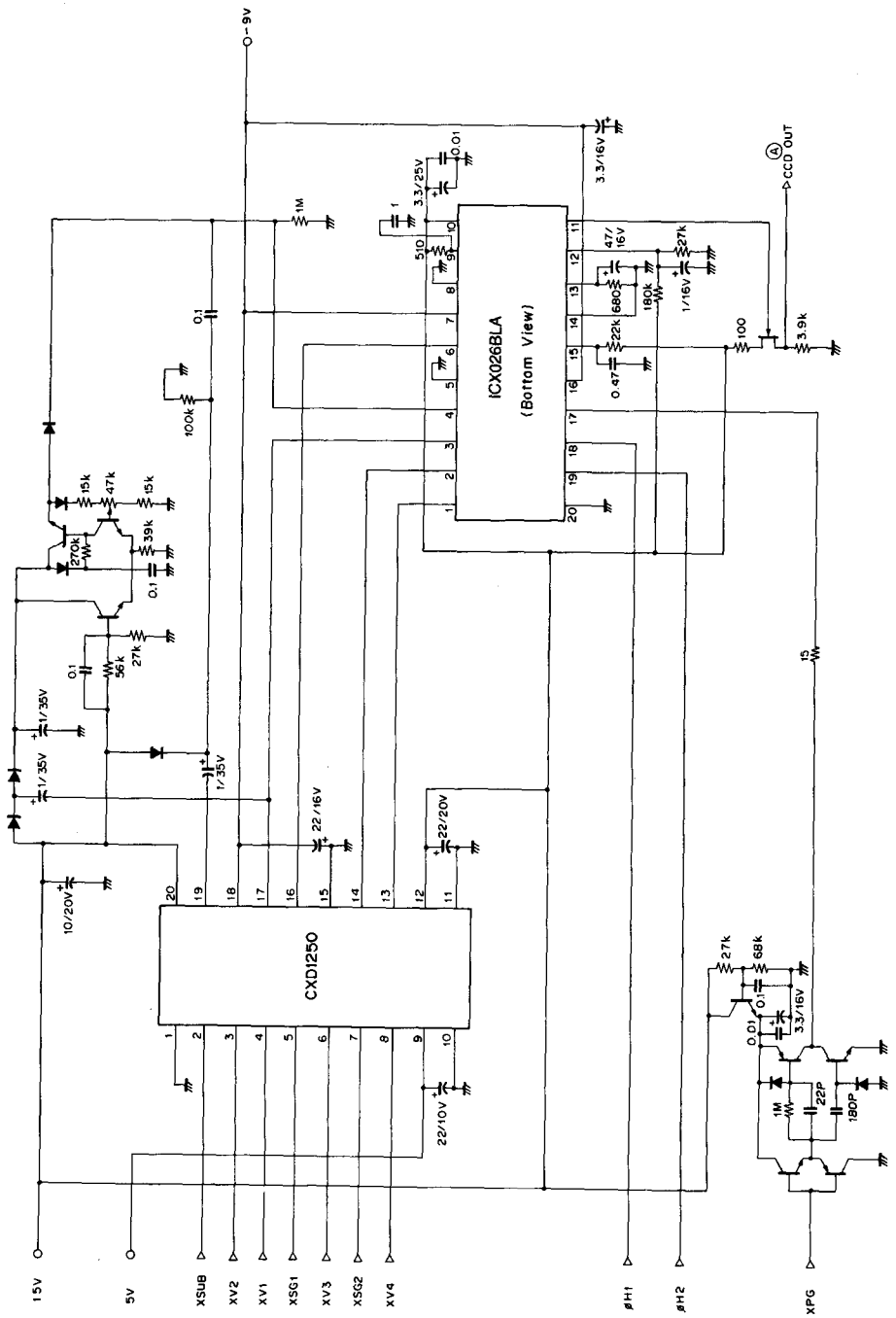
   $F = (\Delta Vf/V_A) \times 100$ (%)

9. Light a stroboscopic tube with the following timing and test the residual image.

   $\Delta Vlag = (Vlag/Vs) \times 100$ (%)

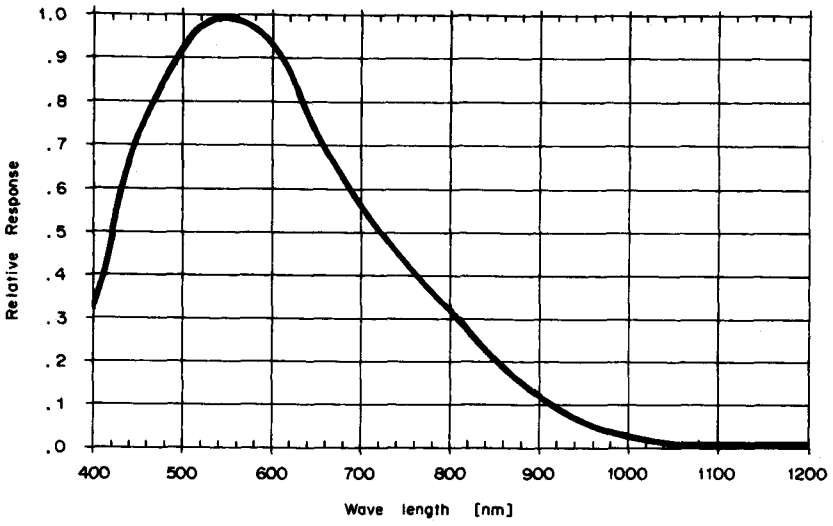


Drive Circuit

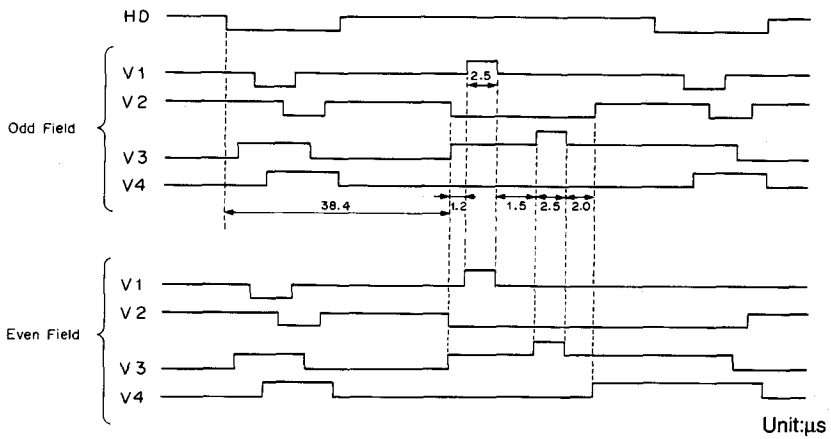


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

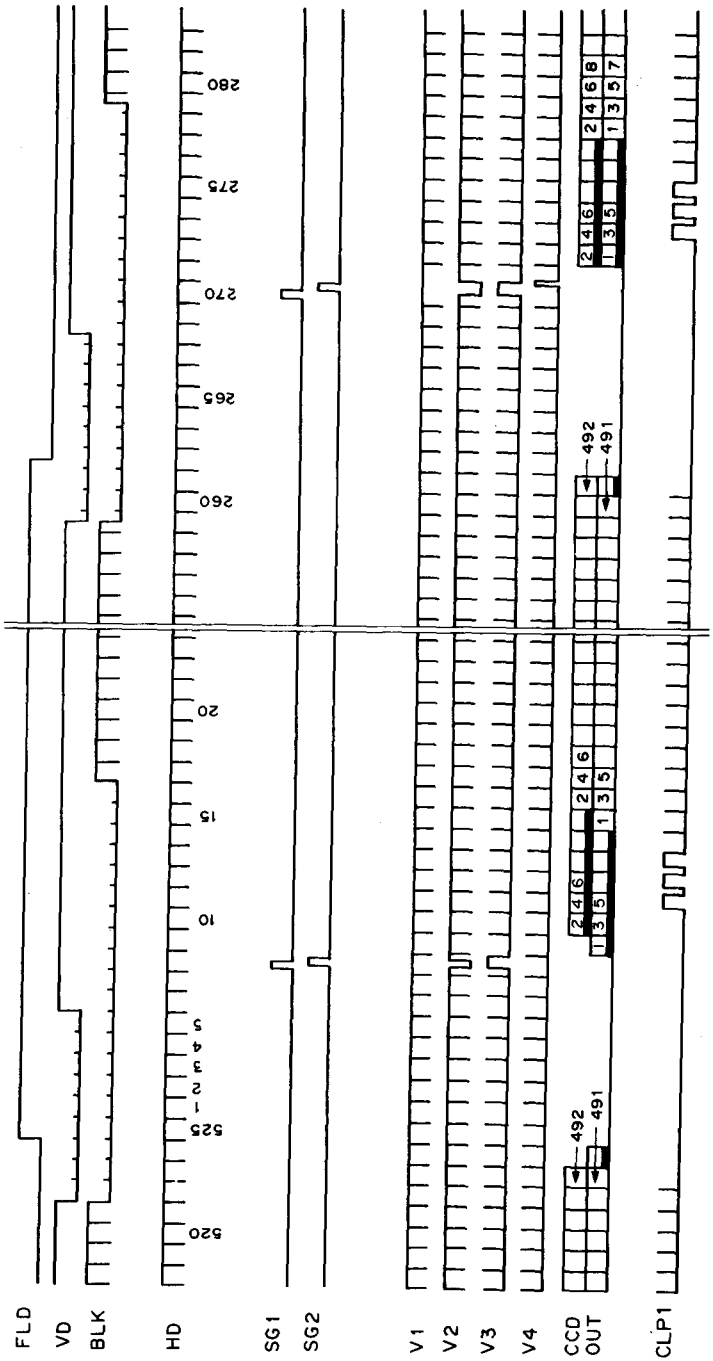
Spectral Sensitivity Characteristics
(Excluding light source characteristics, including lens characteristics)



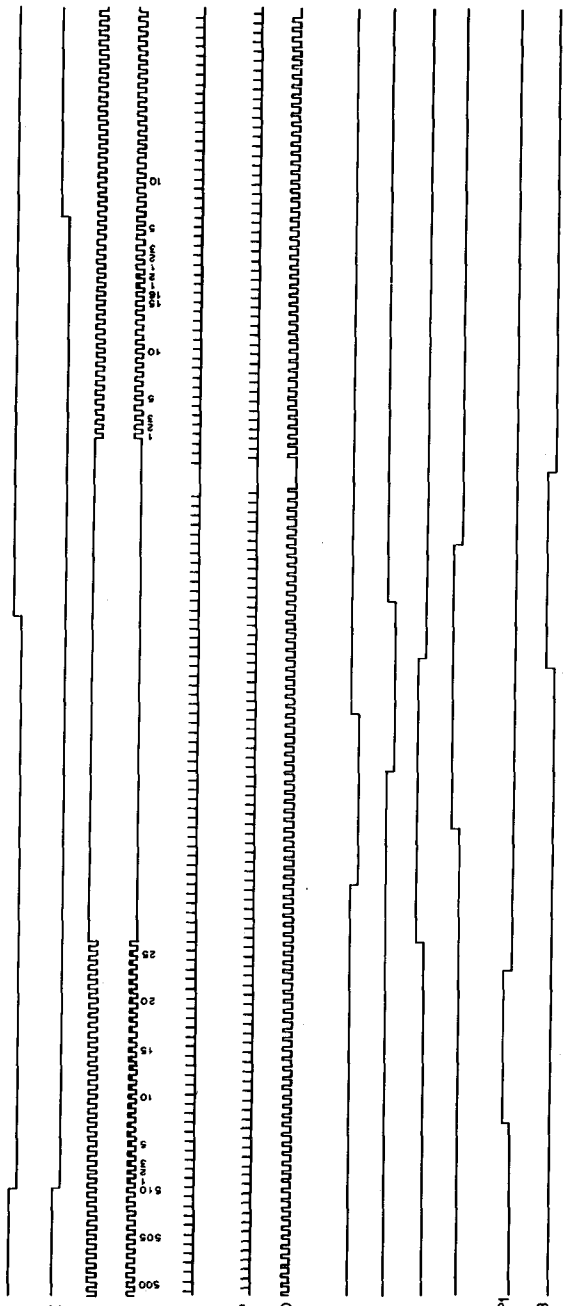
Using read out clock timing chart



Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



During electronic shutter operation

Handling Instructions

1) Static charge prevention
CCD image sensor are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount cool sufficiently.
c) To dismount an imaging device do not use a solder pult. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

SONY

ICX038ALA

1/2 inch CCD Image Sensor for EIA B/W Camera

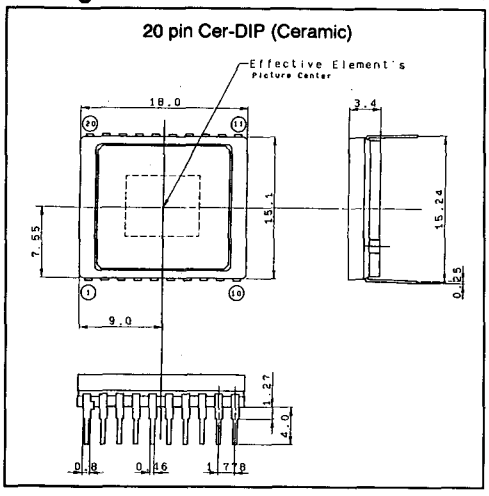
Description

ICX038ALA is an interline transfer CCD solid-state imager suitable for EIA 1/2 inch B/W video cameras. High sensitiveness is achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.

This chip features a field integration read out system, an electronic shutter with variable charge-storage time and 20 pin Cer-DIP package.

Package Outline

Unit : mm

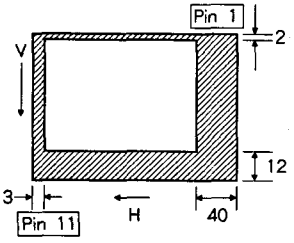


Features

- High image, high sensitivity and low dark current
- Consecutive various speed shutter
  1/60sec. (Typ.), 1/100sec. to 1/10000sec.
- Low smear
- High antiblooming
- Horizontal register 5V drive
- Reset gate 5V drive

Device Structure

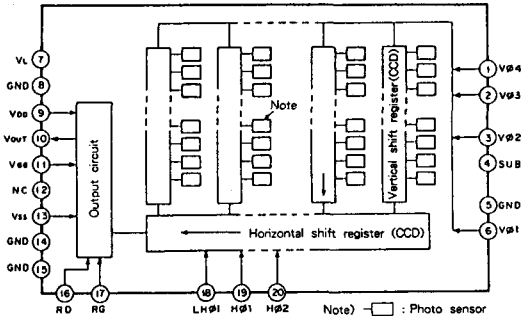
- Optical size 1/2 inch format
- Number of effective pixels 768 (H) ×494 (V) Approx. 380k pixels
- Number of total pixels 811(H) ×508 (V) Approx. 410k pixels
- Interline transfer CCD image sensor
- Chip size 7.95mm (H) ×6.45mm (V)
- Unit cell size 8.4 μm (H) ×9.8 μm (V)
- Optical black Horizontal (H) direction Front 3 pixels Rear 40 pixels
  Vertical (V) direction Front 12 pixels Rear 2 pixels
- Number of dummy bits Horizontal 22
  Vertical 1 (even field only)
- Substrate material silicon



Optical black position (Top View)

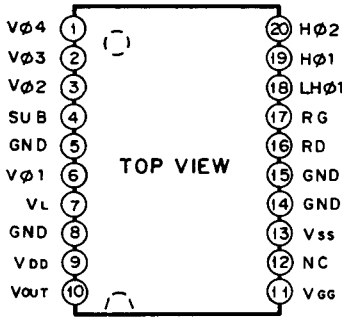
E91705 – ST

Block Diagram



Pin Configuration

(Top View)



Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	$V\phi_4$	Vertical register transfer clock	11	V_{GG}	Output amplifier gate bias
2	$V\phi_3$	Vertical register transfer clock	12	NC	
3	$V\phi_2$	Vertical register transfer clock	13	Vss	Output amplifier source
4	SUB	Substrate (Overflow drain)	14	GND	GND
5	GND	GND	15	GND	GND
6	$V\phi_1$	Vertical register transfer clock	16	RD	Reset drain bias
7	V_L	Protective transistor bias	17	RG	Reset gate clock
8	GND	GND	18	$LH\phi_1$	Horizontal register final stage transfer clock
9	V_{DD}	Output amplifier drain supply	19	$H\phi_1$	Horizontal register transfer clock
10	V_{OUT}	Signal output	20	$H\phi_2$	Horizontal register transfer clock

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB-GND		–0.3 to +55	V	
Supply voltage	V_{DD}, V_{RD}, V_{OUT}, Vss – GND	–0.3 to +18	V	
	V_{DD}, V_{RD}, V_{OUT}, Vss – SUB	–55 to +10	V	
Clock input voltage	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$ – GND	–15 to +20	V	
	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$ – SUB	to +10	V	
Voltage difference between vertical clock input pins		to+15	V	* (Max.)
Voltage difference between horizontal clock input pins		to+17	V	
$H\phi_1$, $H\phi_2$ – $V\phi_4$		–17 to +17	V	
$LH\phi_1$, RG, V_{GG} – GND		–10 to +15	V	
$LH\phi_1$, RG, V_{GG} – SUB		–55 to +10	V	
V_L – SUB		–65 to +0.3	V	
Beside GND, SUB-V_L		–0.3 to +30	V	
Storage temperature		–30 to +80	℃	
Operating temperature		–10 to +60	℃	

* +27V (Max.) when clock width < 10 μs, duty factor < 0.1%.

Bias Conditions

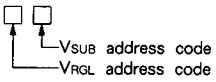
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD}	14.55	15.0	15.45	V	
Reset drain voltage	V_{RD}	14.55	15.0	15.45	V	$V_{RD}=V_{DD}$
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	V_{SS}	Ground through 390 Ω resistor				± 5%
Substrate voltage adjustment range	V_{SUB}	9.0		18.5	V	*2
Fluctuation range after substrate voltage adjustment	Δ V_{SUB}	–3		+3	%	
Reset gate clock voltage adjustment range	V_{RGL}	1.0		4.0	V	*2 *6
Fluctuation range after reset gate clock voltage adjustment	Δ V_{RGL}	–3		+3	%	
Protective transistor bias	V_L	*3				

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		5		mA	
Input current	I_{IN1}			1	μA	*4
Input current	I_{IN2}			10	μA	*5

*2 Substrate voltage (V_{SUB}) • reset gate clock voltage (V_{RGL}) setting value display.
Setting values of substrate voltage and reset gate clock voltage are displayed at the back of the device through a code address. Adjust substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) to the displayed voltage. Fluctuation range after adjustment is ± 3%.

V_{SUB} code address–1 digit display
V_{RGL} code address–1 digit display



Code addresses and actual numerical values correspond to each other as follows.

V_{RGL} address code	1	2	3	4	5	6	7
Numerical value	1.0	1.5	2.0	2.5	3.0	3.5	4.0

V_{SUB} address code	E	f	G	h	J	K	L	m	N	P	Q	R	S	T	U	V	W	X	Y	Z
Numerical value	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5

<Example> "5L" → V_{RGL}=3.0V
V_{SUB}=12.0V

*3 V_L setting is the V_{VL} voltage of the vertical transfer clock waveform.

*4 1. Current to each pin when 18V is applied to V_{DD}, V_{OUT}, Vss and SUB pins, while pins that are not tested are grounded.
2. Current to each pins when 20V is applied sequentially to V φ 1, V φ 2, V φ 3, V φ 4, H φ 1 and H φ 2, while pins that are not tested are grounded. However, 20V is applied to SUB.
3. Current to each pins when 15V is applied sequentially to pins RG, LH φ 1 and V_{GG}, while pins that are not tested are grounded. However, 15V is applied to SUB.
4. Current to V_L pin when it is grounded, while 30V is applied to all pins except pins that are not tested. However, GND and SUB pins are kept open.

*5 Current to SUB pin when 55V is applied to SUB pin, while pins that are not tested are grounded.

Clock Voltage Conditions

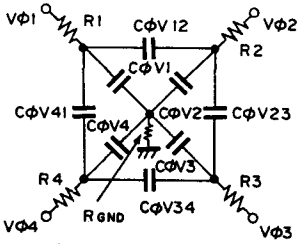
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Read out clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	–0.05	0	0.05	V	2	$V_{VH}=(V_{VH1}+V_{VH2})/2$
	V_{VH3}, V_{VH4}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	–9.6	–9.0	–8.5	V	2	$V_{VL}=(V_{VL3}+V_{VL4})/2$
	$V\phi_V$	8.3	9.0	9.65	V	2	$V\phi_V=V_{VHn}-V_{VLn}$ (n=1 to 4)
	$\lvert V_{VH1} - V_{VH2} \rvert$			0.1	V	2	
	$V_{VH3}-V_{VH}$	–0.25		0.1	V	2	
	$V_{VH4}-V_{VH}$	–0.25		0.1	V	2	
	V_{VHH}			0.5	V	2	High level coupling
	V_{VHL}			0.5	V	2	High level coupling
	V_{VLH}			0.5	V	2	Low level coupling
	V_{VLL}			0.5	V	2	Low level coupling
Horizontal transfer clock voltage	$V\phi_H$	4.75	5.0	5.25	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
Horizontal final stage transfer clock voltage	V_{LHH}	4.45	5.0	5.55	V	4	
	V_{LHL}	–4.7	–4.0	–3.5	V	4	
	$V\phi_{LH}$	8.0	9.0	10.0	V	4	
Reset gate clock voltage	$V\phi_{RG}$	4.5	5.0	5.5	V	5	*6
	$V_{RGLH}-V_{RGLL}$			0.8	V	5	Low level coupling
Substrate clock voltage	$V\phi_{SUB}$	23.0	24.0	25.0	V	6	

*6 No adjustment of reset gate clock voltage is necessary when reset gate clock is driven as indicated below. In this case, reset gate clock voltage set point displayed on back of image sensor has no meaning.

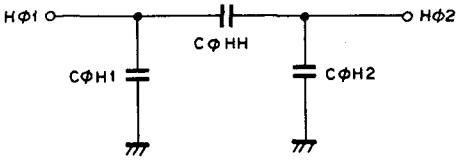
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Reset gate clock voltage	V_{RGL}	–0.2	0	0.2	V	5	
	$V\phi_{RG}$	8.5	9.0	9.5	V	5	

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi_{V1}$, $C\phi_{V3}$		1800		pF	
	$C\phi_{V2}$, $C\phi_{V4}$		2200		pF	
Capacitance between vertical transfer clocks	$C\phi_{V12}$, $C\phi_{V34}$		450		pF	
	$C\phi_{V23}$, $C\phi_{V41}$		270		pF	
Capacitance between horizontal transfer clock and GND	$C\phi_{H1}$, $C\phi_{H2}$		62		pF	
Capacitance between horizontal transfer clocks	$C\phi_{HH}$		47		pF	
Capacitance between horizontal final stage transfer clock and GND	$C\phi_{LH}$		8		pF	
Capacitance between reset gate clock and GND	$C\phi_{RG}$		8		pF	
Capacitance between substrate clock and GND	$C\phi_{SUB}$		400		pF	
Vertical transfer clock serial resistor	R_1, R_2, R_3, R_4		68		Ω	
Vertical transfer clock ground resistor	RGND		15		Ω	



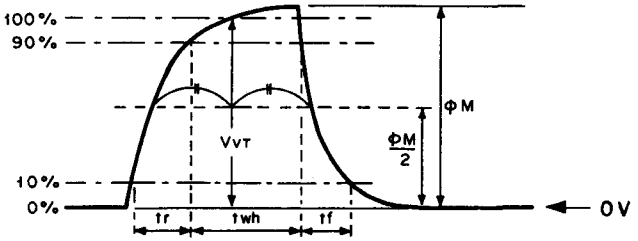
Vertical transfer clock equivalent circuit



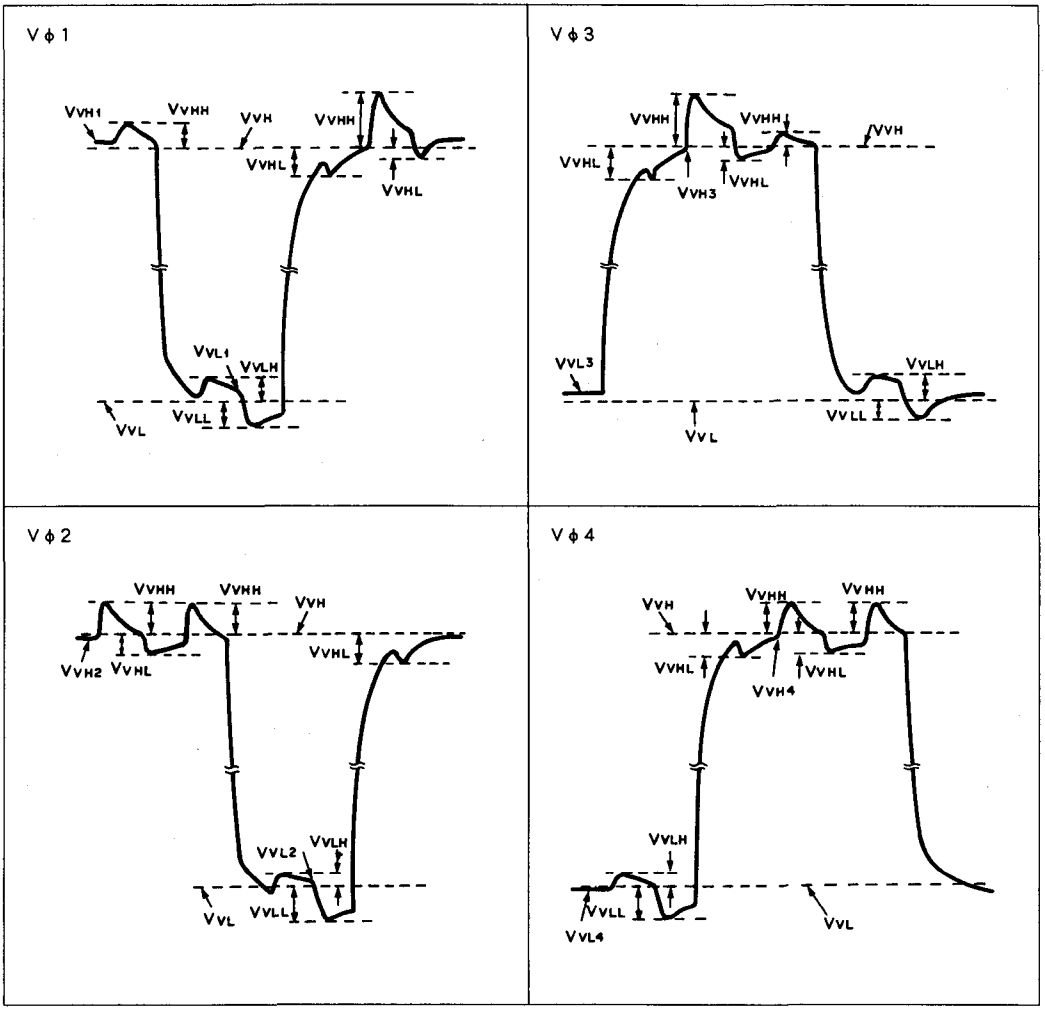
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

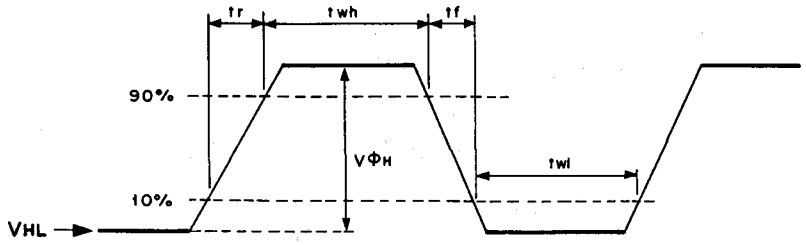
(1) Read out clock waveform



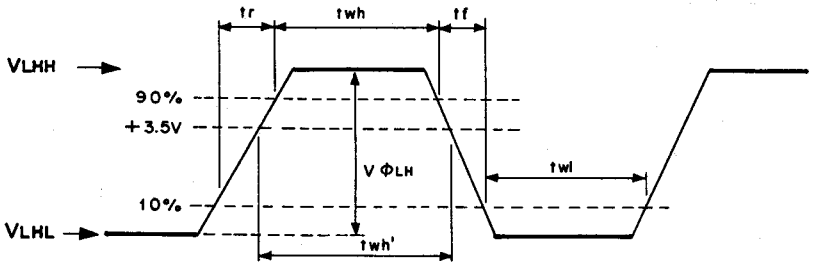
(2) Vertical transfer clock waveform



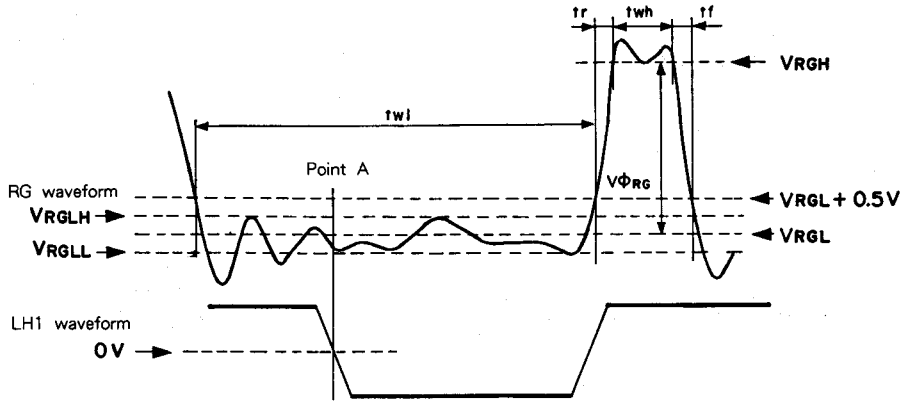
(3) Horizontal transfer clock waveform diagram



(4) Horizontal final stage transfer clock waveform diagram



(5) Reset gate clock waveform diagram



V_{RGLH} is the maximum value and V_{RGLL} the minimum value of the coupling waveform in the period from Point A in the diagram above to RG rise.

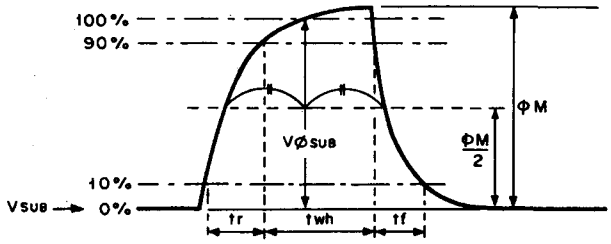
V_{RGL} is the mean value for V_{RGLH} and V_{RGLL}.

$$V_{RGL}=(V_{RGLH}+V_{RGLL})/2$$

V_{RGH} is the minimum value for twh period.

$$V\phi_{RG}=V_{RGH}-V_{RGL}$$

(6) Substrate clock waveform



Clock switching characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	V_T	2.3	2.5						0.5			0.5		μs	During read out
Vertical transfer clock	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$										0.015		0.25	μs	*7
Horizontal transfer clock	$H\phi$		20			20			15	19	*8	15	19	ns	During imaging
Horizontal final stage clock	$LH\phi$		24		22	27			10			9		ns	During imaging
Horizontal transfer/horizontal final stage clock	$H\phi_1$, $LH\phi$		5.38						0.01			0.01		μs	During parallel serial conversion.
Horizontal transfer clock	$H\phi_2$					5.38			0.01			0.01		μs	
Reset gate clock	ϕ_{RG}	11	13			51			3			3		ns	
Substrate clock	ϕ_{SUB}	1.5	1.8							0.5			0.5	μs	During charge drain.

*7 When vertical transfer clock driver CXD1250 is in use.
*8 tf ≧ tr–2 ns

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	$H\phi$	16	20		ns	*9
Horizontal transfer/ horizontal final stage clock	$H\phi2$, $LH\phi$	15	20		ns	*10

*9 "two" is the *overlap period of horizontal transfer* clocks $H\phi_1$ and $H\phi_2$'s twh and twl.
*10 "two" is the overlap period of horizontal transfer clock $H\phi_2$'s twl and horizontal final stage transfer clock $LH\phi$'s twh′ .

Operating Characteristics

(Ta=25℃)

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	150	190		mV	1	
Saturation signal	Vsat	500			mV	2	Ta=60℃
Smear	Sm		0.009	0.015	%	3	
Video signal shading	SH			20	%	4	Zone 0, I
				25	%	4	Zone 0 to II'
Dark signal	Vdt			2	mV	5	Ta=60℃
Dark signal shading	Δ Vdt			1	mV	6	Ta=60℃
Flicker	F			2	%	7	
Lag	Lag			0.5	%	8	

Zone chart of Video signal shading

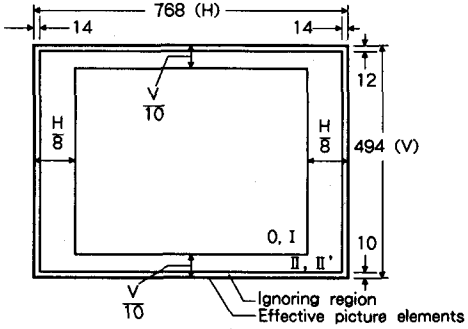


Image Sensor Characteristics Test Method

◎ Test conditions

① Through the following tests the substrate voltage and reset gate clock voltage are set to the value displayed on the device, while the device drive conditions are at the typical value of the bias and clock voltage conditions.

② Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OB) is set as the reference, the values obtained at Ⓐ point in the figure of the Drive Circuit are utilized.

◎ Definition of standard imaging conditions

① Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 cd/ m², color temperature 3200K Halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t=1.0mm) as IR cut filter and image at F8. At this time, light intensity to sensor receiving surface is defined as standard sensitivity testing light intensity. Signal output average value in this condition is called V_A.

② Standard imaging condition II: Image a light source (color temperature of 3200K) which uniformity of brightness is within 2% at all angles. Use a testing standard lens with CM500S (t=1.0mm) as IR cut filter. The light intensity is adjusted to the value indicated in each testing item by lens diaphragm.

1. Sensitivity
   Set to standard imaging condition I and measure signal output (S) at the center of the screen.

2. Saturation signal
   Set to standard imaging condition II. Adjust light intensity to 10 times that of signal output average value (V_A), then test signal output minimum value.

3. Smear
   Set to standard imaging condition II. Adjust light intensity to 500 times that of signal output average value (V_A). Stop read out clock. When the charge drain executed by the electric shutter at the respective H blankings takes place, test the maximum value Vsm of signal output.

   $$Sm=\frac{Vsm}{V_A}\times\frac{1}{500}\times\frac{1}{10}\times 100\ (\%)\ (1/10V)$$

4. Video signal shading
   Set to standard imaging condition II. Adjust light intensity to signal output average value (V_A) with lens diaphragm at F5.6 to F8. Then test maximum (Vmax) and minimum (Vmin) values of signal output.

   $SH=(Vmax-Vmin)/V_A \times 100\ (\%)$

5. Dark signal
   Test signal output average value Vdt when the device ambient temperature is at 60 ℃ and light is obstructed with horizontal idle transfer level as reference.

6. Dark signal shading
   Following 5, test maximum (Vdmax) and minimum (Vdmin) values of dark signal output.

   $\Delta\ Vdt=Vdmax-Vdmin$

7. Flicker

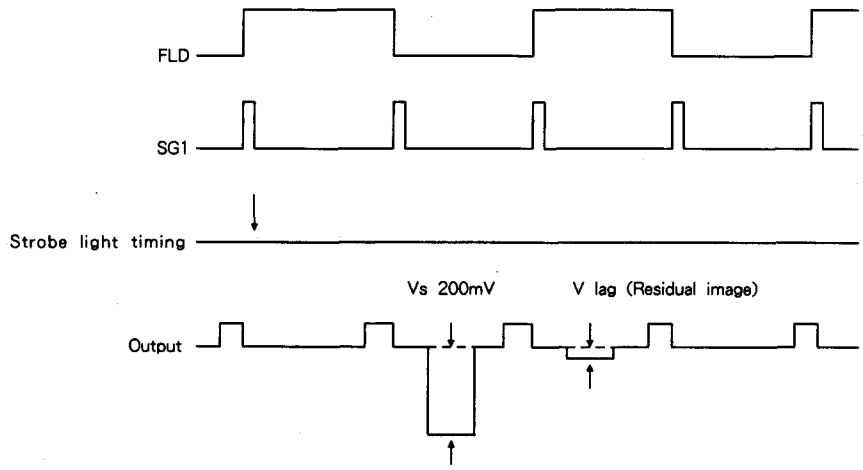
Set to standard imaging condition II. Adjust light intensity to signal output average value (V_A). Then test the signal output difference (Δ Vf) between even field and odd field.

$F=(\Delta Vf/V_A) \times 100$ (%)

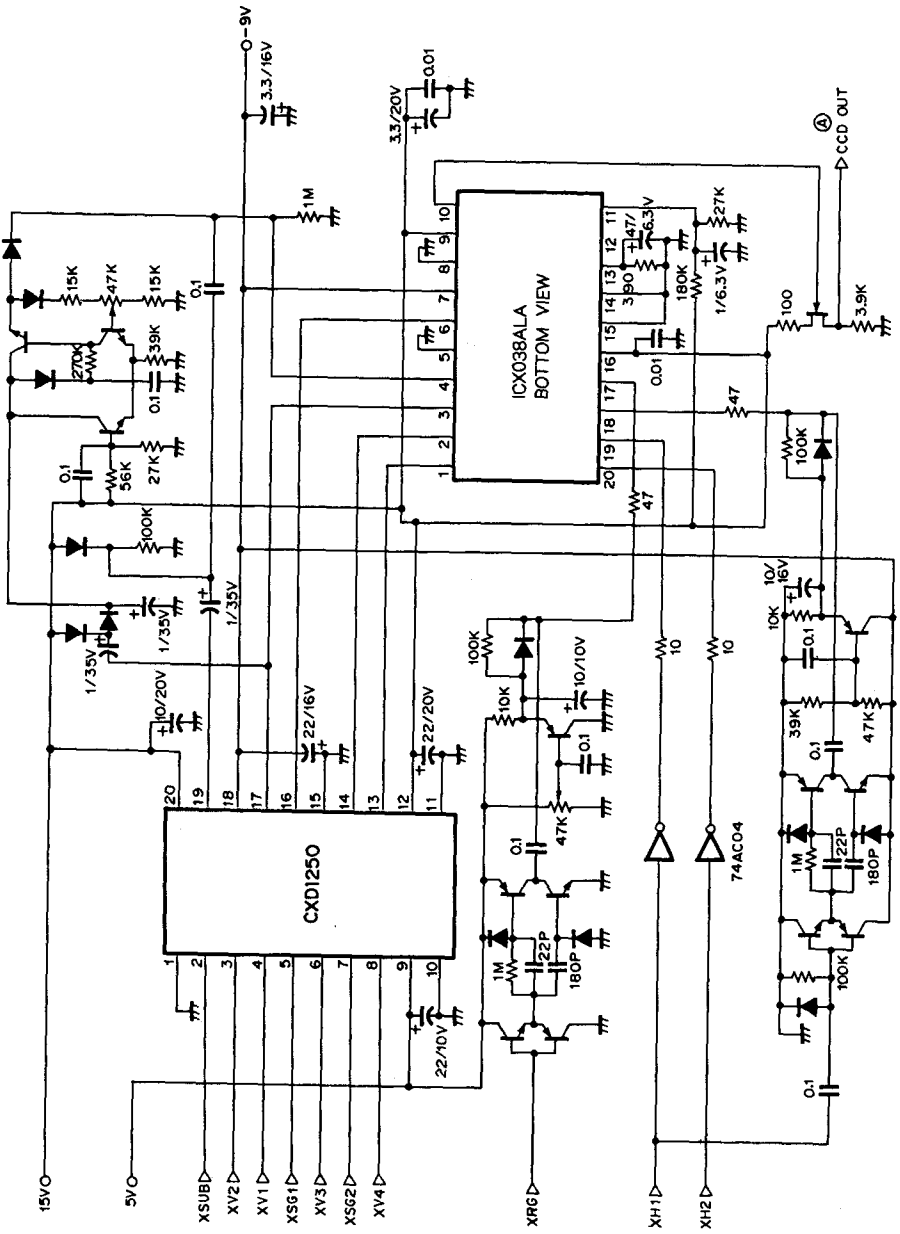
8. Residual image

Adjust signal output value (Vs) by strobe light to 200mV. Then light a stroboscopic tube with the following timing and test the residual image (Vlag).

Lag = (Vlag/Vs) × 100 (%)

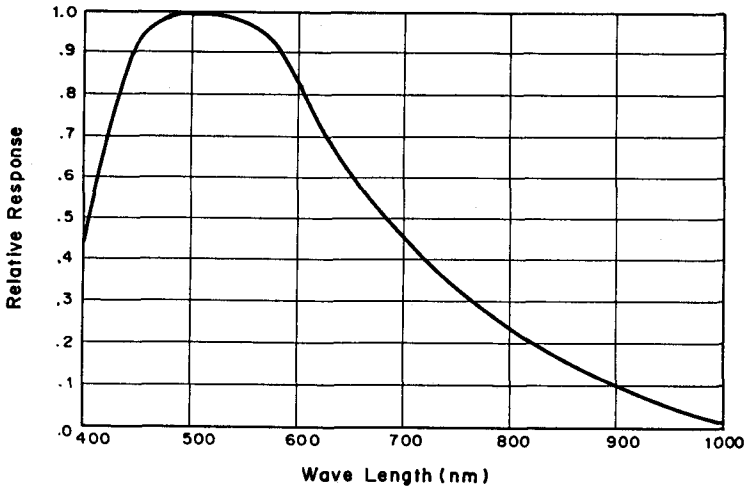


Drive Circuit

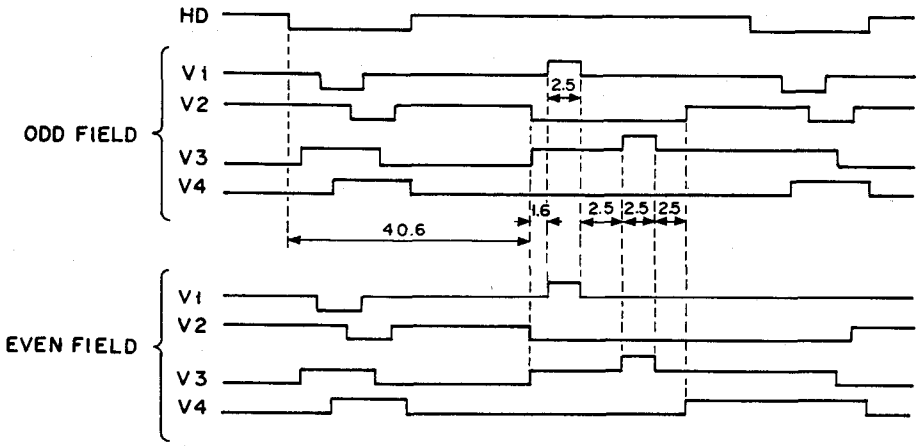


Spectral Sensitivity Characteristics

(Excluding light source characteristics, including lens characteristics)

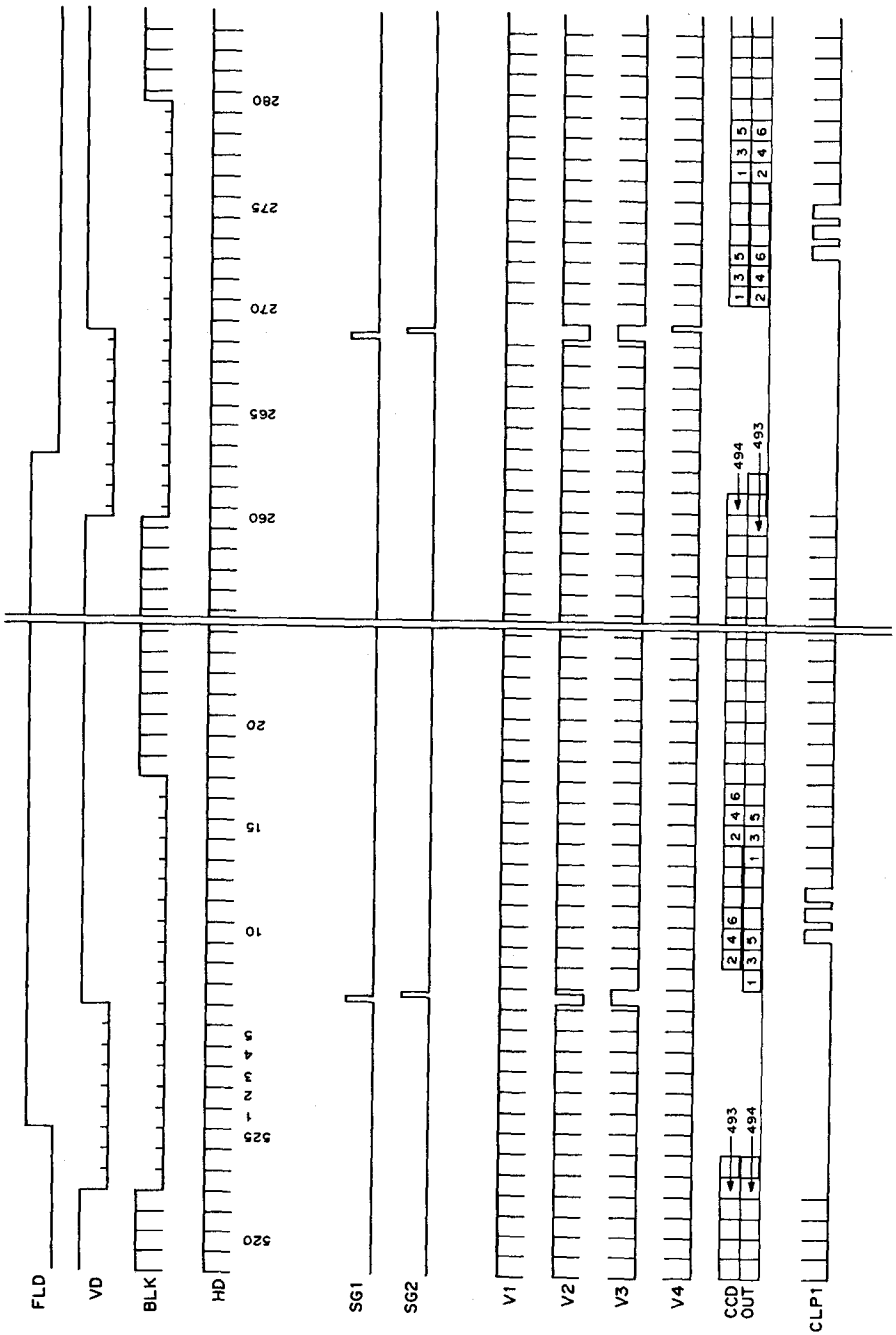


Using read out clock timing chart

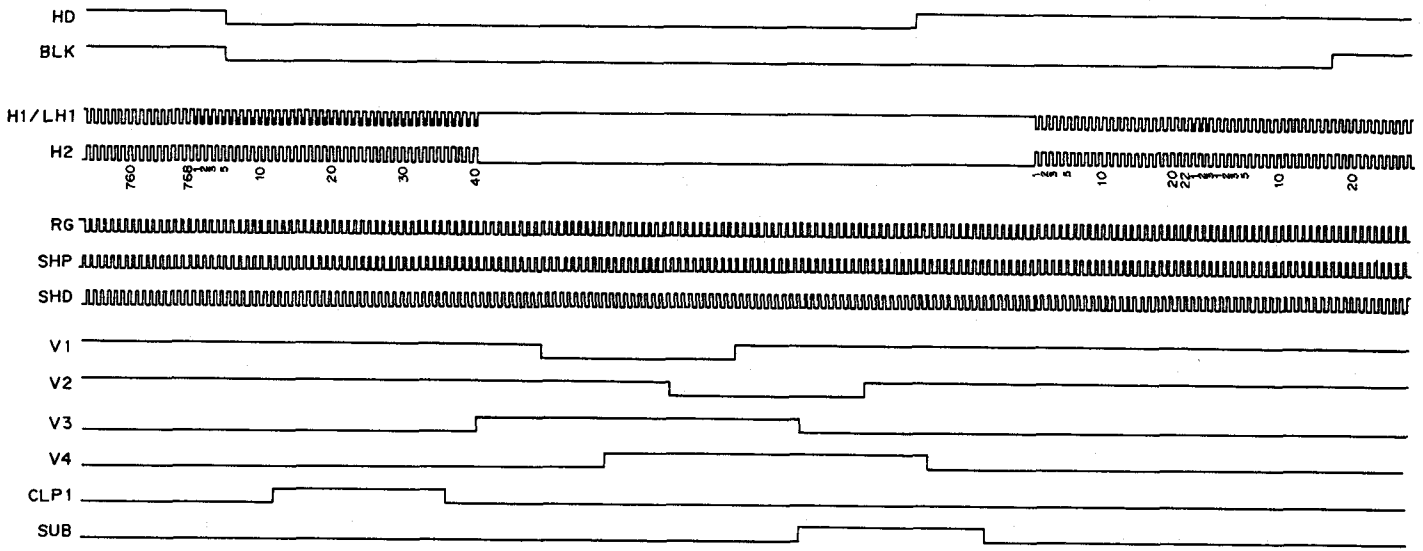


Unit : µs

Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



SONY

ICX038ALA

Handling Instructions

1) Static charge prevention
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensor.
   e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
   a) Make sure the package temperature does not exceed 80 °C .
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an imaging device do not use a solder suction equipment. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
   a) Operate in clean environments (around class 1000 will be appropriate).
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

SONY®

ICX027BLA

1/2 inch CCD Image Sensor for CCIR B/W Camera

Description

The ICX027BLA is an interline transfer CCD solid-state imager suitable for CCIR 1/2 inch B/W video cameras. High sensitiveness is achieved through the adoption of HAD (Hole Accumulation Diode) sensors.

This chip features a field integration read out system, an electronic shutter with variable charge-storage time and 20pin Cer-DIP package.

Features

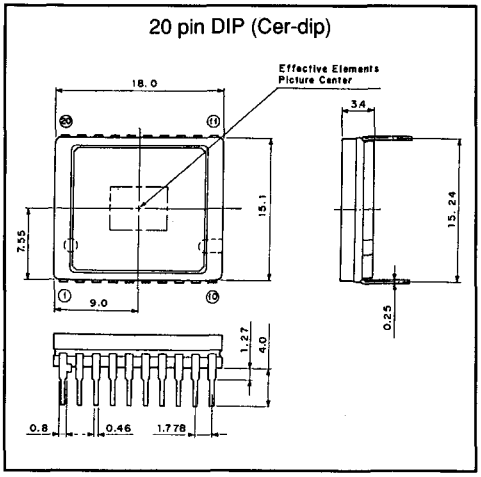
- High sensitivity (+6 dB compare with ICX027AL)
- Optical size 1/2 inch format
- Field integration read out system
- Low dark current
- Horizontal register 5V drive
- High antiblooming
- Low smear
- Variable speed electronic shutter

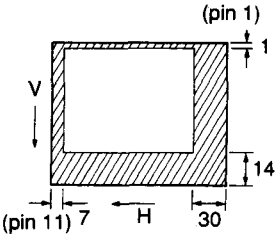
Device Structure

- Number of effective pixels 500 (H) × 582 (V)
- Number of total pixels 537 (H) × 597 (V)
- Interline transfer CCD image sensor
- Chip size 7.84 mm (H) × 6.40 mm (V)
- Unit cell size 12.7 µm (H) × 8.3 µm (V)
- Optical black
  - Horizontal (H) direction Front 7 pixels Rear 30 pixels
  - Vertical (V) direction Front 14 pixels Rear 1 pixels
- Number of dummy bits
  - Horizontal 16
  - Vertical 1 (even field only)
- Substrate material silicon

Package Outline

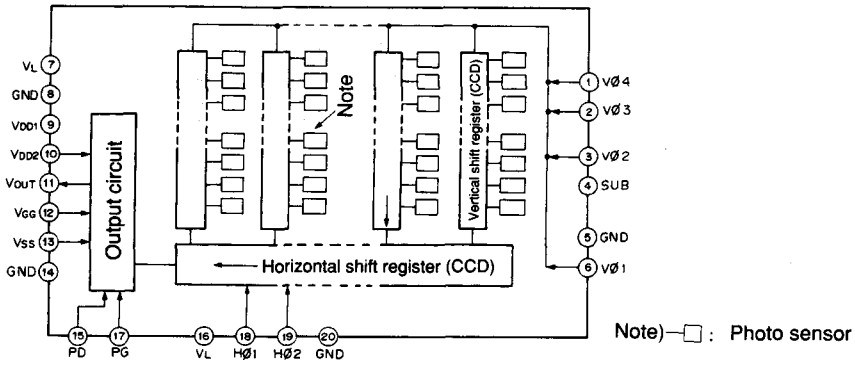
Unit: mm





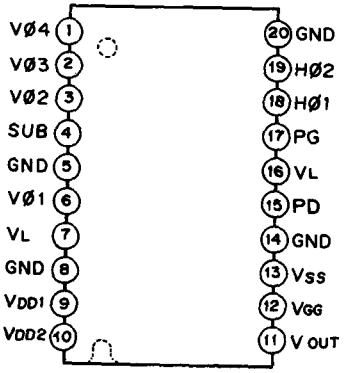
Optical black position (Top View)

Block Diagram



E91641-YA

Pin Configuration (Top View)



Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	11	VOUT	Signal output
2	Vφ3	Vertical register transfer clock	12	VGG	Output amplifier gate bias
3	Vφ2	Vertical register transfer clock	13	VSS	Output amplifier source
4	SUB	Substrate (Overflow drain)	14	GND	GND
5	GND	GND	15	PD	Precharge drain bias
6	Vφ1	Vertical register transfer clock	16	VL	Protective transistor bias
7	VL	Protective transistor bias	17	PG	Precharge gate clock
8	GND	GND	18	Hφ1	Horizontal register transfer clock
9	VDD1	Output amplifier drain supply	19	Hφ2	Horizontal register transfer clock
10	VDD2	Output amplifier drain supply	20	GND	GND

Absolute Maximum Ratings

• Substrate voltage	SUB – GND	−0.3 to +55 V
• Supply voltage	VDD1, VDD2, PD, VOUT, VSS – GND	−0.3 to +18 V
	VDD1, VDD2, PD, VOUT, VSS – SUB	−55 to +10 V
• Clock input voltage	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – GND	−15 to +20 V
	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – SUB	−65 to +10 V
• Voltage difference between vertical clock input pins		15 V*
• Voltage difference between horizontal clock input pins		17 V
• Hφ1, Hφ2, – Vφ4		−17 to +17 V
• PG, VGG – GND		−10 to +15 V
• PG, VGG – SUB		−55 to +10 V
• VL – SUB		−65 to +0.3 V
• Beside GND, SUB, VL – VL		−0.3 to +30 V
• Storage temperature		−30 to +80°C
• Operating temperature		−10 to +55°C

***Note)** +27 V (Max.) when clock width < 10 µs, duty factor < 0.1%

Bias Conditions

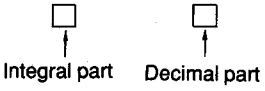
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD1}, V_{DD2}	14.55	15.0	15.45	V	V_{DD1} = V_{DD2}
Precharge drain voltage	V_{PD}	14.55	15.0	15.45	V	V_{PD} = V_{DD1} = V_{DD2}
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	V_{SS}	Ground through 680 Ω resistor				±5%
Substrate voltage adjustment range	V_{SUB}	7		19	V	*1
Fluctuation range after substrate voltage adjustment	V_{SUB}	-3		+3	%	
Protective transistor bias	V_L	*2				

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		2.5		mA	I_{DD} = I_{DD1} + I_{DD2}
Input current	I_{IN1}			1	μA	*3
Input current	I_{IN2}			10	μA	*4

Note) *1. Substrate voltage (V_{SUB}) setting value display.
Substrate voltage setting value is displayed at the back of the device through a code address. Adjust so as to obtain the displayed voltage at SUB pin.

V_{SUB} code address – two digits display



The relation between code address of integral part and actual numerical values.

Code address of integral part	7	8	9	A	B	C	D	E	F	G	H	I	J
Numerical Value	7	8	9	10	11	12	13	14	15	16	17	18	19

<Example> F5 → 15.5 (V)

*2. V_L setting is V_{VL} of the vertical transfer clock waveform.

*3. 1) Current to earth when 18V is applied to pins V_{DD1}, V_{DD2}, V_{OUT}, V_{SS} and SUB pin. However, pins that are not tested are grounded.
2) Current to earth when 20V is sequentially applied to pins $V\phi1$, $V\phi2$, $V\phi3$, $V\phi4$, $H\phi1$ and $H\phi2$. However, 20V is applied to SUB while pins that are not tested are grounded.
3) Current to earth when 15V is sequentially applied to pins PG and V_{GG}. However, 15V is applied to SUB while pins that are not tested are grounded.

*4. 1) Current to earth when 55V is applied to SUB pin. Pins that are not tested are grounded.
2) Current to earth when V_L is grounded, GND and SUB are open and 30V is applied to other pins.

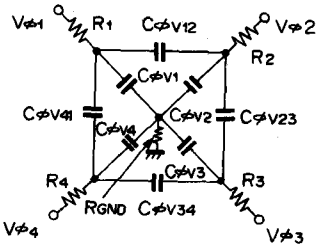
Clock Voltage Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	No.	Remarks
Read out clock voltage	V_{VT}	14.3	15.0	15.7	V	2,6	*1
Vertical transfer clock voltage *2	V_{VH1}, V_{VH2}, V_{VH3}, V_{VH4}	–0.2	0	0.2	V	1,2,3,6	$V_{VH}=(V_{VH1}+V_{VH2})/2$
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	–9.6	–9.0	–8.3	V	1,2,3,6	$V_{VL}=(V_{VL3}+V_{VL4})/2$
	$V_{\phi V}$	8.1	9.0	9.8	V	1,2,3,6	$V_{\phi V}=V_{VHn}-V_{VLn}$ (n=1 to 4)
	$\lvert V_{VH1} - V_{VH2} \rvert$			0.2	V	3,6	
	$V_{VH3} - V_{VH}$	–0.4		0.1	V	2,3,6	
	$V_{VH4} - V_{VH}$	–0.4		0.1	V	1,3,6	
	V_{VHH}			0.8	V	1,2,3,6	High level coupling
	V_{VHL}			1.0	V	1,2,3,6	High level coupling
	V_{VLH}			0.8	V	1,2,3,6	Low level coupling
	V_{VLL}			0.8	V	1,2,3,6	Low level coupling
Horizontal transfer clock voltage	$V_{\phi H}$	4.7	5.0	5.3	V	18,19	*3
	V_{HL}	–0.05	0	0.05	V	18,19	
Precharge gate clock voltage	$V_{\phi PG}$	8.0		11.5	V	17	*4
	V_{PGL}	–0.1	0	0.1	V	17	
Substrate clock voltage	$V_{\phi SUB}$	23.0	32.0	34.0	V	4	*5

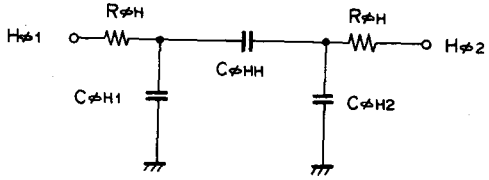
Note) *1. See Fig. 1.
*2. See Fig. 2.
*3. See Fig. 3.
*4. See Fig. 3.
*5. See Fig. 4.

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$, $C_{\phi V3}$		1000		pF	
Capacitance between vertical transfer clock and GND	$C_{\phi V2}$, $C_{\phi V4}$		1200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$, $C_{\phi V34}$		1400		pF	
Capacitance between vertical transfer clocks	$C_{\phi V23}$, $C_{\phi V41}$		900		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, $C_{\phi H2}$		70		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Capacitance between precharge gate clock and GND	$C_{\phi PG}$		8		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		400		pF	
Vertical transfer clock serial resistor	R_1, R_2, R_3, R_4		33		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock serial resistor	$R_{\phi H}$		10		Ω	



Vertical transfer clock equivalent circuit



Horizontal trasfer clock equivalent circuit

Drive Clock Waveform Conditions

1. Read out clock waveform

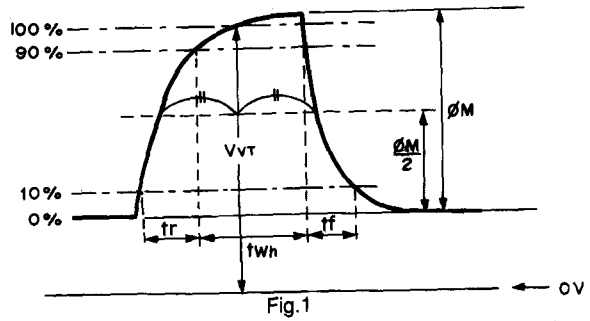


Fig.1

2. Vertical transfer clock waveform

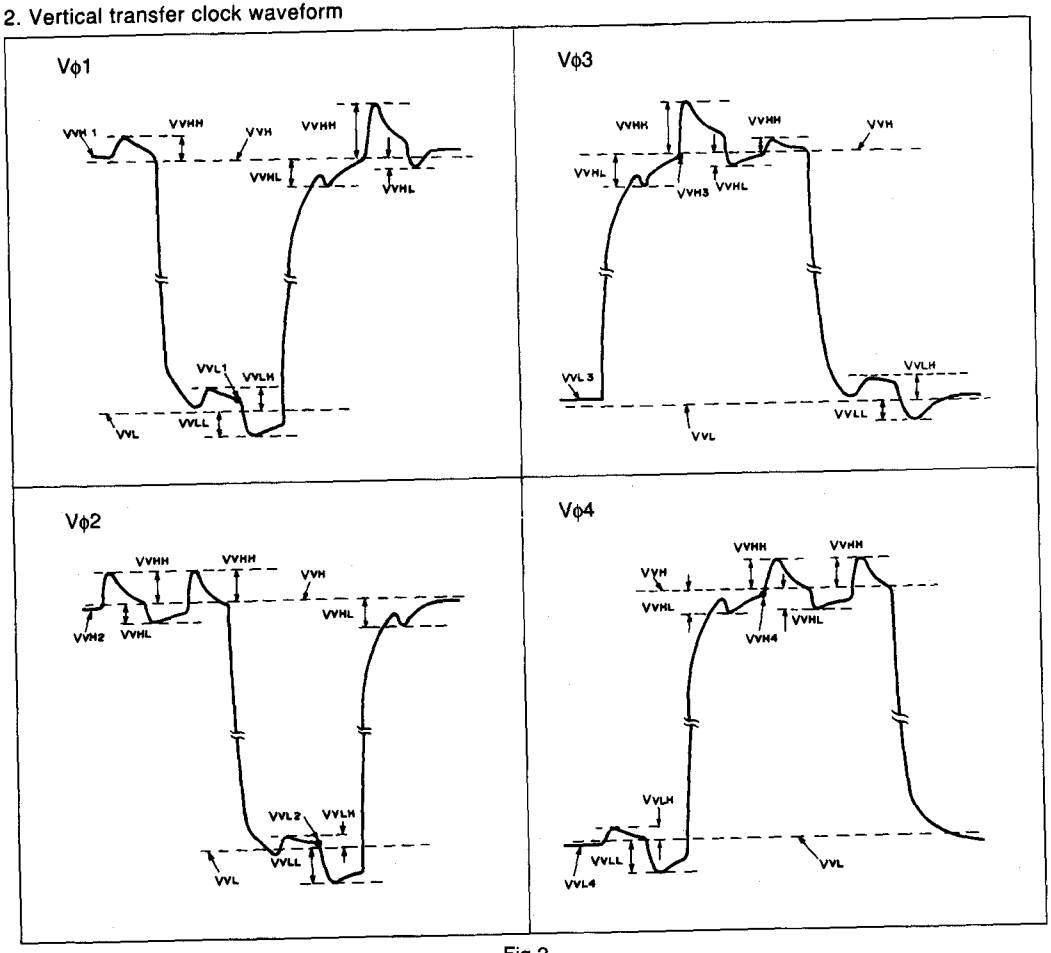


Fig.2

3. Horizontal transfer clock waveform/Precharge gate clock waveform

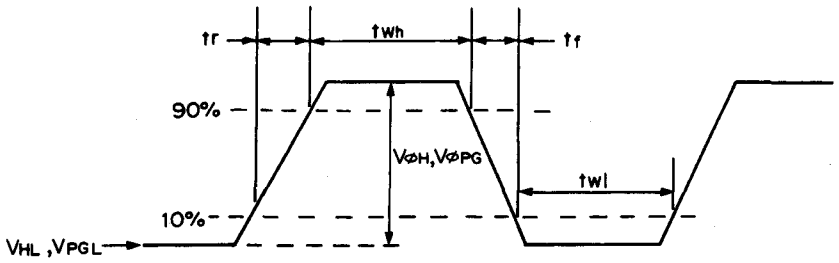


Fig. 3

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	VT	1.5	1.85							0.5			0.5	μs	During read out
Vertical transfer clock	Vφ1,Vφ2,Vφ3,Vφ4									0.45	0.015		0.25	μs	*
Horizontal transfer clock	Hφ	38	42		38	42			12	15		10	15	ns	During imaging
Horizontal transfer clock	Hφ1		5.6						0.012			0.01		μs	During parallel serial conversion.
Horizontal transfer clock	Hφ2					5.6			0.012			0.01		μs	During parallel serial conversion.
Precharge gate clock	φPG	15	17		76	82			4			3		ns	
Substrate clock	φSUB	1.5	2.1							0.5			0.5	μs	During charge drain

***Note)** When vertical transfer clock driver CXD1250 is in use.

4. Substrate clock waveform

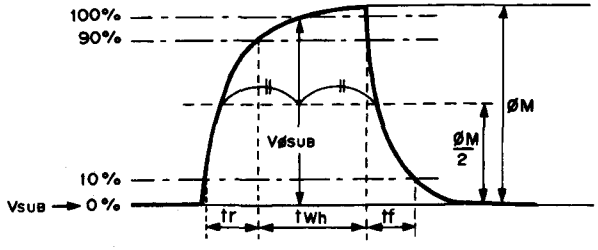


Fig. 4

Operating Characteristics Ta = 25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	220	300		mV	1	
Saturation signal	Vsat	450			mV	2	Ta=55°C
Smear	SM		0.007	0.015	%	3	
Blooming margin		1000			times	4	
Video signal shading	SH			20	%	5	Zone 0, I
				25	%	5	Zone 0 to II'
Dark signal	Vdt			2	mV	6	Ta=55°C
Dark signal shading	ΔVdt			1	mV	7	Ta=55°C
Flicker	F			2	%	8	
Lag	ΔVlag			0.5	%	9	

Test Method

Test conditions

①Through the following tests the substrate voltage should set to the value displayed on the device, while the device drive conditions should be kept within the range of the bias and clock voltage conditions.

②Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OPB) is set as the reference. The values obtained at A point in the figure of the Drive Circuit are utilized.

Definition of standard imaging conditions

①Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 cd/m², 3200 K Halogen source), at F8 with a typical test lens, and CM-500S (t=1.0 mm) for IR cut filter.

②Standard imaging condition II: Use a light source with uniformity within 2%, color temperature of 3200 K and CM-500S (t=1.0 mm) as IR cut filter. The light intensity is adjusted in accordance with the average signals (V_A) indicated in each item.

1. Set to standard imaging condition I and measure signal output (S) at the center of the screen.

2. Set to standard imaging condition II. Adjust light intensity to 10 times when the average signal V_A=150mV. Then test signal Min. Value.

3. Set to standard imaging condition II. Adjust light intensity to 500 times when the average signal V_A=150mV. Stop Read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the Max. value V_{SM} of signal output.

   $SM = (V_{SM}/V_A) \times {}^1/_{500} \times {}^1/_{10} \times 100\ (\%)$ $({}^1/_{10}V)$

4. Set to standard imaging condition II. Adjust light intensity to 1000 times when the average signal V_A=150mV. Then check that there is no blooming.

5. Video signal shading SH
   Set to standard imaging condition II. Test signal Max. (Vmax) and Min. (Vmin) values. Adjust light intensity to obtain an average signal (V_A) of about 150mV.

   $SH = (Vmax - Vmin)/V_A \times 100$ (%)

6. Test the average signal when the device ambient temperature is at 55°C and light is obstructed with horizontal idle transfer level as reference.

7. Following test 6, test Max. (Vd max) and Min. (Vd min) of signal output. Only keep spot defects out of this range.

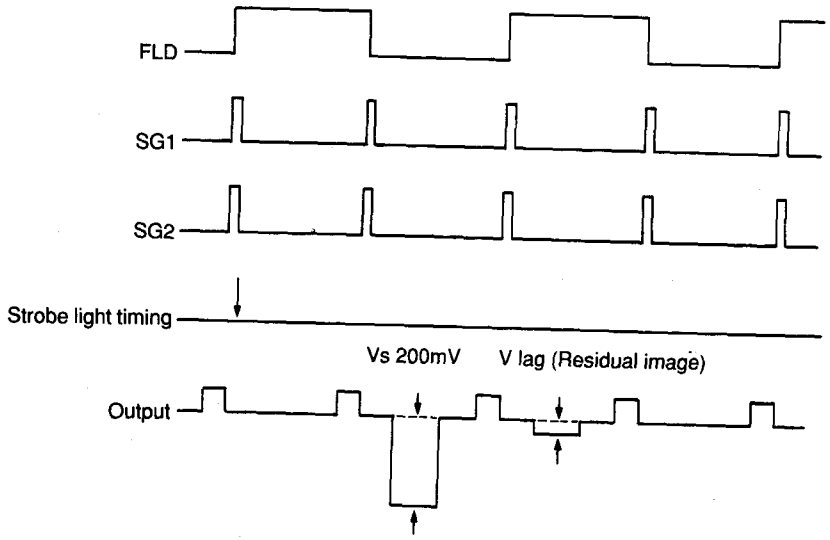
   $\Delta Vdt = Vd\ max - Vd\ min$

8. Set to imaging condition II. Test the output signal difference (ΔVf) between even and odd field. At that time, adjust light intensity to obtain an average signal V_A of about 150mV.

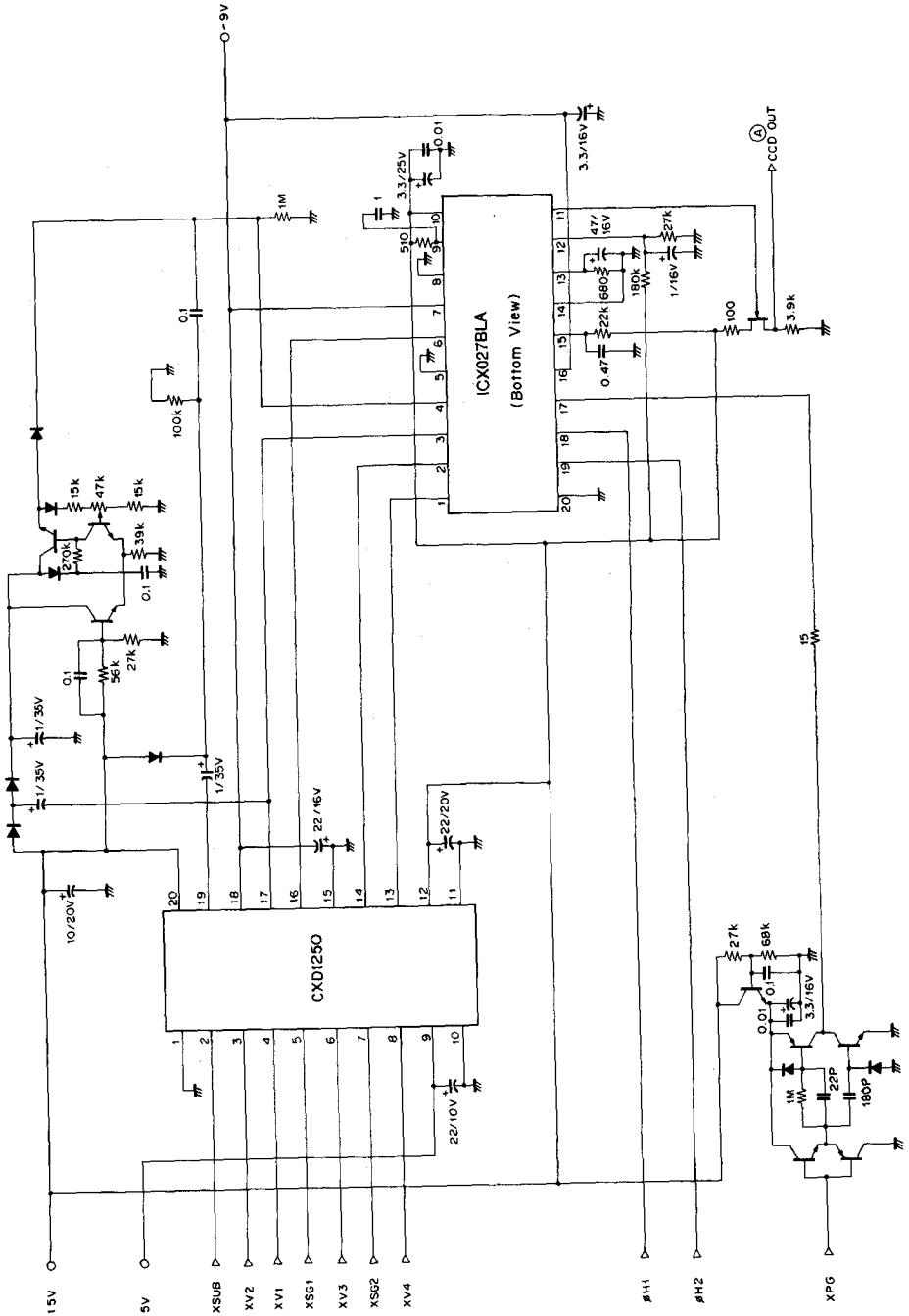
   $F = (\Delta Vf/V_A) \times 100$ (%)

9. Light a stroboscopic tube with the following timing and test the residual image.

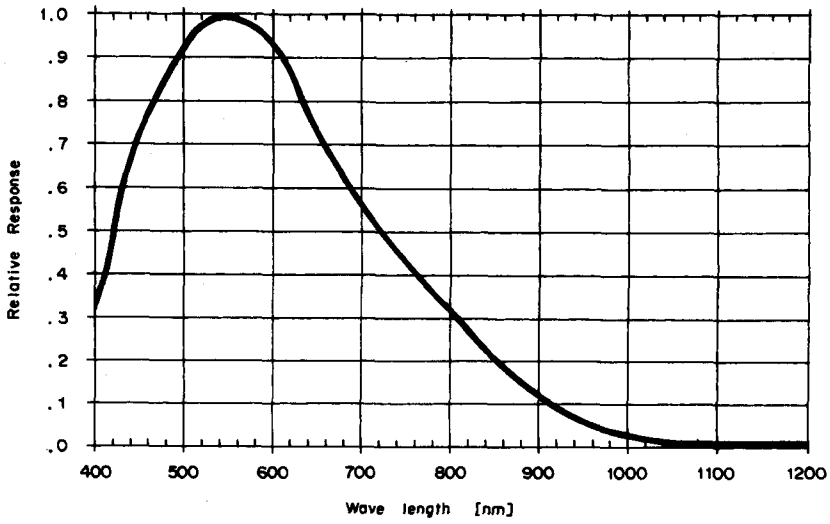
   $\Delta Vlag = (Vlag/Vs) \times 100$ (%)



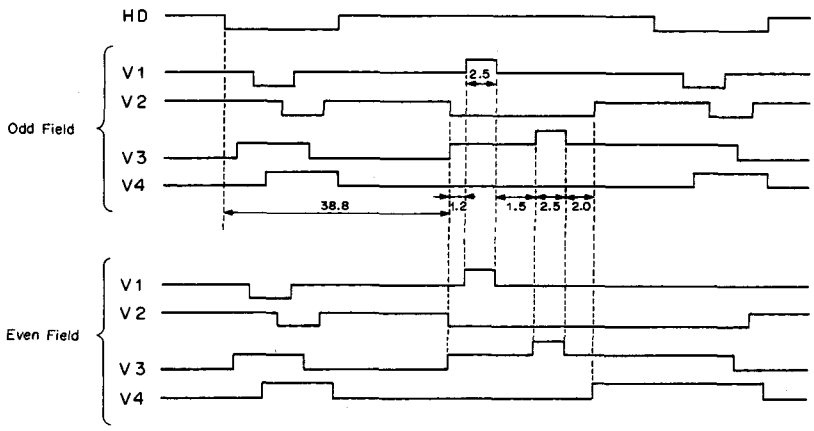
Drive Circuit



Spectral Sensitivity Characteristics
(Excluding light source characteristics, including lens characteristics)

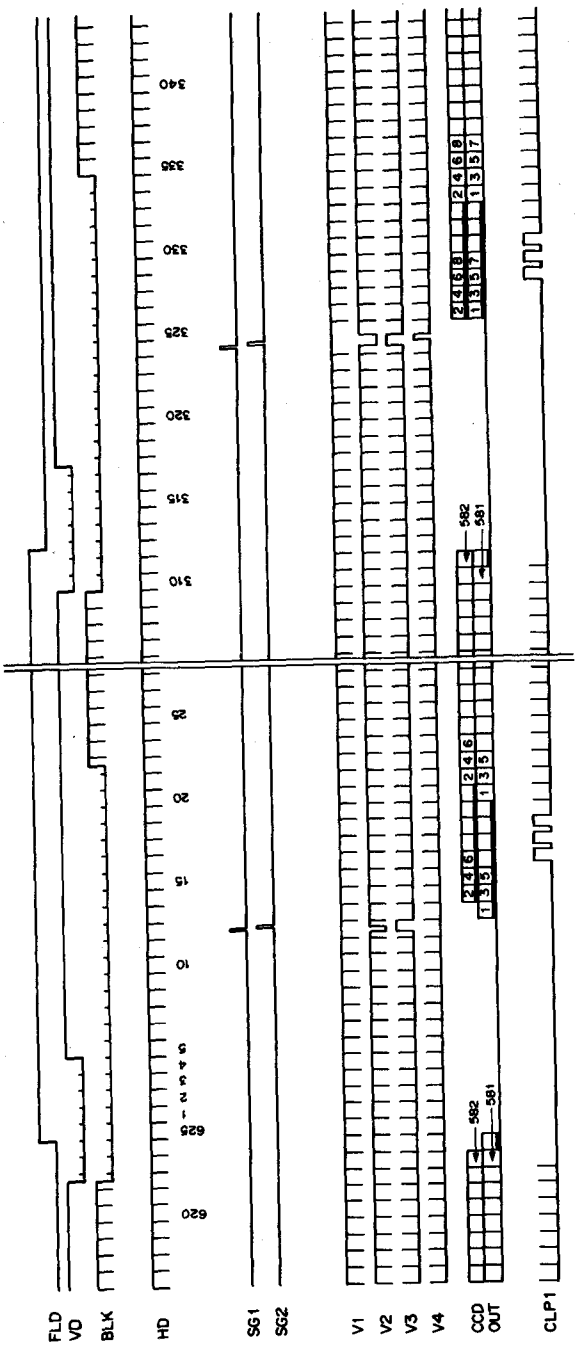


Using Read Out Clock Timing Chart

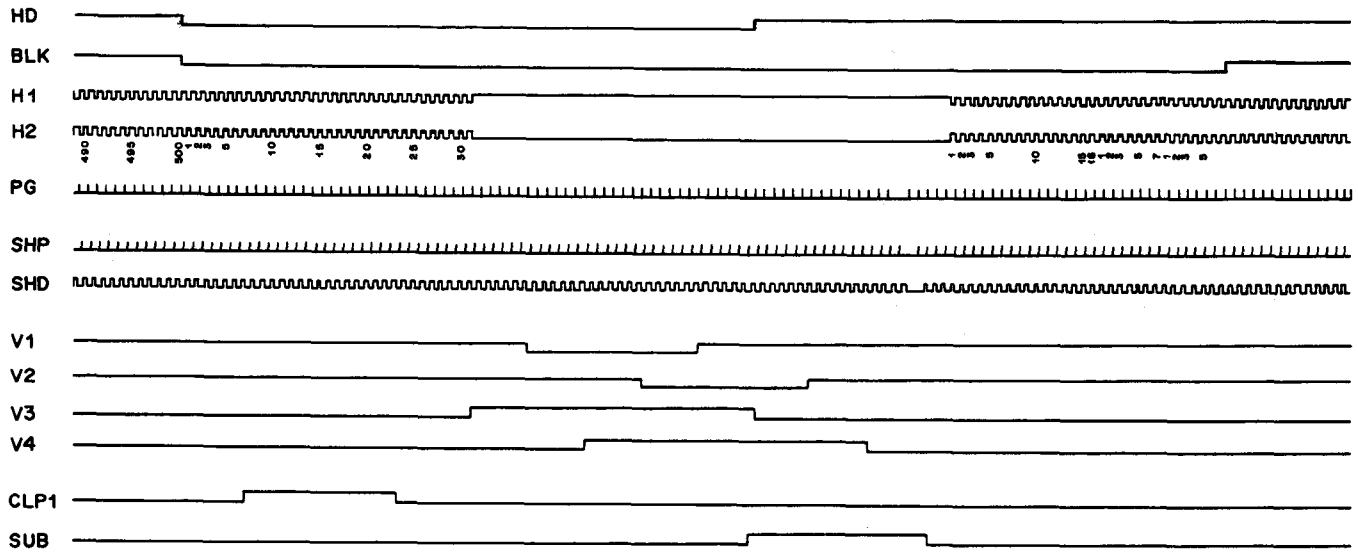


Unit:μs

Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



During electronic shutter operation

Handling Instructions

1) Static charge prevention
CCD image sensor are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount cool sufficiently.
c) To dismount an imaging device do not use a solder pult. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

SONY

ICX039ALA

1/2 inch CCD Image Sensor for CCIR B/W Camera

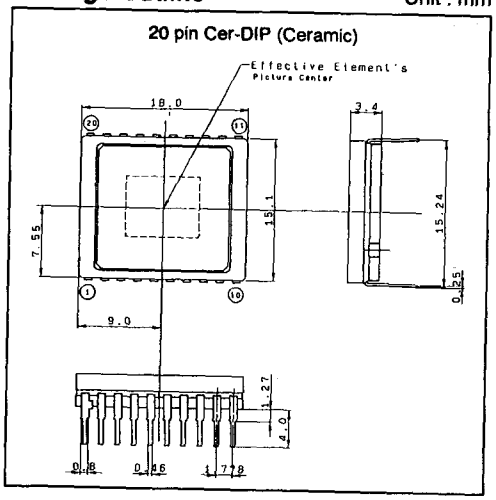
Description

ICX039ALA is an interline transfer CCD solid-state imager suitable for CCIR 1/2 inch B/W video cameras. High sensitiveness is achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.

This chip features a field integration read out system, an electronic shutter with variable charge-storage time and 20 pin Cer-DIP package.

Package Outline

Unit : mm

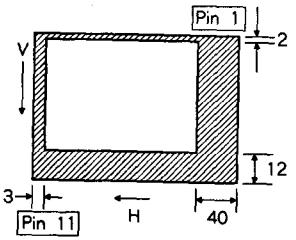


Features

- High image, high sensitivity and low dark current
- Consecutive various speed shutter
  1/50sec. (Typ.), 1/100sec. to 1/10000sec.
- Low smear
- High antiblooming
- Horizontal register 5V drive
- Reset gate 5V drive

Device Structure

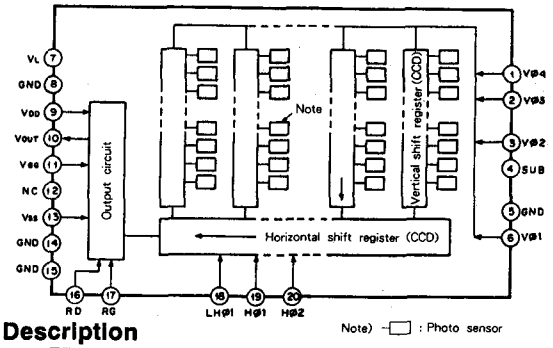
- Optical size 1/2 inch format
- Number of effective pixels 752 (H) ×582 (V) Approx. 440k pixels
- Number of total pixels 795 (H) ×596 (V) Approx. 470k pixels
- Interline transfer CCD image sensor
- Chip size 7.95 mm (H) ×6.45 mm (V)
- Unit cell size 8.6 µm (H) ×8.3 µm (V)
- Optical black Horizontal (H) direction Front 3 pixels Rear 40 pixels
  Vertical (V) direction Front 12 pixels Rear 2 pixels
- Number of dummy bits Horizontal 22
  Vertical 1 (even field only)
- Substrate material silicon



Optical black position (Top View)

E91707 – ST

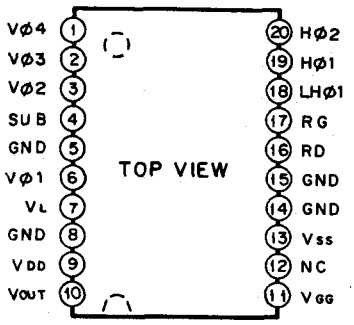
Block Diagram



Note) : Photo sensor

Pin Configuration

(Top View)



Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	V φ 4	Vertical register transfer clock	11	VGG	Output amplifier gate bias
2	V φ 3	Vertical register transfer clock	12	NC	
3	V φ 2	Vertical register transfer clock	13	Vss	Output amplifier source
4	SUB	Substrate (Overflow drain)	14	GND	GND
5	GND	GND	15	GND	GND
6	V φ 1	Vertical register transfer clock	16	RD	Reset drain bias
7	VL	Protective transistor bias	17	RG	Reset gate clock
8	GND	GND	18	LH φ 1	Horizontal register final stage transfer clock
9	VDD	Output amplifier drain supply	19	H φ 1	Horizontal register transfer clock
10	VOUT	Signal output	20	H φ 2	Horizontal register transfer clock

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB-GND		–0.3 to +55	V	
Supply voltage	VDD, VRD, VOUT, Vss – GND	–0.3 to +18	V	
	VDD, VRD, VOUT, Vss – SUB	–55 to +10	V	
Clock input voltage	V φ 1, V φ 2, V φ 3, V φ 4 – GND	–15 to +20	V	
	V φ 1, V φ 2, V φ 3, V φ 4 – SUB	to +10	V	
Voltage difference between vertical clock input pins		to+15	V	* (Max.)
Voltage difference between horizontal clock input pins		to+17	V	
V φ 1, V φ 2 – V φ 4		–17 to +17	V	
LH φ 1, RG, VGG – GND		–10 to +15	V	
LH φ 1, RG, VGG – SUB		–55 to +10	V	
VL –SUB		–65 to +0.3	V	
Beside GND, SUB-VL		–0.3 to +30	V	
Storage temperature		–30 to +80	℃	
Operating temperature		–10 to +60	℃	

* +27V (Max.) when clock width < 10 μs, duty factor < 0.1%.

Bias Conditions

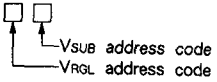
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD}	14.55	15.0	15.45	V	
Reset drain voltage	V_{RD}	14.55	15.0	15.45	V	$V_{RD}=V_{DD}$
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	Vss	Ground through				± 5%
Substrate voltage adjustment range	V_{SUB}	9.0		18.5	V	*2
Fluctuation range after substrate voltage adjustment	Δ V_{SUB}	−3		+3	%	
Reset gate clock voltage adjustment range	V_{RGL}	1.0		4.0	V	*2 *6
Fluctuation range after reset gate clock voltage adjustment	Δ V_{RGL}	−3		+3	%	
Protective transistor bias	V_L	*3				

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		5		mA	
Input current	I_{IN1}			1	μA	*4
Input current	I_{IN2}			10	μA	*5

*2 Substrate voltage (V_{SUB}) • reset gate clock voltage (V_{RGL}) setting value display.
Setting values of substrate voltage and reset gate clock voltage are displayed at the back of the device through a code address. Adjust substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) to the displayed voltage. Fluctuation range after adjustment is ± 3%.

V_{SUB} code address −1 digit display
V_{RGL} code address −1 digit display



Code addresses and actual numerical values correspond to each other as follows.

V_{RGL} address code	1	2	3	4	5	6	7
Numerical value	1.0	1.5	2.0	2.5	3.0	3.5	4.0

V_{SUB} address code	E	f	G	h	J	K	L	m	N	P	Q	R	S	T	U	V	W	X	Y	Z
Numerical value	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5

<Example> "5L" → V_{RGL}=3.0V
V_{SUB}=12.0V

*3 V_L setting is the V_{VL} voltage of the vertical transfer clock waveform.

*4 1. Current to each pin when 18V is applied to V_{DD}, V_{OUT}, Vss and SUB pins, while pins that are not tested are grounded.
2. Current to each pins when 20V is applied sequentially to V φ 1, V φ 2, V φ 3, V φ 4, H φ 1 and H φ 2, while pins that are not tested are grounded. However, 20V is applied to SUB.
3. Current to each pins when 15V is applied sequentially to pins RG, LH φ 1 and V_{GG}, while pins that are not tested are grounded. However, 15V is applied to SUB.
4. Current to V_L pin when it is grounded, while 30V is applied to all pins except pins that are not tested. However, GND and SUB pins are kept open.

*5 Current to SUB pin when 55V is applied to SUB pin, while pins that are not tested are grounded.

Clock Voltage Conditions

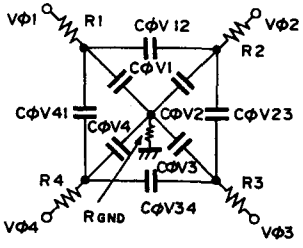
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Read out clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	–0.05	0	0.05	V	2	$V_{VH}=(V_{VH1}+V_{VH2})/2$
	V_{VH3}, V_{VH4}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	–9.6	–9.0	–8.5	V	2	$V_{VL}=(V_{VL3}+V_{VL4})/2$
	V φ V	8.3	9.0	9.65	V	2	V φ V=V_{VHn} –V_{VLn} (n=1 to 4)
	| V_{VH1} –V_{VH2} |			0.1	V	2	
	V_{VH3} –V_{VH}	–0.25		0.1	V	2	
	V_{VH4} –V_{VH}	–0.25		0.1	V	2	
	V_{VHH}			0.5	V	2	High level coupling
	V_{VHL}			0.5	V	2	High level coupling
	V_{VLH}			0.5	V	2	Low level coupling
	V_{VLL}			0.5	V	2	Low level coupling
Horizontal transfer clock voltage	V φ H	4.75	5.0	5.25	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
Horizontal final stage transfer clock voltage	V_{LHH}	4.45	5.0	5.55	V	4	
	V_{LHL}	–4.7	–4.0	–3.5	V	4	
	V φ LH	8.0	9.0	10.0	V	4	
Reset gate clock voltage	V φ RG	4.5	5.0	5.5	V	5	*6
	V_{RGLH} –V_{RGLL}			0.8	V	5	Low level coupling
Substrate clock voltage	V φ SUB	23.0	24.0	25.0	V	6	

*6 No adjustment of reset gate clock voltage is necessary when reset gate clock is driven as indicated below. In this case, reset gate clock voltage set point displayed on back of image sensor has no meaning.

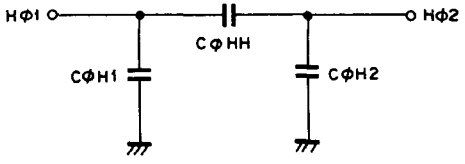
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Reset gate clock voltage	V_{RGL}	–0.2	0	0.2	V	5	
	$V\phi_{RG}$	8.5	9.0	9.5	V	5	

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi_{V1}$, $C\phi_{V3}$		1800		pF	
	$C\phi_{V2}$, $C\phi_{V4}$		2200		pF	
Capacitance between vertical transfer clocks	$C\phi_{V12}$, $C\phi_{V34}$		450		pF	
	$C\phi_{V23}$, $C\phi_{V41}$		270		pF	
Capacitance between horizontal transfer clock and GND	$C\phi_{H1}$, $C\phi_{H2}$		62		pF	
Capacitance between horizontal transfer clocks	$C\phi_{HH}$		47		pF	
Capacitance between horizontal final stage transfer clock and GND	$C\phi_{LH}$		8		pF	
Capacitance between reset gate clock and GND	$C\phi_{RG}$		8		pF	
Capacitance between substrate clock and GND	$C\phi_{SUB}$		400		pF	
Vertical transfer clock serial resistor	R_1, R_2, R_3, R_4		68		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	



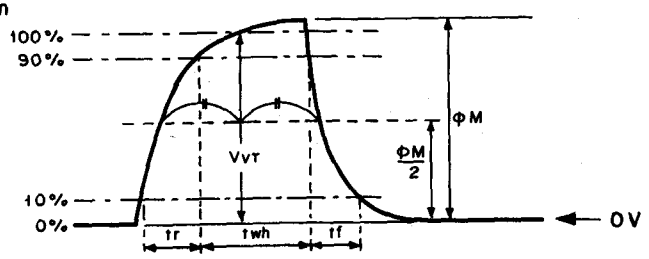
Vertical transfer clock equivalent circuit



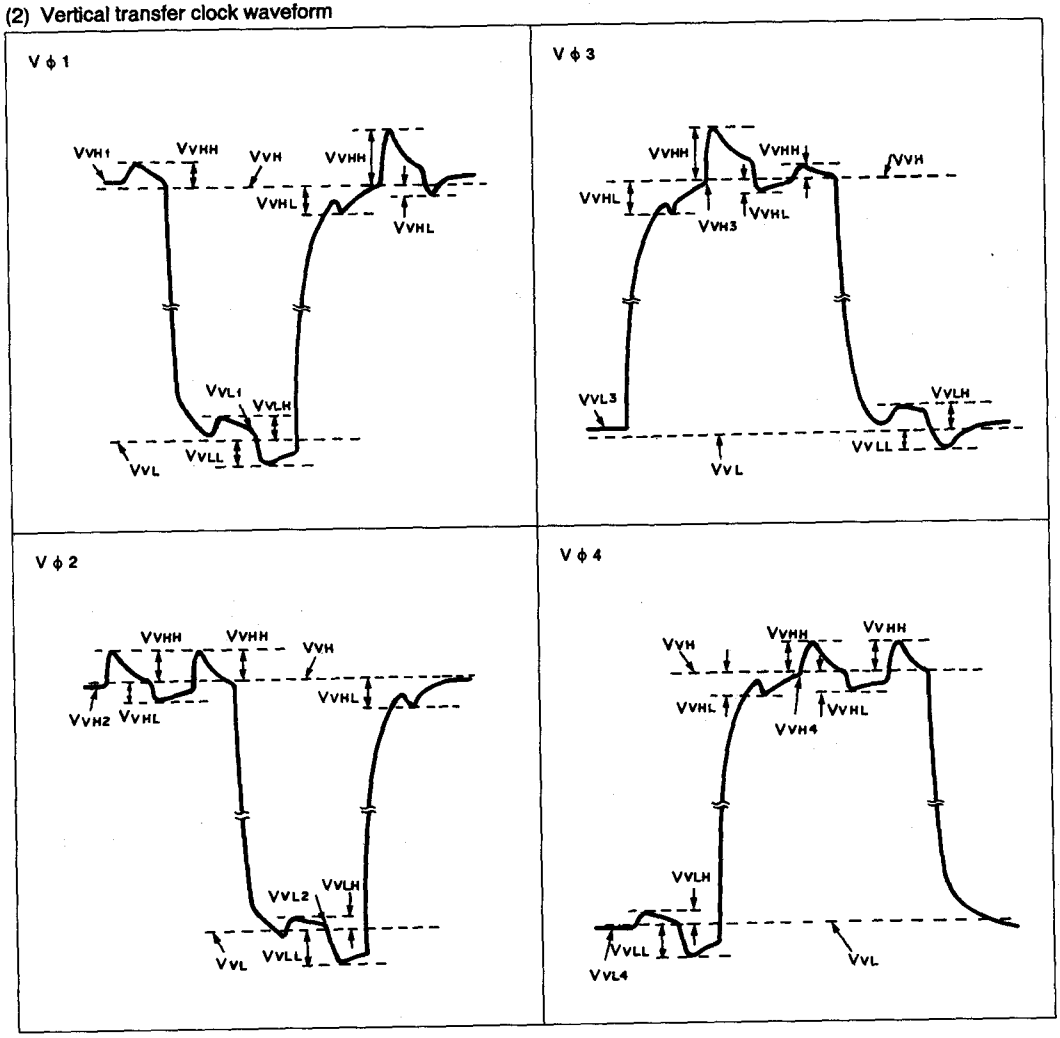
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

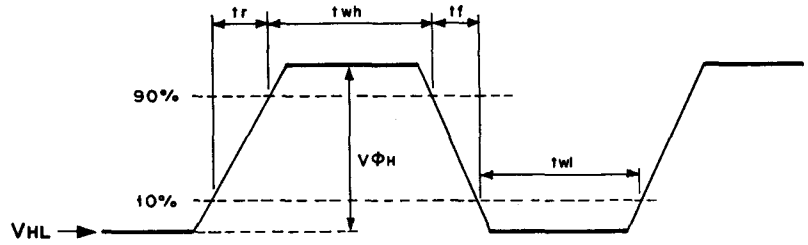
(1) Read out clock waveform



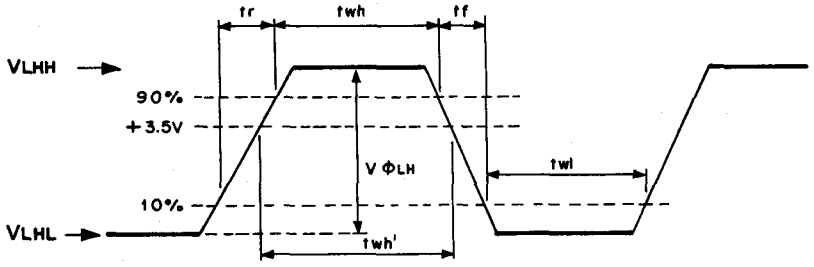
(2) Vertical transfer clock waveform



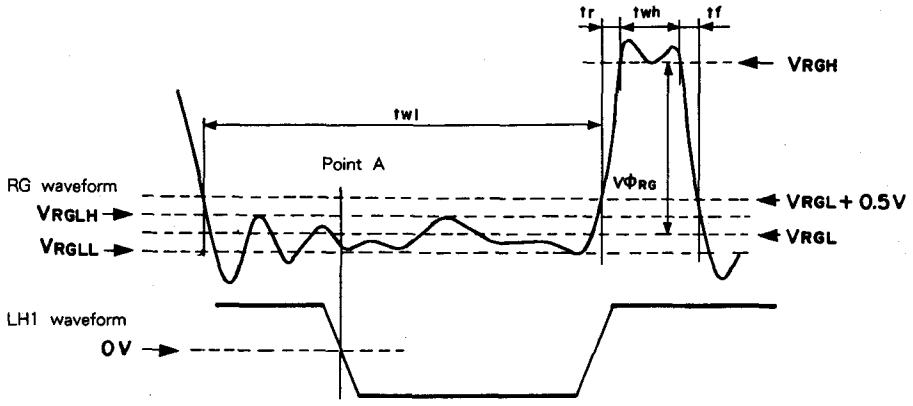
(3) Horizontal transfer clock waveform diagram



(4) Horizontal final stage transfer clock waveform diagram



(5) Reset gate clock waveform diagram



V_{RGLH} is the maximum value and V_{RGLL} the minimum value of the coupling waveform in the period from Point A in the diagram above to RG rise.

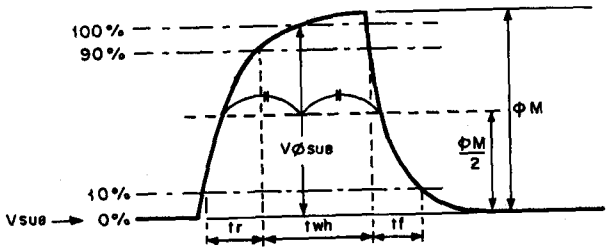
V_{RGL} is the mean value for V_{RGLH} and V_{RGLL}.

$$V_{RGL}=(V_{RGLH}+V_{RGLL})/2$$

V_{RGH} is the minimum value for twh period.

$$V\phi_{RG}=V_{RGH}-V_{RGL}$$

(6) Substrate clock waveform



Clock Switching Characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	VT	2.3	2.5						0.5			0.5		µs	During read out
Vertical transfer clock	Vφ1, Vφ2, Vφ3, Vφ4										0.015		0.25	µs	*7
Horizontal transfer clock	Hφ		20			20			15	19	*8	15	19	ns	During imaging
Horizontal final stage clock	LHφ		24		22	27			10			9		ns	During imaging
Horizontal transfer/horizontal final stage clock	Hφ1, LHφ		5.38						0.01			0.01		µs	During parallel serial conversion.
Horizontal transfer clock	Hφ2					5.38			0.01			0.01		µs	
Reset gate clock	φRG	11	13			51			3			3		ns	
Substrate clock	φSUB	1.5	1.8							0.5			0.5	µs	During charge

*7 When vertical transfer clock driver CXD1250 is in use.

*8 tf ≧ tr –2 ns

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	Hφ	16	20		ns	*9
Horizontal transfer/horizontal final stage clock	Hφ2, LHφ	15	20		ns	*10

*9 "two" is the overlap period of horizontal transfer clocks Hφ1 and Hφ2's twh and twl.

*10 "two" is the overlap period of horizontal transfer clock Hφ2's twl and horizontal final stage transfer clock LHφ's twh′ .

Operating Characteristics

(Ta=25℃)

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	140	180		mV	1	
Saturation signal	Vsat	450			mV	2	Ta=60℃
Smear	Sm		0.009	0.015	%	3	
Video signal shading	SH			20	%	4	Zone 0, I
				25	%	4	Zone 0 to II'
Dark signal	Vdt			2	mV	5	Ta=60℃
Dark signal shading	Δ Vdt			1	mV	6	Ta=60℃
Flicker	F			2	%	7	
Lag	Lag			0.5	%	8	

Zone Chart of Video Signal Shading

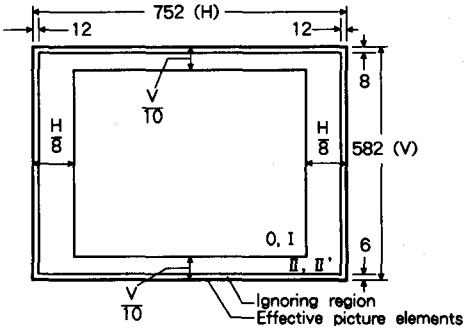


Image Sensor Characteristics Test Method

◎ Test conditions

① Through the following tests the substrate voltage and reset gate clock voltage are set to the value displayed on the device, while the device drive conditions are at the typical value of the bias and clock voltage conditions.

② Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OB) is set as the reference, the values obtained at Ⓐ point in the figure at the Drive Circuit are utilized.

◎ Definition of standard imaging conditions

① Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 cd/ m², color temperature 3200K Halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t=1.0mm) as IR cut filter and image at F8. At this time, light intensity to sensor receiving surface is defined as standard sensitivity testing light intensity. Signal output average value in this condition is called V_A.

② Standard imaging condition II: Image a light source (color temperature of 3200K) which uniformity of brightness is within 2% at all angles. Use a testing standard lens with CM500S (t=1.0mm) as IR cut filter. The light intensity is adjusted to the value indicated in each testing item by lens diaphragm.

1. Sensitivity
   Set to standard imaging condition I and measure signal output (S) at the center of the screen.

2. Saturation signal
   Set to standard imaging condition II. Adjust light intensity to 10 times that of signal output average value (V_A), then test signal output minimum value.

3. Smear
   Set to standard imaging condition II. Adjust light intensity to 500 times that of signal output average value (V_A). Stop read out clock. When the charge drain executed by the electric shutter at the respective H blankings takes place, test the maximum value Vsm of signal output.

   $$Sm=\frac{Vsm}{V_A}\times\frac{1}{500}\times\frac{1}{10}\times 100\ (\%)\ (1/10V)$$

4. Video signal shading
   Set to standard imaging condition II. Adjust light intensity to signal output average value (V_A) with lens diaphragm at F5.6 to F8. Then test maximum (Vmax) and minimum (Vmin) values of signal output.

   $SH=(Vmax-Vmin)/V_A\times 100\ (\%)$

5. Dark signal
   Test signal output average value Vdt when the device ambient temperature is at 60 ℃ and light is obstructed with horizontal idle transfer level as reference.

6. Dark signal shading
   Following 5, test maximum (Vdmax) and minimum (Vdmin) values of dark signal output.

   $\Delta Vdt=Vdmax-Vdmin$

7. Flicker

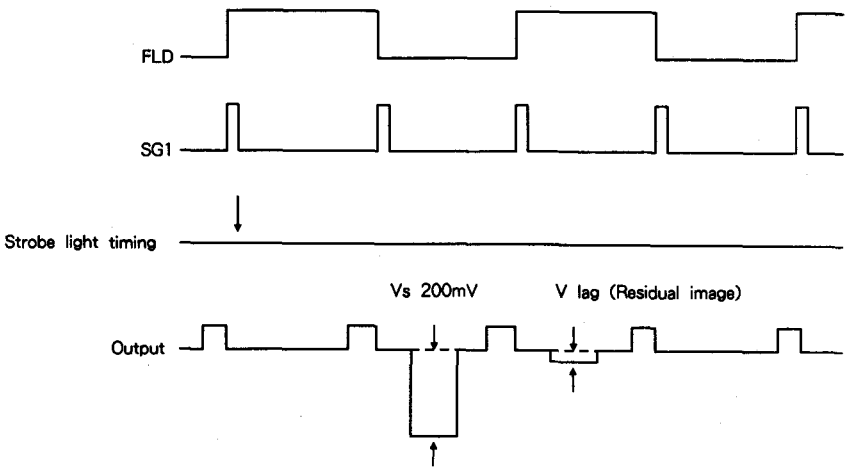
Set to standard imaging condition II. Adjust light intensity to signal output average value (V_A). Then test the signal output difference (Δ Vf) between even field and odd field.

$$F=(\Delta Vf/V_A) \times 100\ (\%)$$

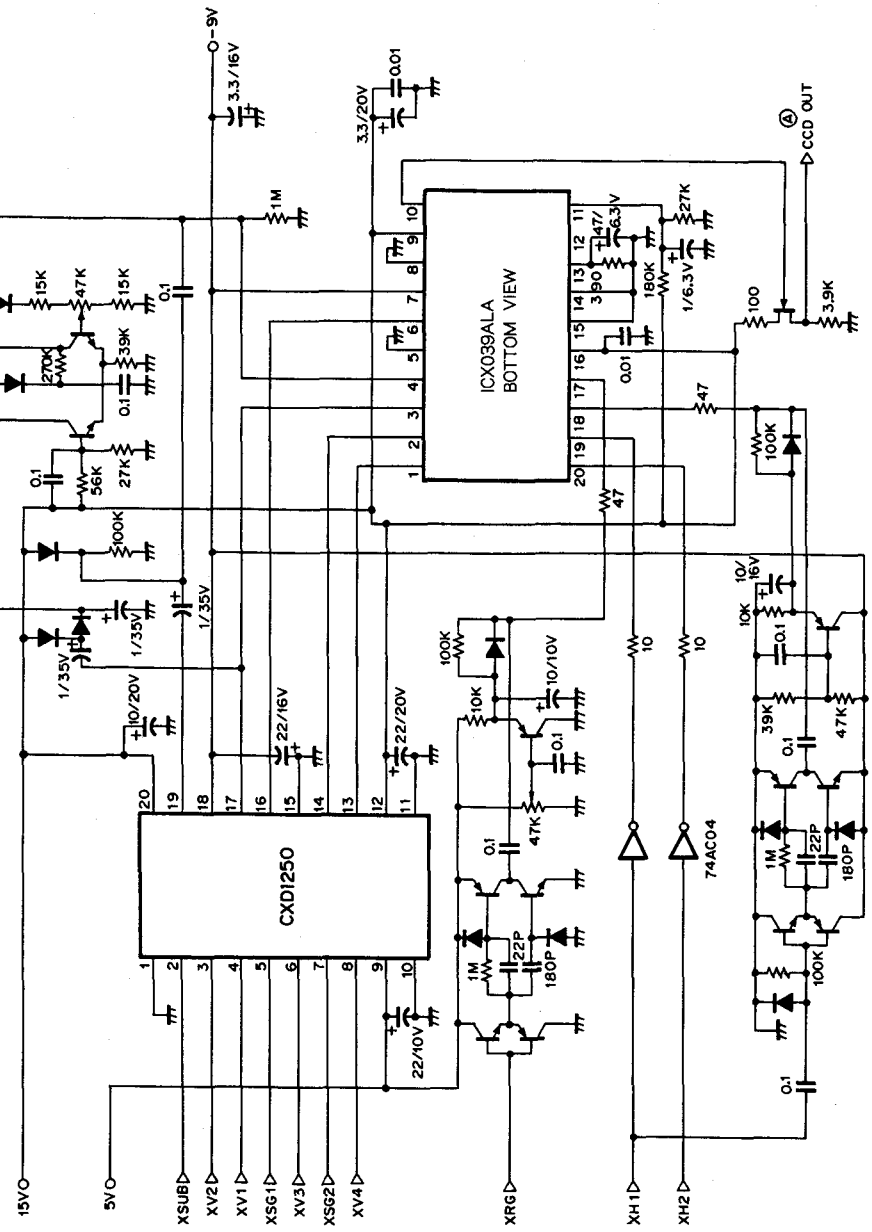
8. Residual image

Adjust signal output value (Vs) by strobe light to 200mV. Then light a stroboscopic tube with the following timing and test the residual image (Vlag).

$$Lag = (Vlag/Vs) \times 100\ (\%)$$

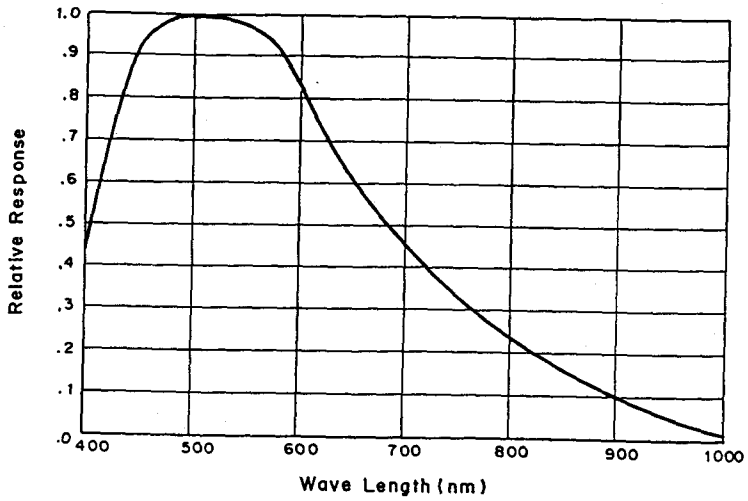


Drive Circuit

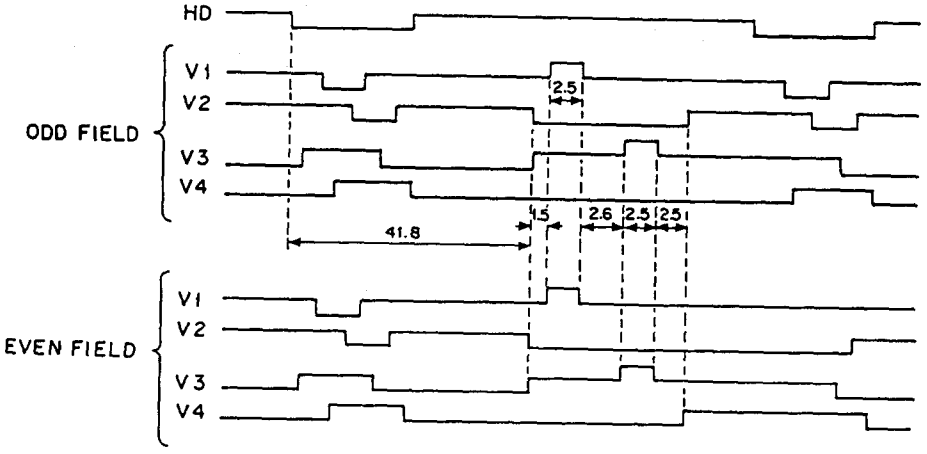


Spectral Sensitivity Characteristics

(Excluding light source characteristics, including lens characteristics)

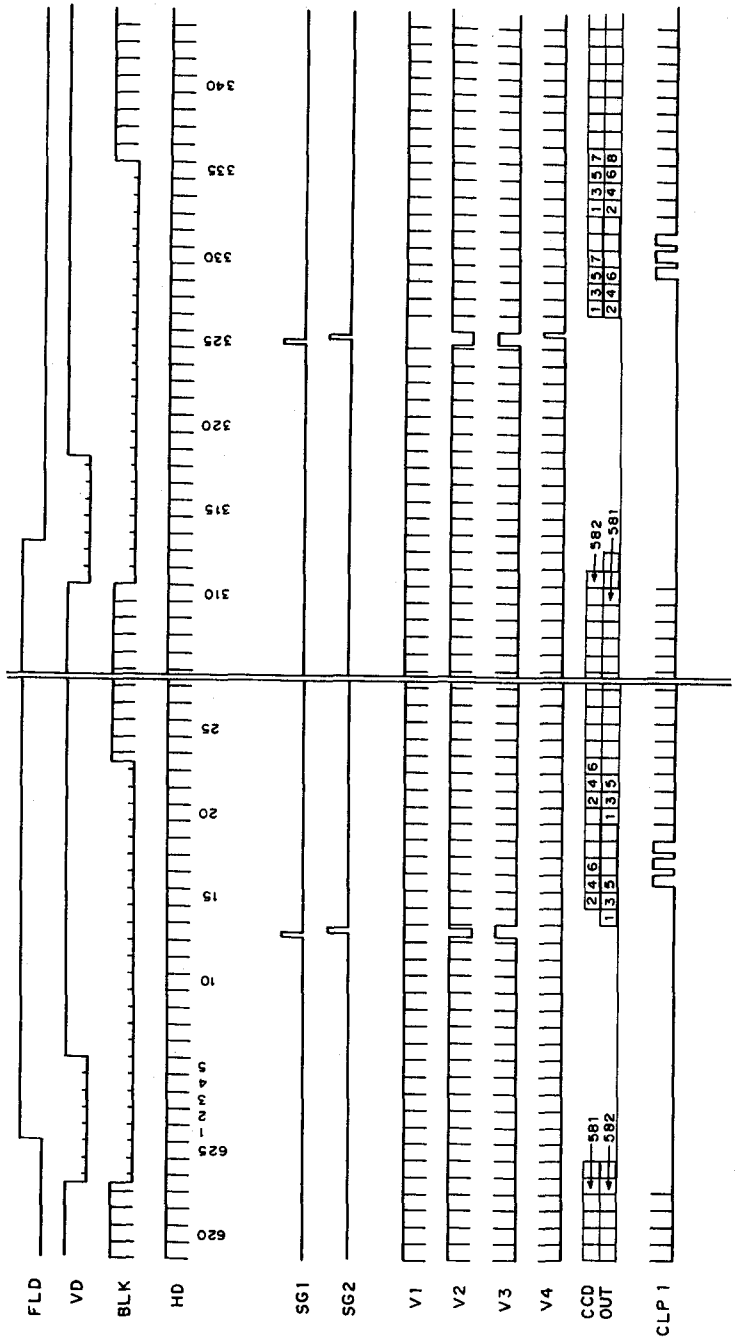


Using read out clock timing chart



Unit : µs

Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)

Handling Instructions

1) Static charge prevention
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensor.
   e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
   a) Make sure the package temperature does not exceed 80 °C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an imaging device do not use a solder suction equipment. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
   a) Operate in clean environments (around class 1000 will be appropriate).
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

SONY

ICX044ALA

1/3 inch CCD Image Sensor for EIA B/W Camera

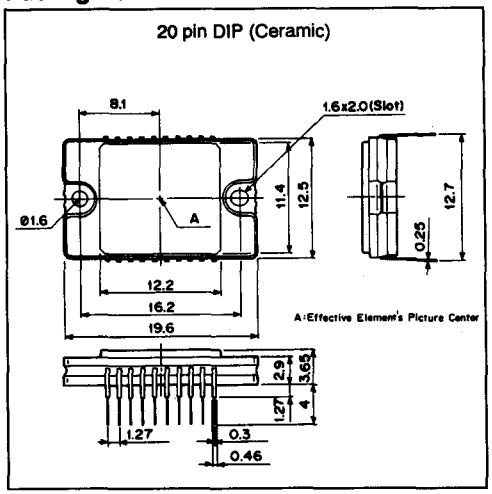
Description

The ICX044ALA is an interline transfer CCD solid-state image sensor suitable for EIA 1/3 inch B/W video cameras. High sensitivity is achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.

This chip features a field integration read out system, an electronic shutter with variable charge-storage time and 20pin Cer-DIP Package.

Package Outline

Unit : mm

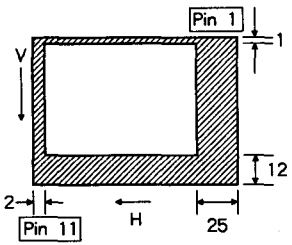


Features

- High sensitivity and low dark current
- Consecutive various speed shutter 1/60s. (Typ.), 1/100s. to 1/10000s.
- Low smear
- High antiblooming
- Horizontal register 5V drive
- Reset gate 5V drive

Device Structure

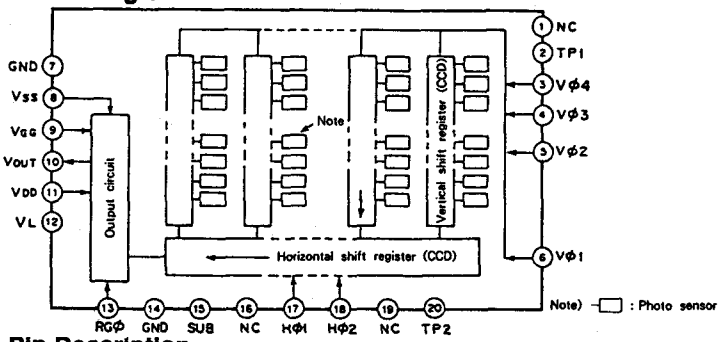
- Optical size 1/3 inch format
- Number of effective pixels
  510 (H) × 492 (V) Approx. 250k pixels
- Number of total pixels
  537 (H) × 505 (V) Approx. 270k pixels
- Interline transfer CCD image sensor
- Chip size 6.3mm (H) × 5.4mm (V)
- Unit cell size 9.6 µm (H) × 7.5 µm (V)
- Optical black Horizontal (H) direction Front 2 pixels Rear 25 pixels
  Vertical (V) direction Front 12 pixels Rear 1 pixels
- Number of dummy bits Horizontal 16
  Vertical 1 (even field only)
- Substrate material silicon



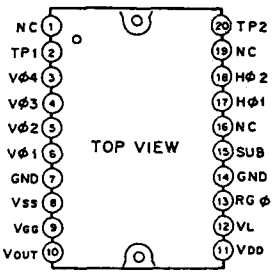
Optical black position (Top View)

E91541A1Y – ST

Block Diagram



Pin Configuration



Pin Description

No.	Symbol	Description		No.	Symbol	Description
1	NC			11	V_{DD}	Output amplifier drain supply
2	TP_1	Input bias		12	V_L	Protective transistor bias
3	$V\phi_4$	Vertical register transfer clock		13	RG ϕ	Reset gate clock
4	$V\phi_3$	Vertical register transfer clock		14	GND	GND
5	$V\phi_2$	Vertical register transfer clock		15	SUB	Substrate (Overflow drain)
6	$V\phi_1$	Vertical register transfer clock		16	NC	
7	GND	GND		17	$H\phi_1$	Horizontal register transfer clock
8	Vss	Output amplifier source		18	$H\phi_2$	Horizontal register transfer clock
9	V_{GG}	Output amplifier gate bias		19	NC	
10	V_{OUT}	Signal output		20	TP_2	Input bias

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB-GND		–0.3 to +55	V	
Supply voltage	V_{DD}, V_{OUT}, Vss, TP1, TP2 – GND	–0.3 to +18	V	
	V_{DD}, V_{OUT}, Vss, TP1, TP2 – SUB	–55 to +10	V	
Clock input voltage	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $H\phi_1$, $H\phi_2$ – GND	–15 to +20	V	
	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $H\phi_1$, $H\phi_2$ – SUB	–65 to +10	V	
Voltage difference between vertical clock input pins		to+15	V	*
Voltage difference between horizontal clock input pins		to+17	V	
$H\phi_1$, $H\phi_2$ – $V\phi_4$		–17 to +17	V	
RG, V_{GG} – GND		–10 to +15	V	
RG, V_{GG} – SUB		–55 to +10	V	
V_L – SUB		–65 to +0.3	V	
Beside GND, SUB-V_L		–0.3 to +30	V	
Storage temperature		–30 to +80	℃	
Operating temperature		–10 to +60	℃	

* +27V (Max.) when clock width<10 μs, duty factor<0.1%.

Bias Conditions

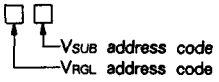
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD}	14.55	15.0	15.45	V	
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	V_{SS}	Ground through 680 Ω resistor				± 5%
Substrate voltage adjustment range	V_{SUB}	9.0		18.5	V	*1
Fluctuation range after substrate voltage adjustment	Δ V_{SUB}	−3		+3	%	
Reset gate clock voltage adjustment range	V_{RGL}	1.0		4.0	V	*1
Fluctuation range after reset gate clock voltage adjustment	Δ V_{RGL}	−3		+3	%	
Protective transistor bias	V_L	*2				
Input bias	TP_1, TP_2	14.55	15.0	15.45	V	TP_1=TP_2

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		3		mA	
Input current	I_{IN1}			1	μA	*3
Input current	I_{IN2}			10	μA	*4

*** 1)** Substrate voltage (V_{SUB}) • reset gate clock voltage (V_{RGL}) setting value display.
Setting values of substrate voltage and reset gate clock voltage are displayed at the back of the device through a code address. Adjust substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) to the displayed voltage. Fluctuation range after adjustment is ± 3%.

V_{SUB} code address–1 digit display
V_{RGL} code address–1 digit display



Code addresses and actual numerical values correspond to each other as follows.

V_{RGL} address code	1	2	3	4	5	6	7
Numerical value	1.0	1.5	2.0	2.5	3.0	3.5	4.0

V_{SUB} address code	E	f	G	h	J	K	L	m	N	P	Q	R	S	T	U	V	W	X	Y	Z
Numerical value	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5

<Example> "5L" → V_{RGL}=3.0V
V_{SUB}=12.0V

*** 2)** V_L setting is the V_{VL} voltage of the vertical transfer clock waveform.

* 3) 1. Current to each pin when 18V is applied to V_{DD}, V_{OUT}, Vss, SUB, TP_1 and TP_2 pins, while pins that are not tested are grounded.
2. Current to each pins when 20V is applied sequentially to $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $H\phi_1$ and $H\phi_2$, while pins that are not tested are grounded. However, 20V is applied to SUB.
3. Current to each pins when 15V is applied sequentially to pins RG and V_{GG}, while pins that are not tested are grounded. However, 15V is applied to SUB.
4. Current to V_L pin when it is grounded, while 30V is applied to all pins except pins that are not tested. However, GND and SUB pins are kept open.

* 4) Current to SUB pin when 55V is applied to SUB pin, while pins that are not tested are grounded.

Clock Voltage Conditions

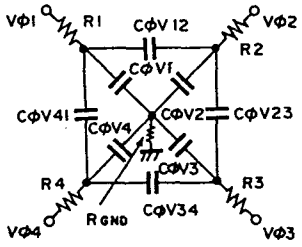
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Read out clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2} V_{VH3}, V_{VH4}	− 0.2	0	0.2	V	2	V_{VH}= (V_{VH1}+V_{VH2}) /2
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	− 9.6	− 9.0	− 8.5	V	2	V_{VL}= (V_{VL3}+V_{VL4}) /2
	$V\phi_V$	8.3	9.0	9.8	V	2	$V\phi_V$=V_{VHn} − V_{VLn} (n=1 to 4)
	|V_{VH1} − V_{VH2}|			0.1	V	2	
	V_{VH3} − V_{VH}	− 0.25		0.1	V	2	
	V_{VH4} − V_{VH}	− 0.25		0.1	V	2	
	V_{VHH}			0.5	V	2	High level coupling
	V_{VHL}			0.5	V	2	High level coupling
	V_{VLH}			0.5	V	2	Low level coupling
	V_{VLL}			0.5	V	2	Low level coupling
Horizontal transfer clock voltage	$V\phi_H$	4.5	5.0	5.25	V	3	
	V_{HL}	− 0.05	0	0.05	V	3	
Reset gate clock voltage	$V\phi_{RG}$	4.5	5.0	5.5	V	4	*
	V_{RGLH} − V_{RGLL}			0.8	V	4	Low level coupling
Substrate clock voltage	$V\phi_{SUB}$	23.0	24.0	25.0	V	5	

* No adjustment of reset gate clock voltage is necessary when reset gate clock is driven as indicated below. In this case, reset gate clock voltage set point displayed on back of image sensor has no meaning.

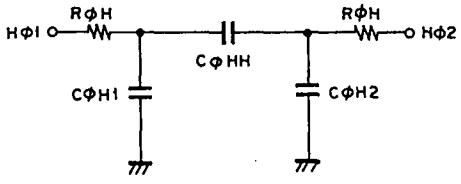
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Reset gate clock voltage	V_{RGL}	− 0.1	0	0.1	V	4	
	$V\phi_{RG}$	8.5	9.0	9.5	V	4	

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi_{V1}$, $C\phi_{V3}$		820		pF	
	$C\phi_{V2}$, $C\phi_{V4}$		1000		pF	
Capacitance between vertical transfer clocks	$C\phi_{V12}$, $C\phi_{V34}$		680		pF	
	$C\phi_{V23}$, $C\phi_{V41}$		470		pF	
Capacitance between horizontal transfer clock and GND	$C\phi_{H1}$, $C\phi_{H2}$		40		pF	
Capacitance between horizontal transfer clocks	$C\phi_{HH}$		40		pF	
Capacitance between reset gate clock and GND	$C\phi_{RG}$		5		pF	
Capacitance between substrate clock and GND	$C\phi_{SUB}$		270		pF	
Vertical transfer clock serial resistor	R_1, R_2, R_3, R_4		80		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock serial resistor	$R\phi_H$		20		Ω	



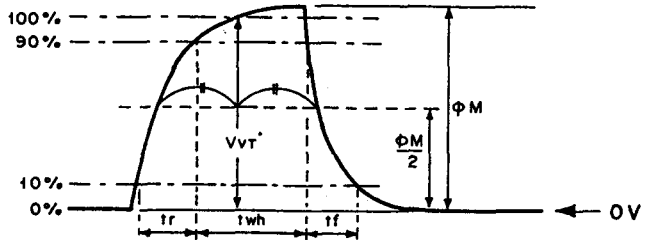
Vertical transfer clock equivalent circuit



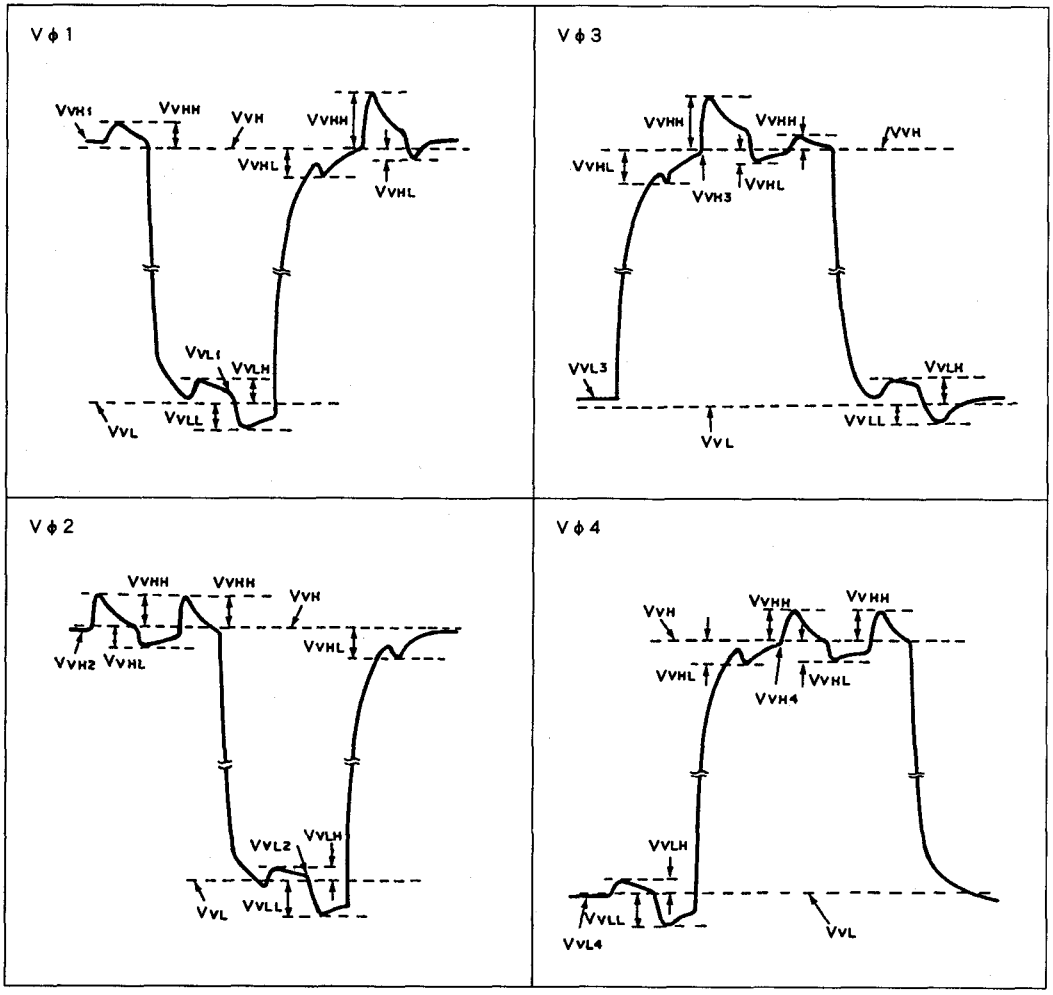
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

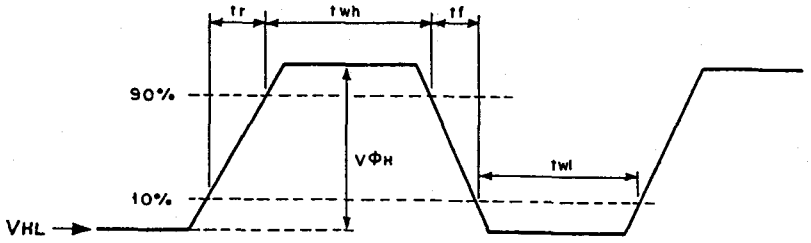
(1) Read out clock waveform



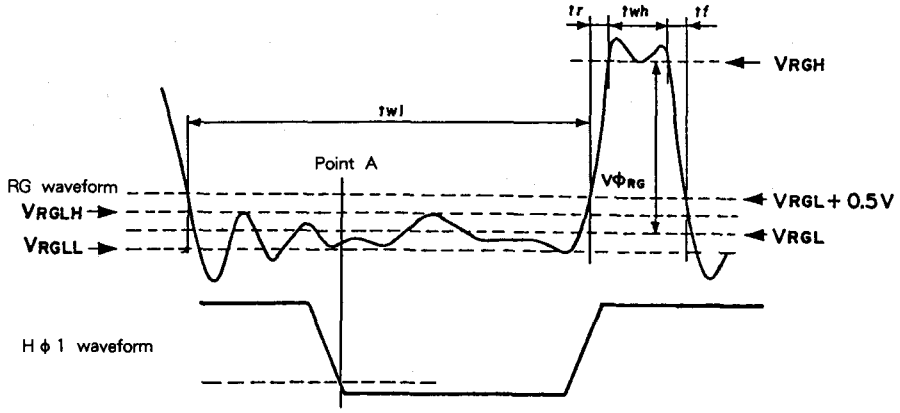
(2) Vertical transfer clock waveform



(3) Horizontal transfer clock waveform diagram



(4) Reset gate clock waveform diagram



VRGLH is the maximum value and VRGLL the minimum value of the coupling waveform in the period from Point A in the diagram above to RG rise.

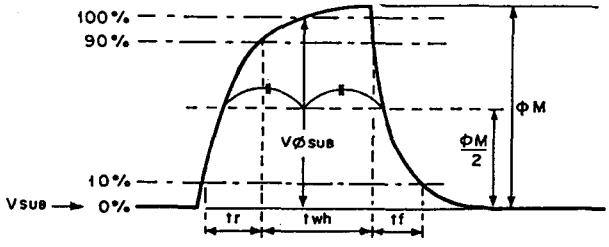
VRGL is the mean value for VRGLH and VRGLL.

$$V_{RGL} = (V_{RGLH} + V_{RGLL}) / 2$$

VRGH is the minimum value for twh period.

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

(5) Substrate clock waveform



Clock Switching Characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	V_T	2.3	2.5						0.5			0.5		µs	During read out
Vertical transfer clock	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$										0.015		0.25	µs	*1
Horizontal transfer clock	$H\phi$	37	41		38	42			12	15	*2	10	15	ns	During imaging
Horizontal transfer clock	$H\phi_1$		5.6						0.012			0.012		µs	During parallel serial conversion.
Horizontal transfer clock	$H\phi_2$					5.6			0.012			0.012		µs	
Reset gate clock	ϕ_{RG}	11	15		75	79			6.5			4.5		ns	
Substrate clock	ϕ_{SUB}	1.5	2.0							0.5			0.5	µs	During charge drain.

* 1) When vertical transfer clock driver CXD1250 is in use.
* 2) tf ≧ tr–2 ns

Image Sensor Characteristics

(Ta=25℃)

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	180	220		mV	1	
Saturation signal	Vsat	500			mV	2	Ta=60℃
Smear	Sm		0.007	0.012	%	3	
Video signal shading	SH			20	%	4	Zone 0, I
				25	%	4	Zone 0 to II'
Dark signal	Vdt			2	mV	5	Ta=60℃
Dark signal shading	Δ Vdt			1	mV	6	Ta=60℃
Flicker	F			2	%	7	
Lag	Lag			0.5	%	8	

Zone Chart of Video Signal Shading

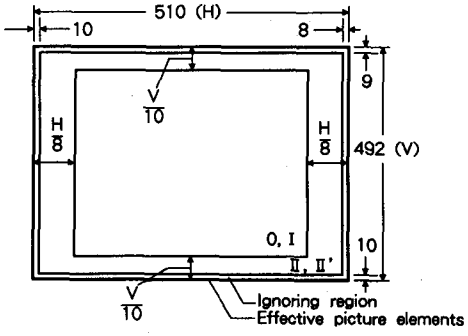


Image Sensor Characteristics Test Method

◎ Test conditions

① Through the following tests the substrate voltage and reset gate clock voltage are set to the value displayed on the device, while the device drive conditions are at the typical value of the bias and clock voltage conditions.

② Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OB) is set as the reference for the signal output which is taken as the signal output or the chroma signal output of the testing system.

◎ Definition of standard imaging conditions

① Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 cd/m², color temperature 3200K Halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t=1.0mm) as IR cut filter and image at F8.

② Standard imaging condition II: Image a light source (color temperature of 3200K) which uniformity of brightness is within 2% at all angles. Use a testing standard lens with CM500S (t=1.0mm) as IR cut filter. The light intensity is adjusted to the value indicated in each testing item by lens diaphragm.

1. Sensitivity
   Set to standard imaging condition I and measure signal (S) at the center of the screen.

2. Saturation signal
   Set to standard imaging condition II. Adjust light intensity to 10 times that of signal output average value (V_A=150mV), then test signal minimum value.

3. Smear
   Set to standard imaging condition II. Adjust light intensity to 500 times that of signal output average value (V_A=150mV). Stop read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the maximum value VSm of signal output.

$$Sm=\frac{VSm}{V_A}\times\frac{1}{500}\times\frac{1}{10}\times 100\ (\%)\ (1/10V)$$

4. Video signal shading
   Set to standard imaging condition II. Adjust light intensity to signal output average value (V_A=150mV) with lens diaphragm at F5.6 to F8. Then test maximum (Vmax) and minimum (Vmin) values of signal.

   $SH=(Vmax-Vmin)/V_A\times 100\ (\%)$

5. Dark signal
   Test signal output average value Vdt when the device ambient temperature is at 60°C and light is obstructed with horizontal idle transfer level as reference.

6. Dark signal shading
   Following 5, test maximum (Vdmax) and minimum (Vdmin) values of dark signal output.

   $\Delta Vdt=Vdmax-Vdmin$

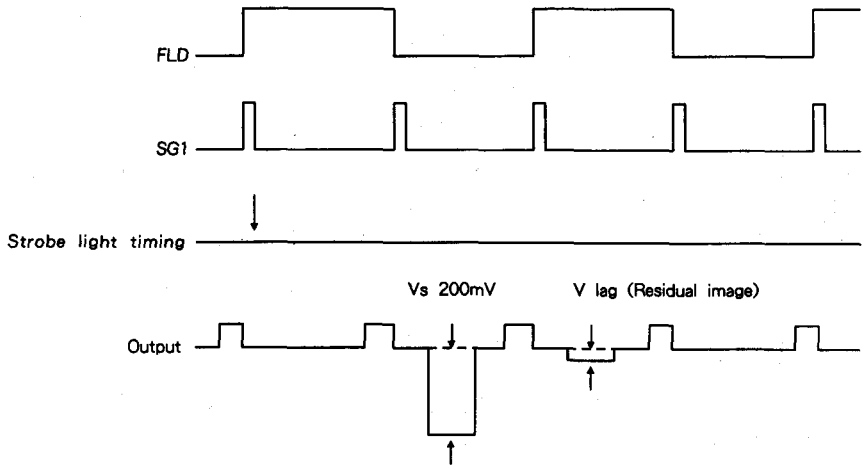
7. Flicker
   Set to standard imaging condition II. Adjust light intensity to signal output average value (V_A=150mV). Then test the signal difference (Δ Vf) between even field and odd field.

   $F=(\Delta Vf/V_A)\times 100\ (\%)$

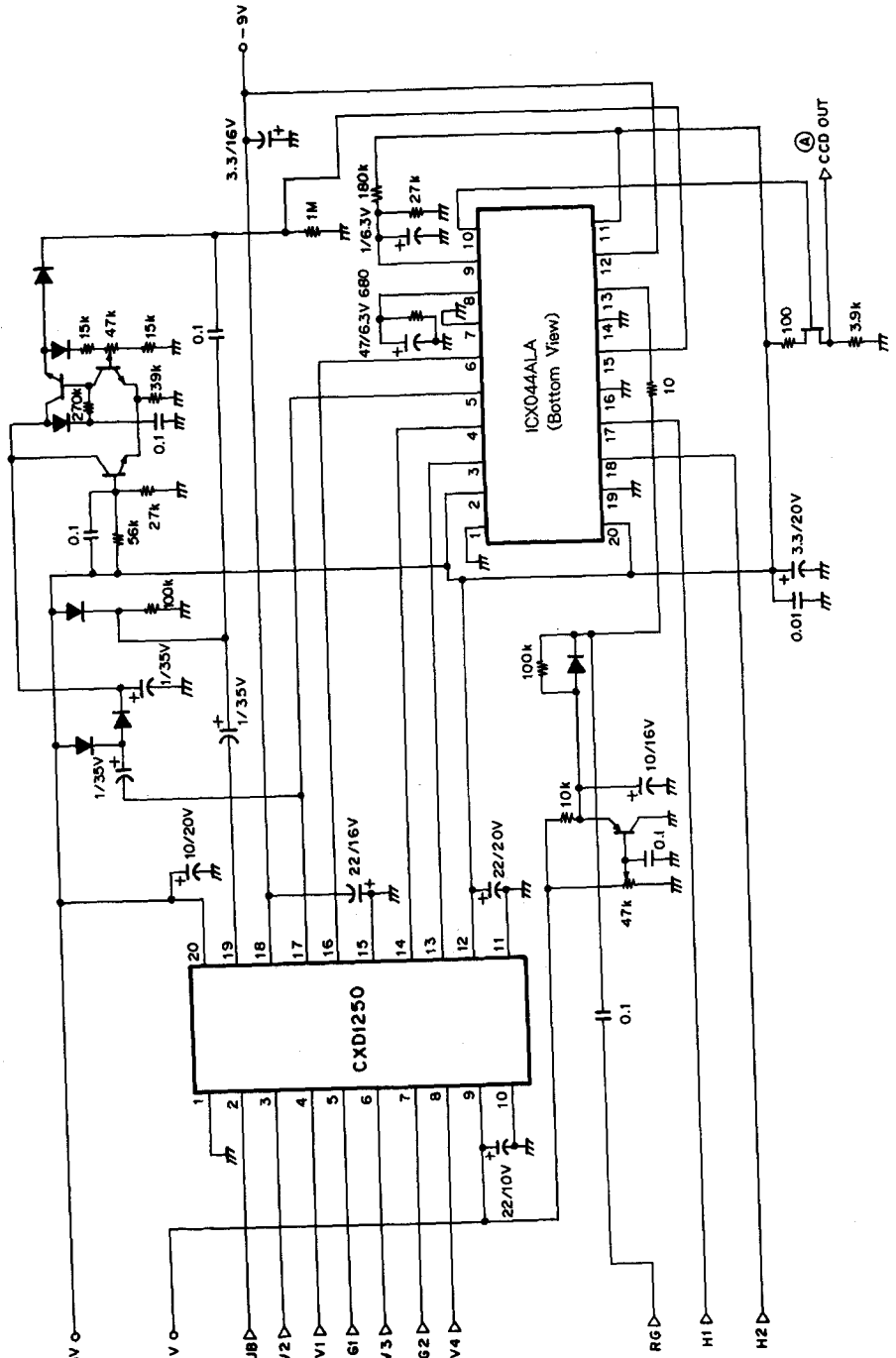
8. Residual image

Adjust signal output value (Vs) by strobe light to 200mV. Then light a stroboscopic tube with the following timing and test the residual image (Vlag).

Lag = (Vlag/Vs) × 100 (%)



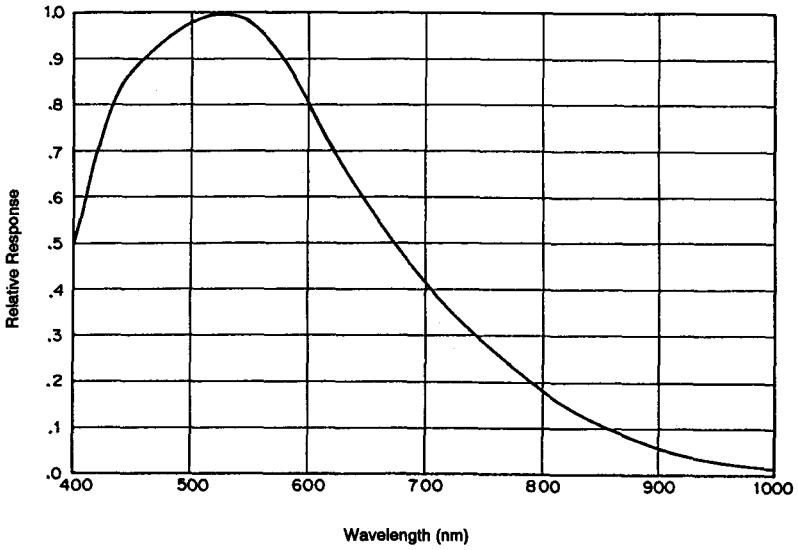
Drive Circuit



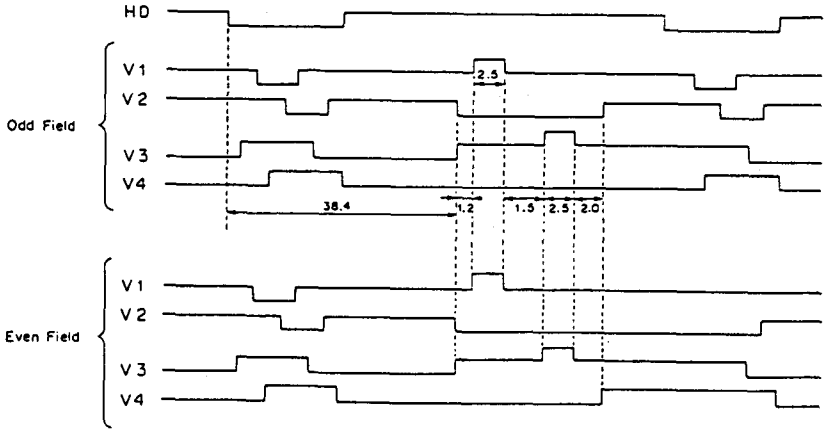
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Spectral Sensitivity Characteristics

(Excluding light source characteristics, including lens characteristics)

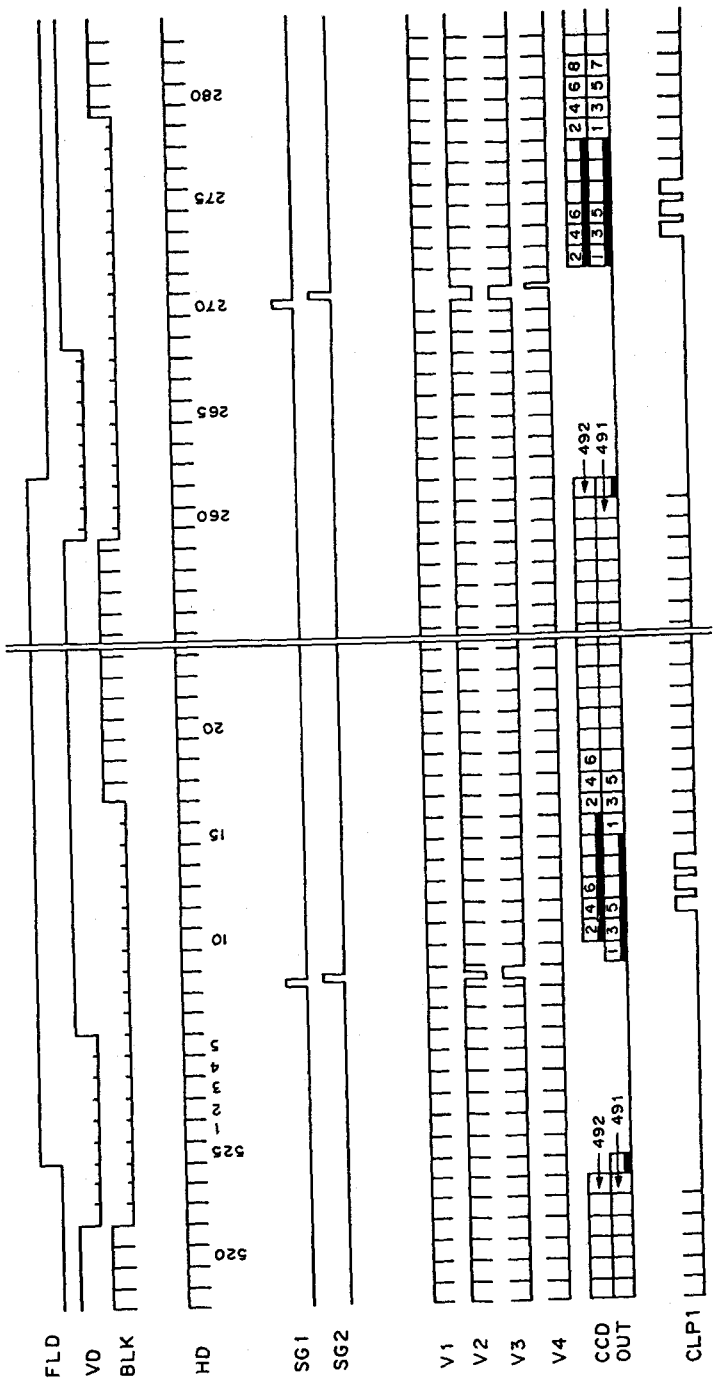


Sensor Read Out Clock Timing Chart

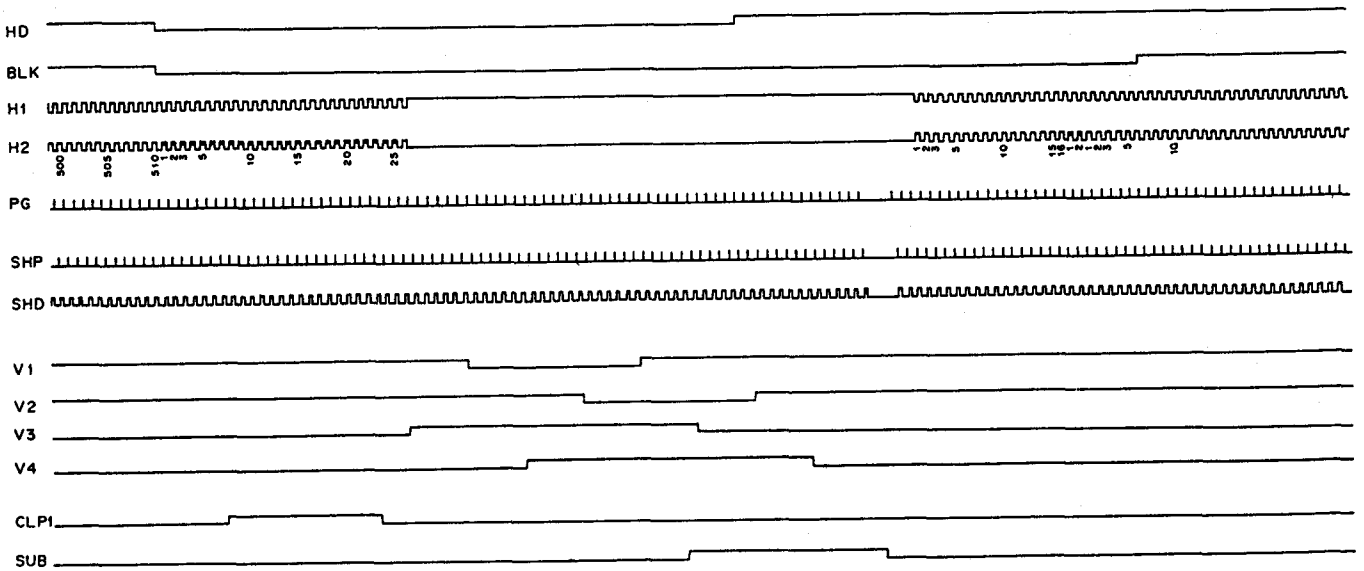


Unit : µs

Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



(During electronic shutter operation)

Handling Instructions

1) Static charge prevention
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensor.
   e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
   a) Make sure the package temperature does not exceed 80 °C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an imaging device do not use a solder suction equipment. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
   a) Operate in clean environments (around class 1000 will be appropriate).
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

SONY

ICX045ALA

1/3 inch CCD Image Sensor for CCIR B/W Camera

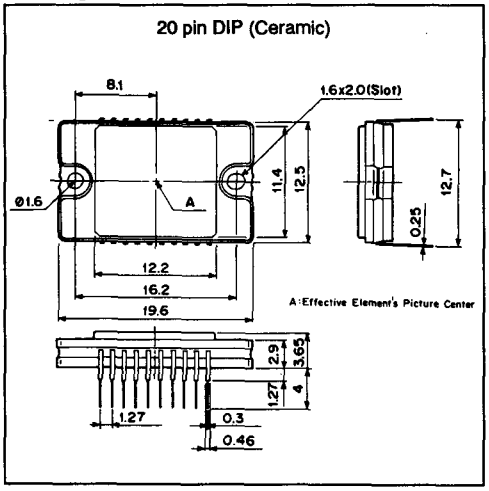
Description

The ICX045ALA is an interline transfer CCD solid-state image sensor suitable for CCIR 1/3 inch B/W video cameras. High sensitivity is achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.

This chip features a field integration read out system, an electronic shutter with variable charge-storage time and 20pin Cer-DIP Package.

Package Outline

Unit : mm

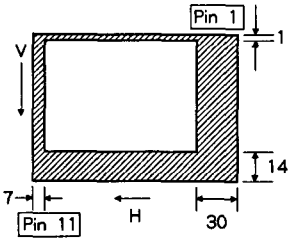


Features

- High sensitivity and low dark current
- Consecutive various speed shutter
  1/50s (Typ.), 1/100s to 1/10000s
- Low smear
- High antiblooming
- Horizontal register 5V drive
- Reset gate 5V drive

Device Structure

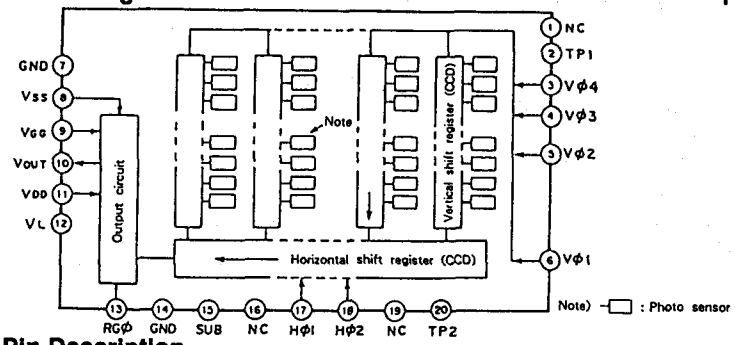
- Optical size 1/3 inch format
- Number of effective pixels
  500 (H) × 582 (V) Approx. 290k pixels
- Number of total pixels
  537 (H) × 597 (V) Approx. 320k pixels
- Interline transfer CCD image sensor
- Chip size 6.3mm (H) × 5.4mm (V)
- Unit cell size 9.8 µm (H) × 6.3 µm (V)
- Optical black Horizontal (H) direction Front 7 pixels Rear 30 pixels
  Vertical (V) direction Front 14 pixels Rear 1 pixels
- Number of dummy bits Horizontal 16
  Vertical 1 (even field only)
- Substrate material silicon



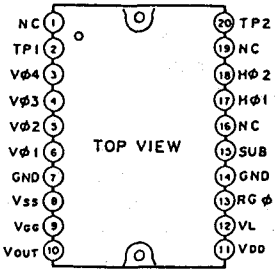
Optical black position (Top View)

E91543A1Y – ST

Block Diagram



Pin Configuration



Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	NC		11	V_{DD}	Output amplifier drain supply
2	TP_1	Input bias	12	V_L	Protective transistor bias
3	V φ 4	Vertical register transfer clock	13	RG φ	Reset gate clock
4	V φ 3	Vertical register transfer clock	14	GND	GND
5	V φ 2	Vertical register transfer clock	15	SUB	Substrate (Overflow drain)
6	V φ 1	Vertical register transfer clock	16	NC	
7	GND	GND	17	H φ 1	Horizontal register transfer clock
8	Vss	Output amplifier source	18	H φ 2	Horizontal register transfer clock
9	V_{GG}	Output amplifier gate bias	19	NC	
10	V_{OUT}	Signal output	20	TP_2	Input bias

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB-GND		−0.3 to +55	V	
Supply voltage	V_{DD}, V_{OUT}, Vss, TP1, TP2 − GND	−0.3 to +18	V	
	V_{DD}, V_{OUT}, Vss, TP1, TP2 − SUB	−55 to +10	V	
Clock input voltage	V φ 1, V φ 2, V φ 3, V φ 4, H φ 1, H φ 2 − GND	−15 to +20	V	
	V φ 1, V φ 2, V φ 3, V φ 4, H φ 1, H φ 2 − SUB	−65 to +10	V	
Voltage difference between vertical clock input pins		to+15	V	*
Voltage difference between horizontal clock input pins		to+17	V	
H φ 1, H φ 2 − V φ 4		−17 to +17	V	
RG, V_{GG} − GND		−10 to +15	V	
RG, V_{GG} − SUB		−55 to +10	V	
V_L − SUB		−65 to +0.3	V	
Beside GND, SUB-V_L		−0.3 to +30	V	
Storage temperature		−30 to +80	°C	
Operating temperature		−10 to +60	°C	

* +27V (Max.) when clock width<10 μs, duty factor<0.1%.

Bias Conditions

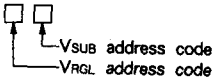
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD}	14.55	15.0	15.45	V	
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	V_{SS}	Ground through 680 Ω resistor				± 5%
Substrate voltage adjustment range	V_{SUB}	9.0		18.5	V	*1
Fluctuation range after substrate voltage adjustment	Δ V_{SUB}	−3		+3	%	
Reset gate clock voltage adjustment range	V_{RGL}	1.0		4.0	V	*1
Fluctuation range after reset gate clock voltage adjustment	Δ V_{RGL}	−3		+3	%	
Protective transistor bias	V_L	*2				
Input bias	TP_1, TP_2	14.55	15.0	15.45	V	TP_1=TP_2

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		3		mA	
Input current	I_{IN1}			1	μA	*3
Input current	I_{IN2}			10	μA	*4

*** 1)** Substrate voltage (V_{SUB}) • reset gate clock voltage (V_{RGL}) setting value display.
Setting values of substrate voltage and reset gate clock voltage are displayed at the back of the device through a code address. Adjust substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) to the displayed voltage. Fluctuation range after adjustment is ± 3%.

V_{SUB} code address–1 digit display
V_{RGL} code address–1 digit display



Code addresses and actual numerical values correspond to each other as follows.

V_{RGL} address code	1	2	3	4	5	6	7
Numerical value	1.0	1.5	2.0	2.5	3.0	3.5	4.0

V_{SUB} address code	E	f	G	h	J	K	L	m	N	P	Q	R	S	T	U	V	W	X	Y	Z
Numerical value	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5

<Example> "5L" → V_{RGL}=3.0V
V_{SUB}=12.0V

*** 2)** V_L setting is the V_{VL} voltage of the vertical transfer clock waveform.

*** 3)** 1. Current to each pin when 18V is applied to V_{DD}, V_{OUT}, Vss, SUB, TP_1 and TP_2 pins, while pins that are not tested are grounded.
2. Current to each pins when 20V is applied sequentially to $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $H\phi_1$ and $H\phi_2$, while pins that are not tested are grounded. However, 20V is applied to SUB.
3. Current to each pins when 15V is applied sequentially to pins RG and V_{GG}, while pins that are not tested are grounded. However, 15V is applied to SUB.
4. Current to V_L pin when it is grounded, while 30V is applied to all pins except pins that are not tested. However, GND and SUB pins are kept open.

*** 4)** Current to SUB pin when 55V is applied to SUB pin, while pins that are not tested are grounded.

Clock Voltage Conditions

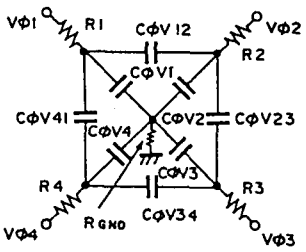
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Read out clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2} V_{VH3}, V_{VH4}	− 0.2	0	0.2	V	2	V_{VH}= (V_{VH1}+V_{VH2}) /2
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	− 9.6	− 9.0	− 8.5	V	2	V_{VL}= (V_{VL3}+V_{VL4}) /2
	$V\phi_V$	8.3	9.0	9.8	V	2	$V\phi_V$=V_{VHn} − V_{VLn} (n=1 to 4)
	|V_{VH1} − V_{VH2}|			0.1	V	2	
	V_{VH3} − V_{VH}	− 0.25		0.1	V	2	
	V_{VH4} − V_{VH}	− 0.25		0.1	V	2	
	V_{VHH}			0.5	V	2	High level coupling
	V_{VHL}			0.5	V	2	High level coupling
	V_{VLH}			0.5	V	2	Low level coupling
	V_{VLL}			0.5	V	2	Low level coupling
Horizontal transfer clock voltage	$V\phi_H$	4.5	5.0	5.25	V	3	
	V_{HL}	− 0.05	0	0.05	V	3	
Reset gate clock voltage	$V\phi_{RG}$	4.5	5.0	5.5	V	4	*
	V_{RGLH} − V_{RGLL}			0.8	V	4	Low level coupling
Substrate clock voltage	$V\phi_{SUB}$	23.0	24.0	25.0	V	5	

* No adjustment of reset gate clock voltage is necessary when reset gate clock is driven as indicated below. In this case, reset gate clock voltage set point displayed on back of image sensor has no meaning.

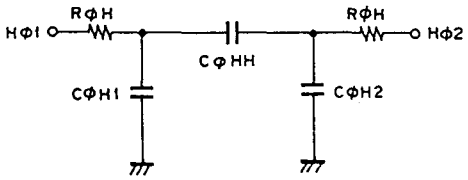
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Reset gate clock voltage	V_{RGL}	− 0.1	0	0.1	V	4	
	$V\phi_{RG}$	8.5	9.0	9.5	V	4	

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi_{V1}$, $C\phi_{V3}$		820		pF	
	$C\phi_{V2}$, $C\phi_{V4}$		1000		pF	
Capacitance between vertical transfer clocks	$C\phi_{V12}$, $C\phi_{V34}$		680		pF	
	$C\phi_{V23}$, $C\phi_{V41}$		470		pF	
Capacitance between horizontal transfer clock and GND	$C\phi_{H1}$, $C\phi_{H2}$		40		pF	
Capacitance between horizontal transfer clocks	$C\phi_{HH}$		40		pF	
Capacitance between reset gate clock and GND	$C\phi_{RG}$		5		pF	
Capacitance between substrate clock and GND	$C\phi_{SUB}$		270		pF	
Vertical transfer clock serial resistor	R_1, R_2, R_3, R_4		80		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock serial resistor	$R\phi_H$		20		Ω	



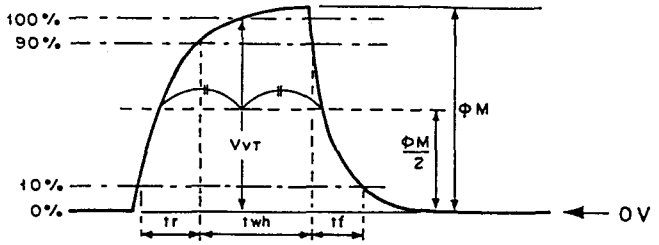
Vertical transfer clock equivalent circuit



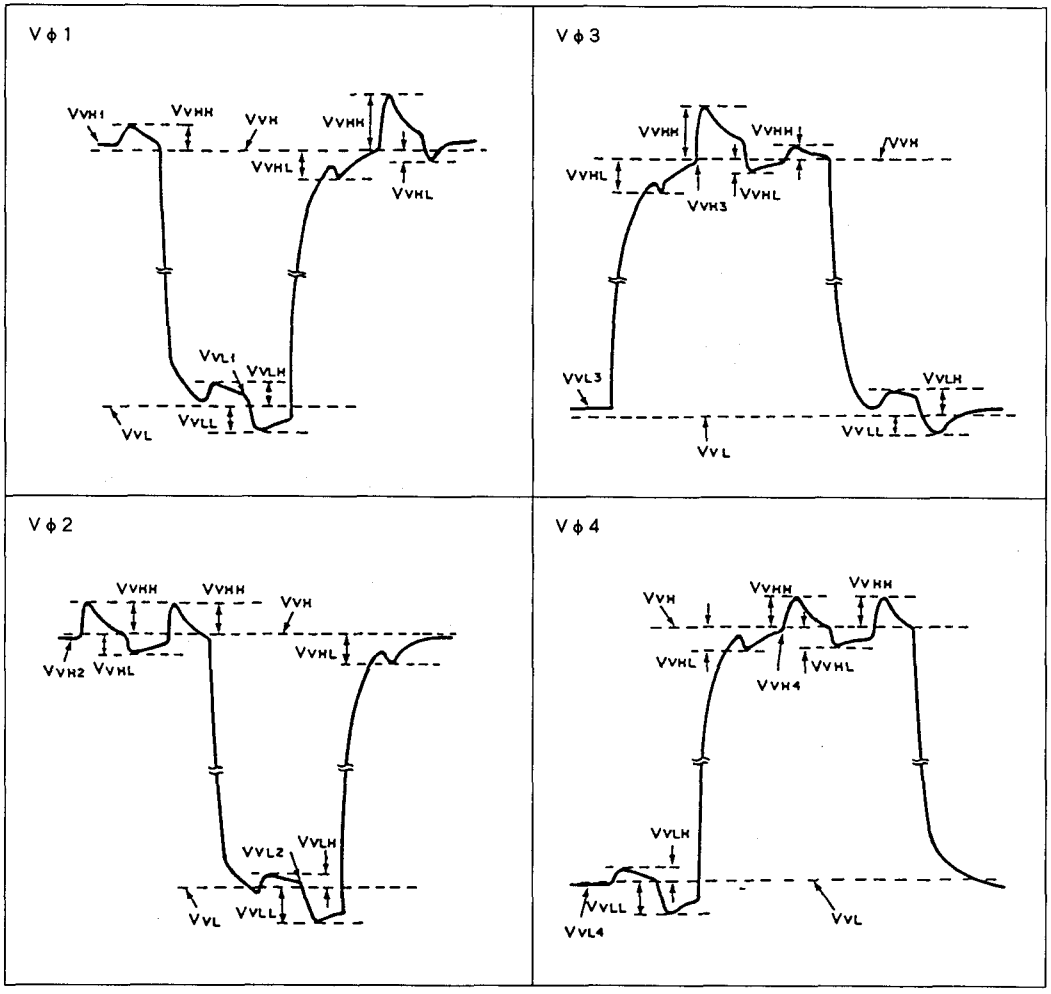
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

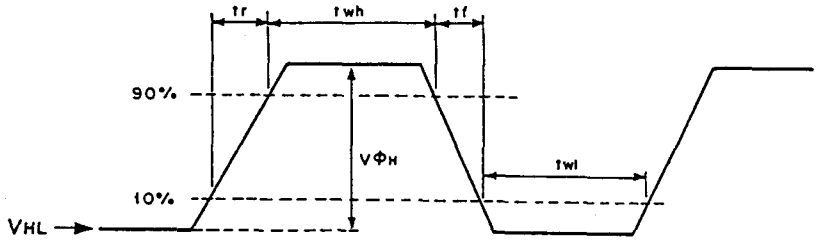
(1) Read out clock waveform



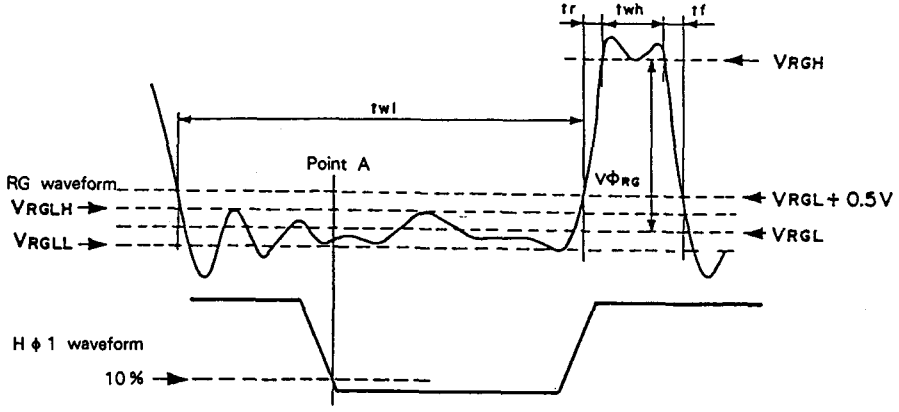
(2) Vertical transfer clock waveform



(3) Horizontal transfer clock waveform diagram



(4) Reset gate clock waveform diagram



VRGLH is the maximum value and VRGLL the minimum value of the coupling waveform in the period from Point A in the diagram above to RG rise.

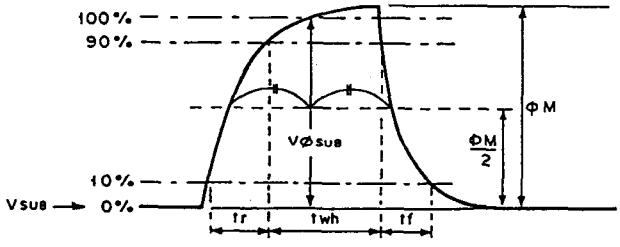
VRGL is the mean value for VRGLH and VRGLL.

$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

VRGH is the minimum value for twh period.

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

(5) Substrate clock waveform



Clock Switching Characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	V_T	2.3	2.5						0.5			0.5		µs	During read out
Vertical transfer clock	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$										0.015		0.25	µs	*1
Horizontal transfer clock	$H\phi$	37	41		38	42			12	15	*2	10	15	ns	During imaging
Horizontal transfer clock	$H\phi_1$		5.6						0.012			0.012		µs	During parallel serial conversion.
Horizontal transfer clock	$H\phi_2$					5.6			0.012			0.012		µs	
Reset gate clock	ϕ_{RG}	11	15		75	79			6.5			4.5		ns	
Substrate clock	ϕ_{SUB}	1.5	2.0							0.5			0.5	µs	During charge drain.

*** 1)** When vertical transfer clock driver CXD1250 is in use.

*** 2)** tf ≧ tr–2 ns

Image Sensor Characteristics

(Ta=25℃)

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	160	200		mV	1	
Saturation signal	Vsat	450			mV	2	Ta=60℃
Smear	Sm		0.007	0.012	%	3	
Video signal shading	SH			20	%	4	Zone 0, I
				25	%	4	Zone 0 to II'
Dark signal	Vdt			2	mV	5	Ta=60℃
Dark signal shading	Δ Vdt			1	mV	6	Ta=60℃
Flicker	F			2	%	7	
Lag	Lag			0.5	%	8	

Zone Chart of Video Signal Shading

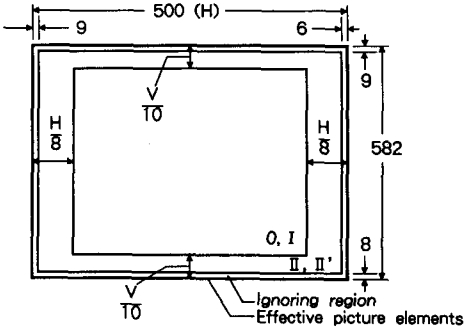


Image Sensor Characteristics Test Method

◎ Test conditions

① Through the following tests the substrate voltage and reset gate clock voltage are set to the value displayed on the device, while the device drive conditions are at the typical value of the bias and clock voltage conditions.

② Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OB) is set as the reference for the signal output which is taken as the signal output or the chroma signal output of the testing system.

◎ Definition of standard imaging conditions

① Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 cd/ m², color temperature 3200K Halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t=1.0mm) as IR cut filter and image at F8.

② Standard imaging condition II: Image a light source (color temperature of 3200K) which uniformity of brightness is within 2% at all angles. Use a testing standard lens with CM500S (t=1.0mm) as IR cut filter. The light intensity is adjusted to the value indicated in each testing item by lens diaphragm.

1. Sensitivity
   Set to standard imaging condition I and measure signal (S) at the center of the screen.

2. Saturation signal
   Set to standard imaging condition II. Adjust light intensity to 10 times that of signal output average value (V_A=150mV), then test signal minimum value.

3. Smear
   Set to standard imaging condition II. Adjust light intensity to 500 times that of signal output average value (V_A=150mV). Stop read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the maximum value VSm of signal output.

$$Sm=\frac{VSm}{V_A}\times\frac{1}{500}\times\frac{1}{10}\times 100\ (\%)\ (1/10V)$$

4. Video signal shading
   Set to standard imaging condition II. Adjust light intensity to signal output average value (V_A=150mV) with lens diaphragm at F5.6 to F8. Then test maximum (Vmax) and minimum (Vmin) values of signal.

   $SH=(Vmax-Vmin)/V_A\times 100\ (\%)$

5. Dark signal
   Test signal output average value Vdt when the device ambient temperature is at 60℃ and light is obstructed with horizontal idle transfer level as reference.

6. Dark signal shading
   Following 5, test maximum (Vdmax) and minimum (Vdmin) values of dark signal output.

   $\Delta Vdt=Vdmax-Vdmin$

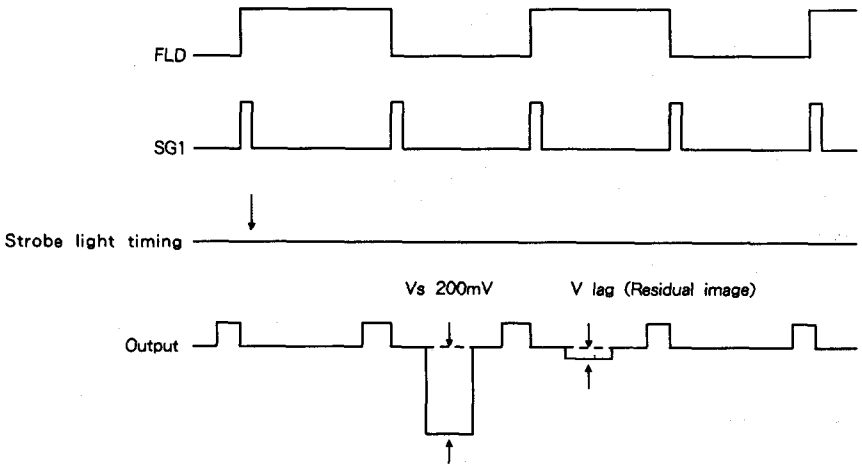
7. Flicker
   Set to standard imaging condition II. Adjust light intensity to signal output average value (V_A=150mV). Then test the signal difference (Δ Vf) between even field and odd field.

   $F=(\Delta Vf/V_A)\times 100\ (\%)$

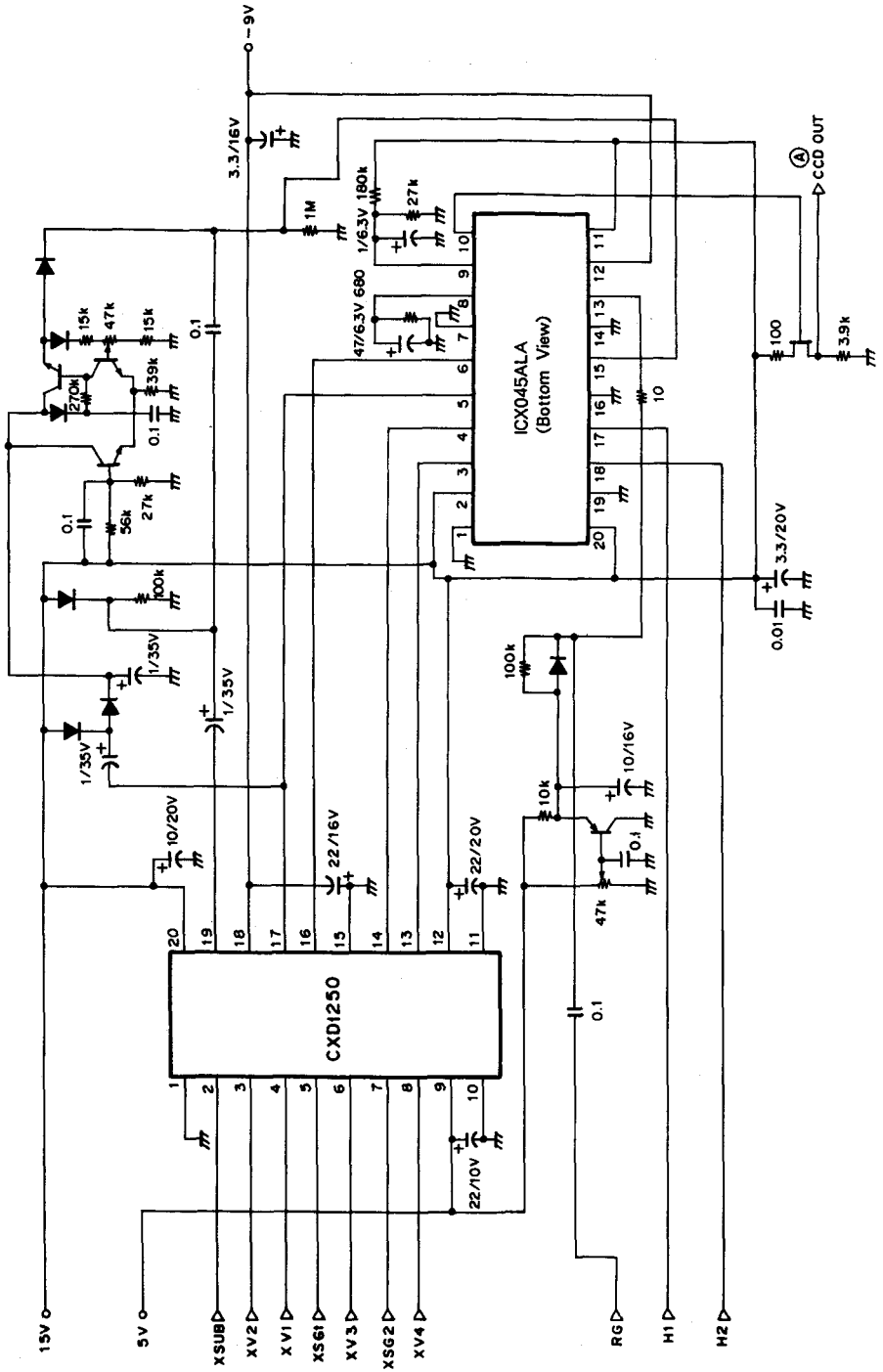
8. Residual image

Adjust signal output value (Vs) by strobe light to 200mV. Then light a stroboscopic tube with the following timing and test the residual image (Vlag).

Lag = (Vlag/Vs) × 100 (%)



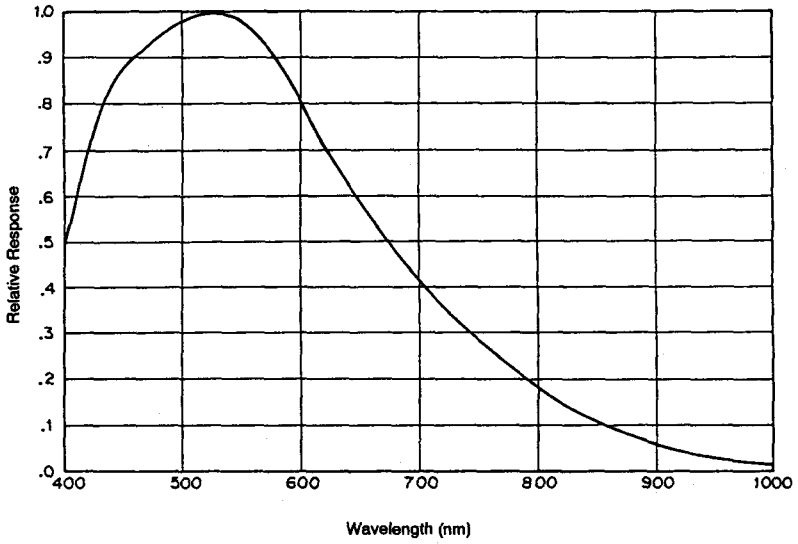
Drive Circuit



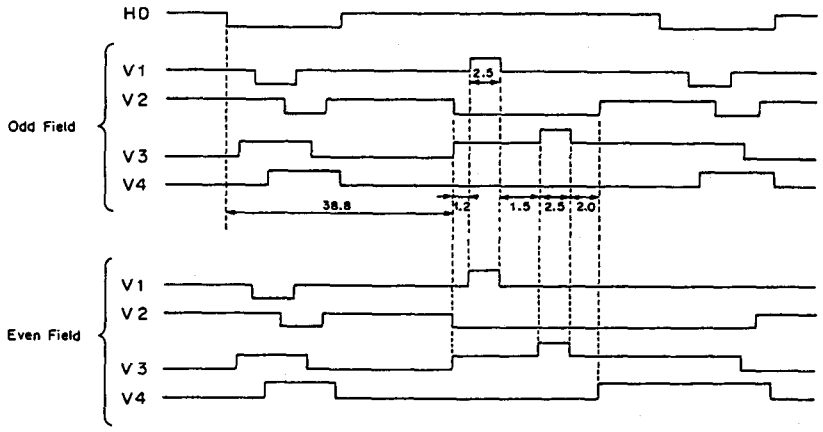
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Spectral Sensitivity Characteristics

(Excluding light source characteristics, including lens characteristics)

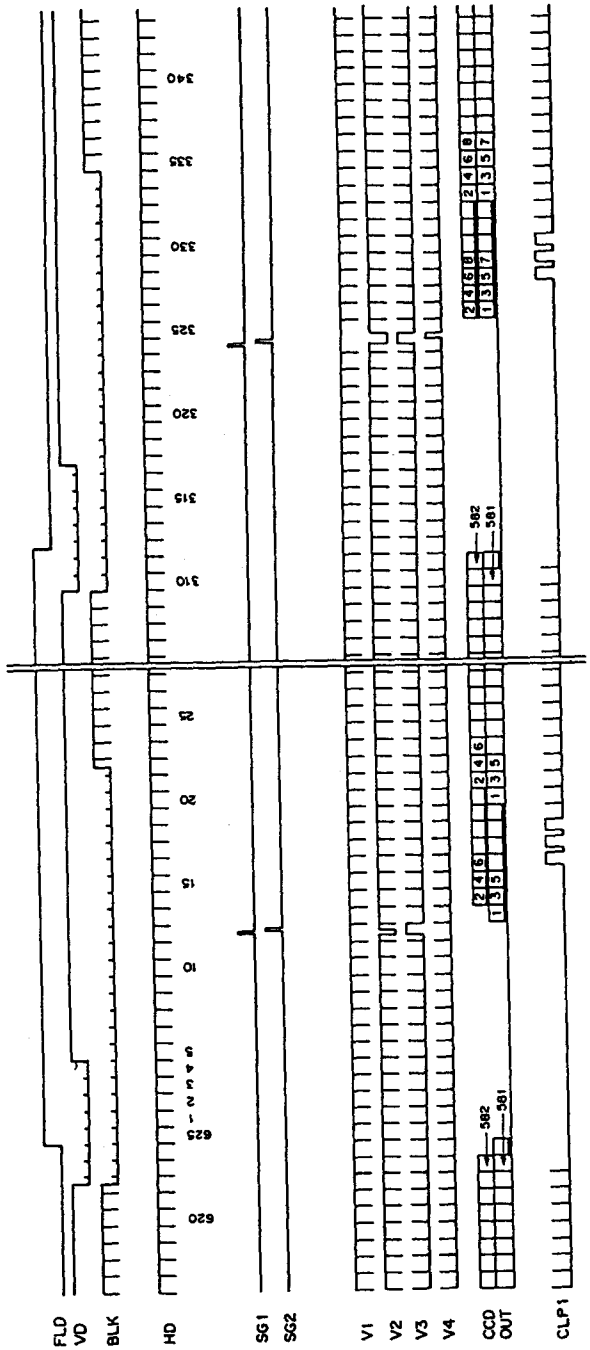


Sensor Read Out Clock Timing Chart

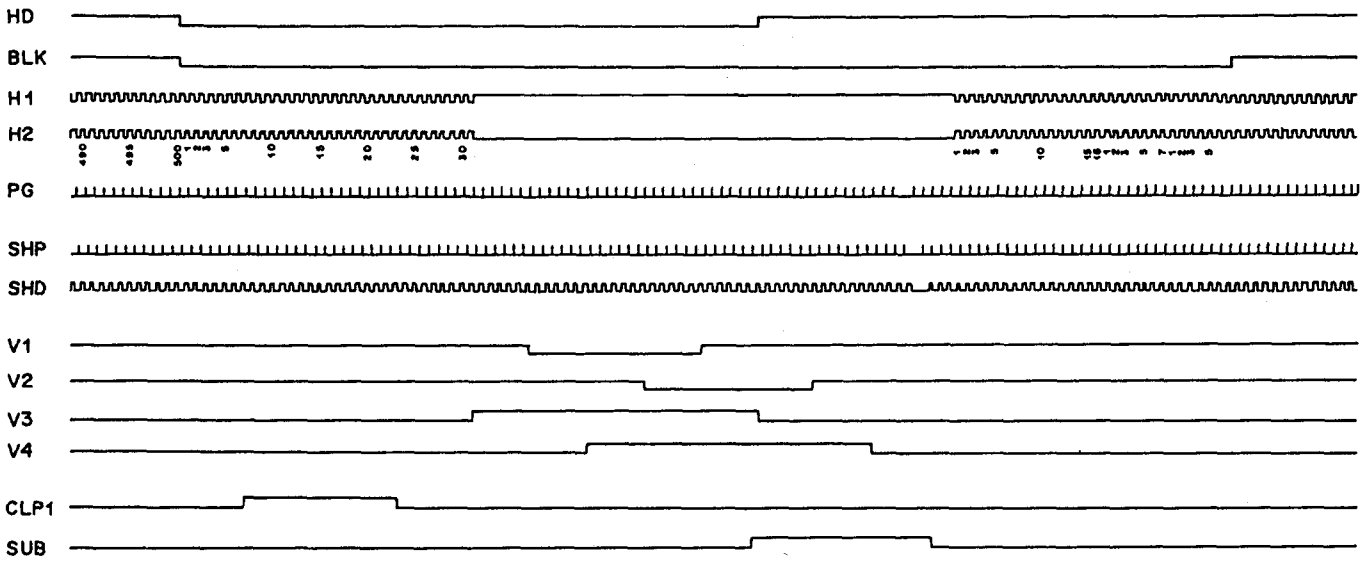


Unit : µs

Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



(During electronic shutter operation)

Handling Instructions

1) Static charge prevention
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80 °C .
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
c) To dismount an imaging device do not use a solder suction equipment. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

CCD Image Sensor System

3) CCD Image Sensor System

Type	Functions				Page
	Classification		Image sensor	Features	
IS026BK IS027BK	Color	NTSC	ICX026BK	• Variable electronic shutter equipped • Extemal synchronization possible • High senstivity • High density mounting adopting small packages	285
		PAL	ICX027BK		

SONY ISO26BK/ISO27BK

CCD Color Imager System

Description

This new color imager system made up of a CCD imager and peripheral hybrid IC's realizes very compact CCD color cameras.
Improvement in sensitivity characteristic has been realized through the adoption of ICX 026 BK/027 BK. The system is available whereas independent hybrid IC's are not.

- CCD imagers
  ICX026BK (NTSC)
  ICX027BK(PAL)

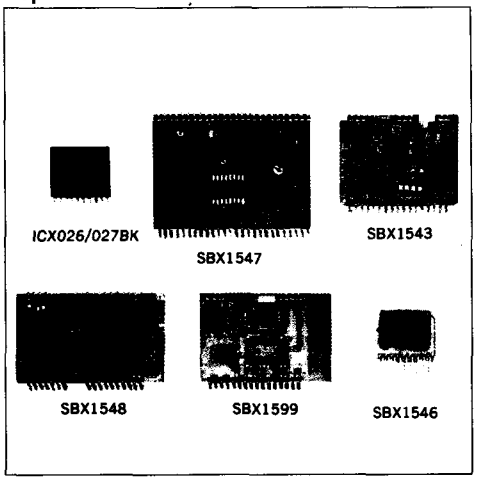
- Hybrid IC's

NTSC	SBX1547-01	Drive and AGC circuit
	SBX1543-01	Matrix circuit
	SBX1548-01	Encoder
	SBX1599-01	VBS gen-lock
	SBX1546-01	AWB circuit
PAL	SBX1547-21	Drive and AGC circuit
	SBX1543-01	Matrix circuit
	SBX1548-21	Encoder
	SBX1599-21	VBS gen-lock
	SBX1546-01	AWB circuit

Features

- CCD imager
  High sensitivity (Low dark current)
  High resolution
  Variable speed electronic shutter function
  N-sub, P-well structure
- Hybrid IC's
  No adjustment required: Function trimming used
  Highly compact mounting: Small size IC package used
  UL approved
- System kit
  Peripherals greatly reduced
  Gen lock for color framing adaptable
  Color difference signals, Y/C separated signals output
  AGC ON/OFF possible

Top View



Imager system		System structure
NTSC	ISO26BK-30F	ICX026BK-3 +SBX1547-01
	ISO26BK-30G	ICX026BK-3 +SBX1547-01 +SBX1543-01 +SBX1548-01
	ISO26BK-30J	ICX026BK-3 +SBX1547-01 +SBX1543-01 +SBX1548-01 +SBX1599-01
	ISO26BK-30H	ICX026BK-3 +SBX1547-01 +SBX1543-01 +SBX1548-01 +SBX1546-01
	ISO26BK-30K	ICX026BK-3 +SBX1547-01 +SBX1543-01 +SBX1548-01 +SBX1599-01 +SBX1546-01
PAL	ISO27BK-30F	ICX027BK-3 +SBX1547-21
	ISO27BK-30G	ICX027BK-3 +SBX1547-21 +SBX1543-01 +SBX1548-21
	ISO27BK-30J	ICX027BK-3 +SBX1547-21 +SBX1543-01 +SBX1548-21 +SBX1599-21
	ISO27BK-30H	ICX027BK-3 +SBX1547-21 +SBX1543-01 +SBX1548-21 +SBX1546-01
	ISO27BK-30K	ICX027BK-3 +SBX1547-21 +SBX1543-01 +SBX1548-21 +SBX1599-21 +SBX1546-01

E89420-HP

Systems

Absolute maximum ratings (Ta=25°C)

Item	Hybrid ICs					CCD Imager	
	SBX1547	SBX1543	SBX1548	SBX1599	SBX1546		
Supply voltage	V_{CC1} 6.3V	V_{CC1} 6V	V_{CC1} 6.3V	V_{CC1} 6.3V	V_{CC1} 7V	V_{DD1}	
	V_{CC2} 20V			V_{CC2} 12V		V_{DD2}	20V
	V_{CC3} 25V					V_{PD}	
	V_{CC4} −16V					V_{SS}	
						V_{SUB}	55V
Operating temperature	−10 to +60°C						
Storage temperature	−30 to +80°C						

Hybrid ICs recommended operating conditions

SBX1547		SBX1543		SBX1548		SBX1599		SBX1546	
Supply voltage (V)	Current consumption (mA)	Supply voltage (V)	Current consumption (mA)	Supply voltage (V)	Current consumption (mA)	Supply voltage (V)	Current consumption (mA)	Supply voltage (V)	Current consumption (mA)
V_{CC1} 5±0.25V	105(Typ.)	V_{CC1} 5±0.25V	100(Typ.)	V_{CC1} 5±0.25V	95(Typ.)	V_{CC1} 5±0.25V	20(Typ.)	V_{CC1} 5±0.25V	2.5(Typ.)
V_{CC2} 15±0.45V	12(Typ.)					V_{CC2} 8.5±0.5V	15(Typ.)		
V_{CC3} 22±1.5V	0.5(Typ.)								
V_{CC4} −9.5±0.5V	2(Typ.)								

System Operating Characteristics

Evaluation board

	NTSC Specifications	PAL Specifications
Scanning system	525Lines 30frame/sec.	625Lines 25frame/sec.
	2 : 1 Interlace	
Video signal	1.0Vp-p, 75Ω, Negative sync signal	
Horizontal resolution	330TV Lines	
S/N ratio	More than 43dB (AGC off, γon)	
Power consumption	1.8W (Without AWB, Gen-lock)	
Sync system	Internal/External selection possible. (composite video signal input to hybrid IC for external sync use)	

Electrical characteristics 1 (Ta=25°C)

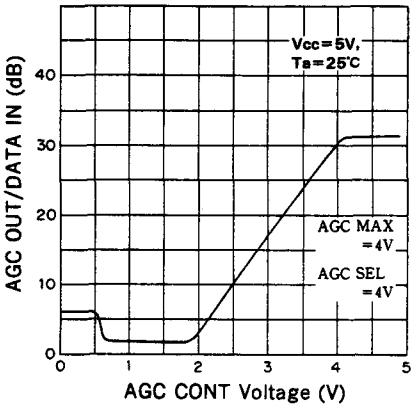
Item			Symbol	Test condition	Min.	Typ.	Max.	Unit
A to E system	Vertical transfer clock φV1, φV3	H level	V_T		13	15	17	V
		M level	V_{VM}		−0.5	0	0.7	
		Amplitude	$V_{\phi V}$		8		11	
	Vertical transfer clock φV2, φV4	H level	V_{VM}		−0.5	0	0.7	V
		Amplitude	$V_{\phi V}$		8		11	
	Horizontal transfer clock φH1, φH2	L level	V_{HL}				0.5	V
		Amplitude	$V_{\phi H}$		4.5	5	5.5	
	Precharge clock φPG	L level	V_{PGL}				0.5	V
		Amplitude	$V_{\phi PG}$		9		12	
	Substrate clock φSUB	Amplitude	$V_{\phi SUB}$		30		35	V
	Color separation output	S_1, S_2, Y output	Vf	Input data 150mVp-p		500		mVp-p
		DC output	V_{fDC}	DC bias	1.8	1.9	2.0	V
	IRIS output	IRIS output	V_{IR}			285		mVp-p
		DC output	V_{IRDC}	DC bias	1.8	1.9	2.0	V

Electrical characteristics 2 (Ta=25°C)

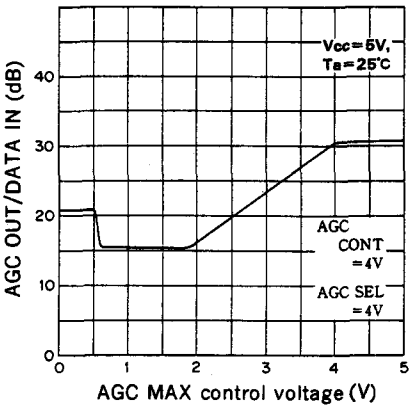
Item				Symbol	Test condition	Min.	Typ.	Max.	Unit
B to E System	R, G, B, output	NTSC	R	V_{RNT}	Standard Imaging Condition, Application system circuit	340	400	460	mV
			G	V_{GNT}	Standard Imaging Condition, Application system circuit	450	520	590	
			B	V_{BNT}	Standard Imaging Condition, Application system circuit	210	260	310	
		PAL	R	V_{RPA}	Standard Imaging Condition, Application system circuit	310	370	430	mV
			G	V_{GPA}	Standard Imaging Condition, Application system circuit	480	550	620	
			B	V_{BPA}	Standard Imaging Condition, Application system circuit	240	290	340	
		DC		V_{CLDC}	DC bias	1.7	1.9	2.0	V
	WB Control	Cont32		V_{C32}	Typ. (3200°k) DC bias		1.0		V
	Set up level			V_{set}			20	50	mV
	Sync level	NTSC		V_{SYNT}		250	285	320	mV
		PAL		V_{SYPA}		270	300	330	
	Burst level	NTSC		V_{BUNT}		250	285	320	mV
		PAL		V_{BUPA}		270	300	330	

* Definition of Standard Imaging condition
A pattern box (luminance 706 Nit, Color temperature 3200°K, with halogen lamp) is imaged using a test standard lens, F5.6 contraction, at that time there is no pattern and CM-500S 1.0mmt is utilized as I.R cut filter.

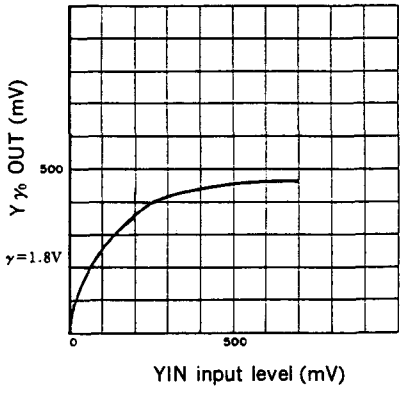
AGC Amp gain control characteristics
(SBX1547)



AGC Amp Max. gain control characteristics
(SBX1547)

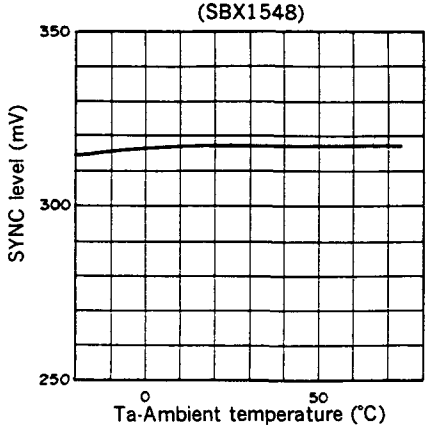


Yγ characteristics
(SBX1543)



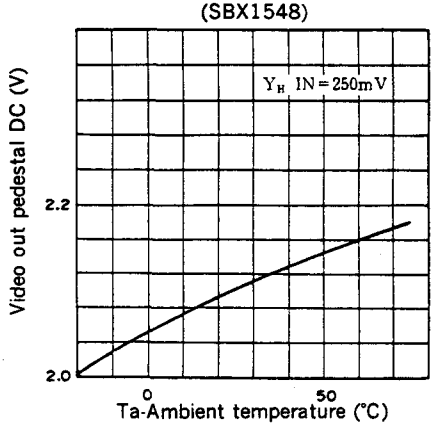
SYNC level temperature characteristics

(SBX1548)



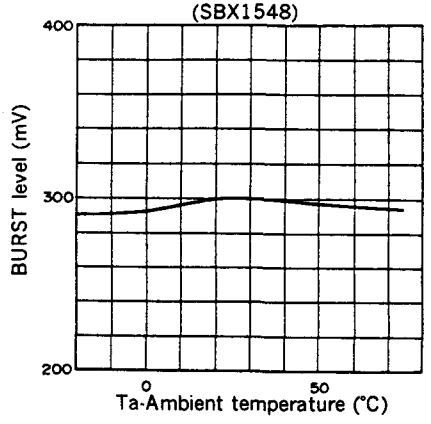
VIDEO OUT pin pedestal DC

(SBX1548)



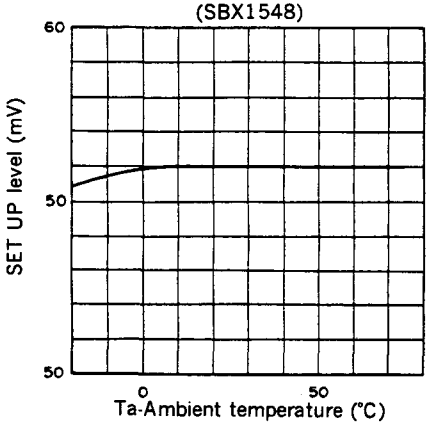
Burst level temperature characteristics

(SBX1548)



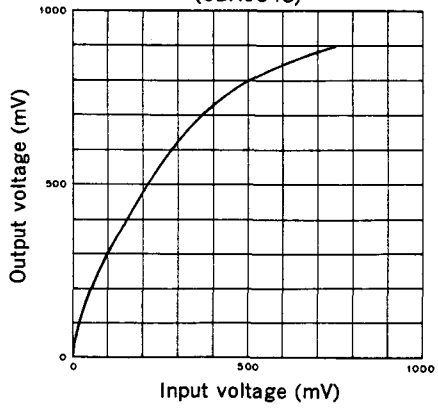
SET UP level temperature characteristics

(SBX1548)



C-γ control characteristics

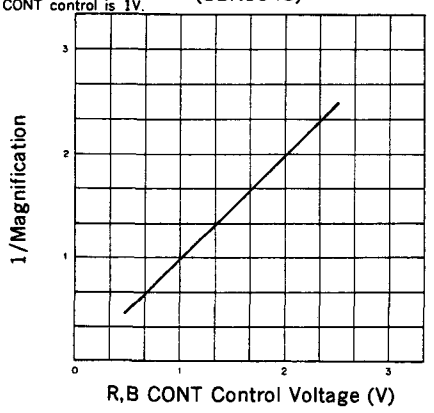
(SBX1548)



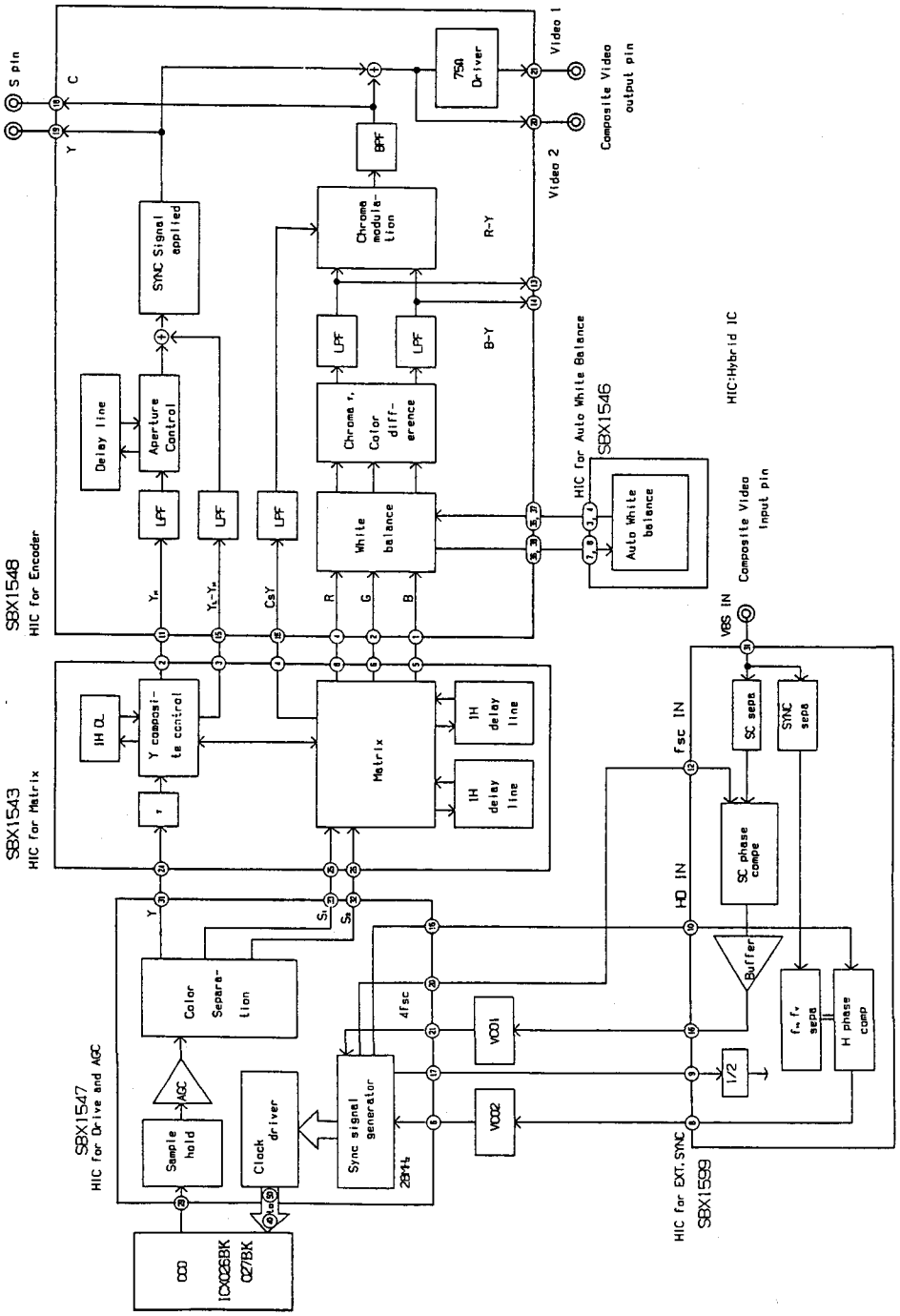
WB R, B CONT control characteristics

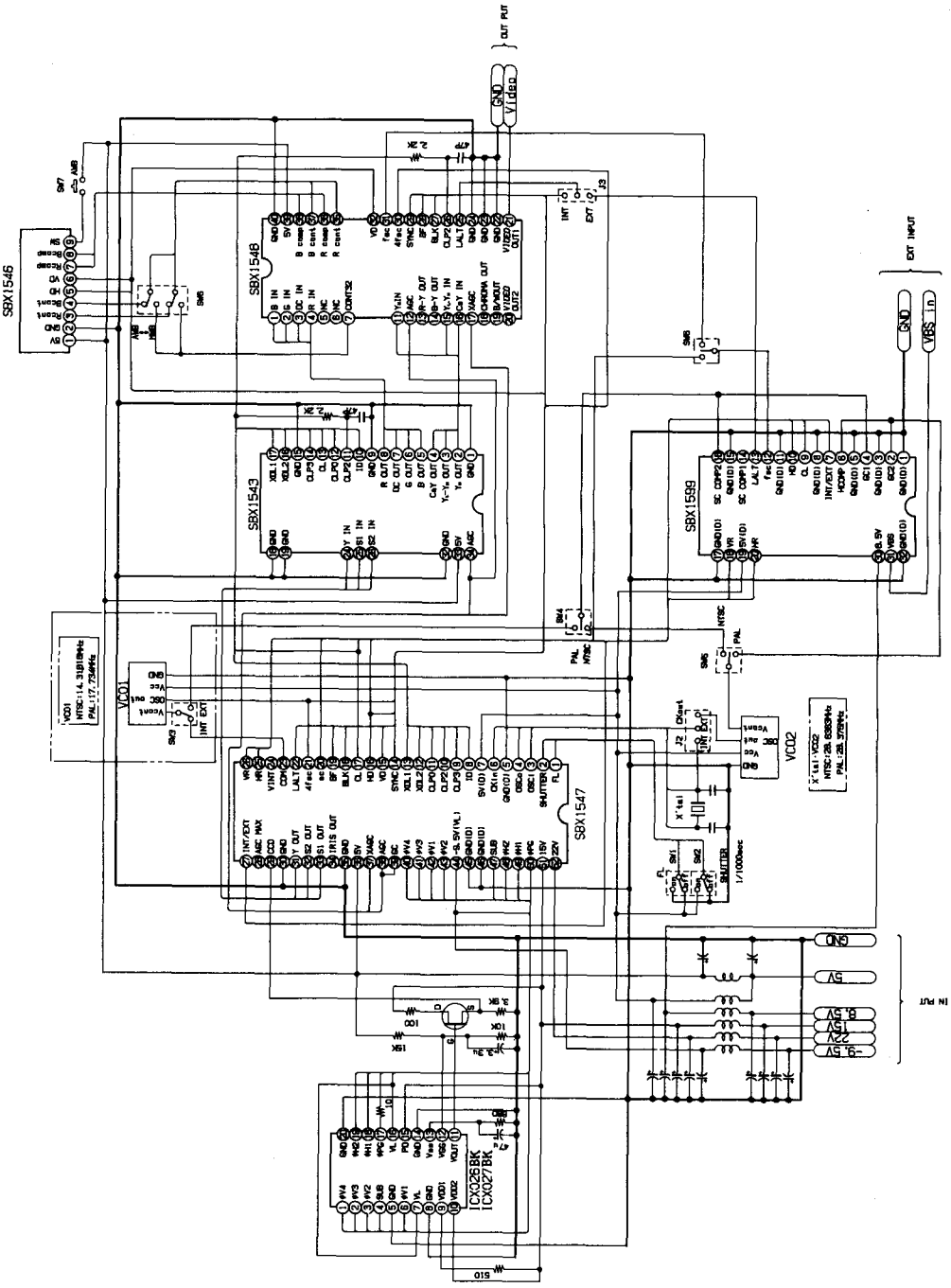
Output is taken at 1 when R,B CONT control is 1V.

(SBX1548)



System Block Diagram

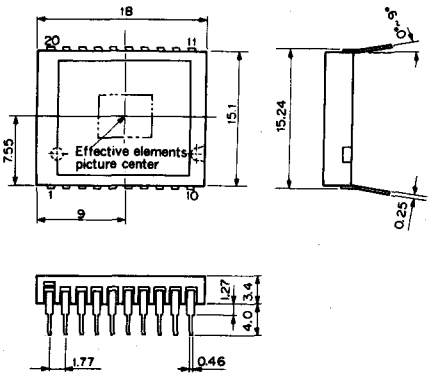



SBX1546
SBX1548
SBX1543
SBX1599
SBX1547
VCO1
VCO2
ICX026BK
ICX027BK
OUT PUT
EXT INPUT
IN PUT
GND
Y/Video
VBS In
5V
INT
EXT
NTSC
PAL
SHUTTER
1/1000sec

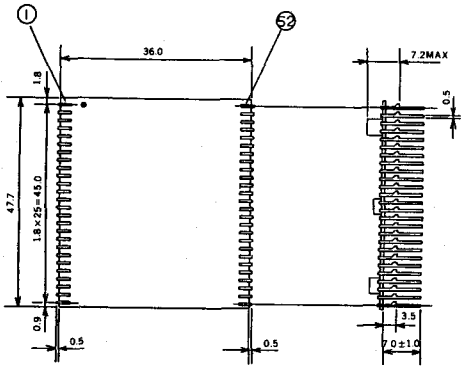
Package Outline **Unit: mm**

20pin DIP (Ceramic)

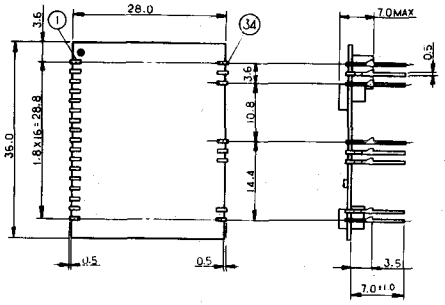
ICX026BK-3
ICX027BK-3



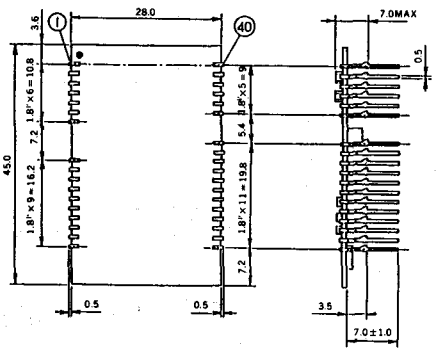
SBX1547-01/02



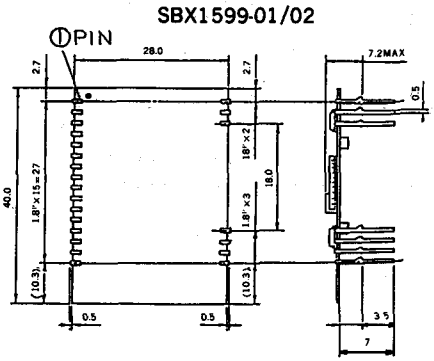
SBX1543-01



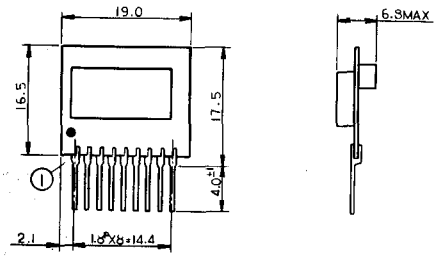
SBX1548-01/21



SBX1599-01/02



SBX1546-01



CCD image sensor Handling Instructions

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- Ionized air is recommended for discharge when handling CCD image sensor.
- For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
- Make sure the package temperature does not exceed 80°C.
- Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30 W soldering iron and solder each pin in less than 2 seconds. For repairs and remount cool sufficiently.
- To dismount an imaging device do not use a solder pulf. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
- Operate in clean environments (around class 1000 will be appropriate).
- Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended).
- Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
- Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
- When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods to ultra violet rays, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

7) Defect compensation ROM
- This is shipped mounted on SBX1547 in pair with the CCD image sensor. To load on the set, match with a CCD image sensor bearing an indentical serial number label.
When there is no defect there is no ROM or serial number.

Scanning System IC for Video Camera

4) Scanning System IC for Video Camera

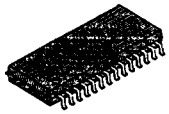
Type	Applications	Functions	Page
CXD1030M	Sync signal generator	14MHz (18MHz) demultiplier, for NTSC, PAL	297
CXD1158M		14MHz (18MHz) demultiplier, for NTSC, PAL, Sub carrier output×3	307
CXD1159Q		14MHz (18MHz) demultiplier, for NTSC, PAL, Sub Window pulse output	317
CXD1217M		For NTSC, PAL, PALM, SECAM, Color framing in NTSC, PAL, PALM	327
CXD1217Q			339
CXD1035BQ-Z	Timing pulse generator for scanning system	CCD drive timing pulse generation, Signal processing pules generation, for ICX022BL, ICX024BL	351
CXD1149Q/R		CCD drive timing pulse generation, Signal processing pules generation, for ICX022BN/ICX024BN, Variable speed electronic shutter timing generation (1/60 to 1/10000s.)	363
CXD1156Q/R		CCD drive timing pulse generation, Variable speed electronic shutter timing generation (1/60 to 1/10000s.) for ICX026BKA/BLA, ICX027BKA/BLA	377
CXD1252AR/AQ		CCD drive timing pulse generation, Signal processing pulse generation, Variable speed electronic shutter timing generation (built-in slow shutter) for ICX038BNA/ICX039BNA	390
CXD1253AR/AQ		CCD drive timing pulse generation, Signal processing pulse generation, Variable speed electronic shutter timing generation (built-in slow shutter) for ICX026CKA/ICX027CKA, ICX044BKA/ICX045BKA	409
CXD1255Q		CCD drive timing pulse generation, Signal processing pulse generation, Variable speed electronic shutter timing generation (1/60 to 1/10000s.) for ICX038ALA/ICX039ALA	428
CXD1141M	Variable speed electronic shutter timing generator	Variable speed electronic shutter timing generation (1/60 to 1/10000s.) for ICX022BL/ICX024BL	442
CXD1251Q	Blemish compensation timing generator	Blemish compensation timing generation	446
CXB0026AM	Vertical/horizontal clock driver	CCD image sensor driver×2, Compatible with high frequency operation	451
CXA1065M	Vertical clock driver	CCD image sensor driver×4, Lead-out pulse generation inverter, Negative voltage generation inverter	454
CXD1250M		CCD image sensor driver×4, Lead-out pulse generation inverter, Shutter pulse driver	469

SONY

CXD1030M

Sync. Signal Generator for Camera

28 pin SOP (Plastic)



Description

The CXD1030M is a sync. signal generator for video cameras.

Features

- Adapts to NTSC or PAL by switching mode
- Low power consumption
  (Standard NTSC: 25 mW; PAL: 30 mW)
- Built-in phase comparator and inverter for active filter (separate power supply for the filter inverter)
- External sync.

Function

Sync. signal generator

Structure

Silicon gate CMOS IC

Application

Video • Camera

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	V_{SS}* − 0.3 to 7.0	V
• Input voltage	V_I	V_{SS}* − 0.3 to V_{DD} + 0.3	V
• Output voltage	V_O	V_{SS}* − 0.3 to V_{DD} + 0.3	V
• Operating temperature	T_{opr}	− 20 to + 75	°C
• Storage temperature	T_{stg}	− 55 to + 150	°C

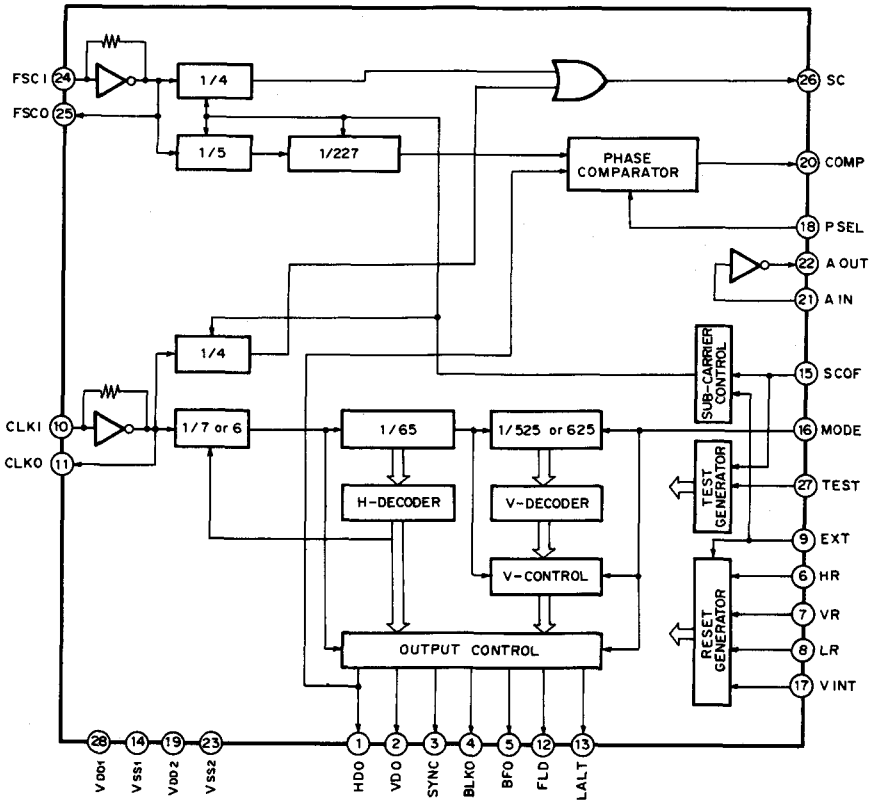
* V_{SS} = 0V

Recommended Operating Conditions

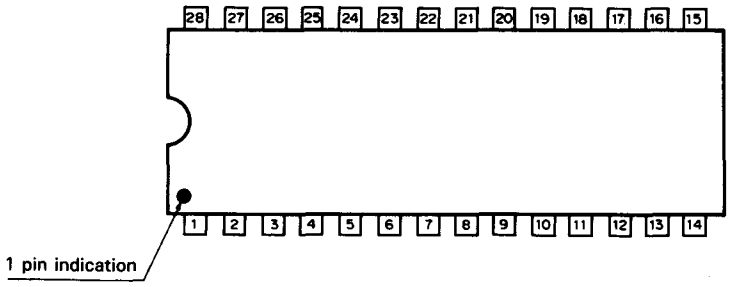
• Supply voltage	V_{DD}	4.50 to 5.50	V
• Operating temperature	T_{opr}	− 20 to + 75	°C

E89Z05 – ST

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	HDO	O	Horizontal drive pulse
2	VDO	O	Vertical drive pulse
3	SYNC	O	Complex synchronized pulse
4	BLKO	O	Complex branking pulse
5	BFO	O	Burst flug pulse
6	HR	I	H reset input
7	VR	I	V reset input
8	LR	I	LALT reset input
9	EXT	I	Interinal/external mode switching $\overline{\text{INT}}$/EXT
10	CLKI	I	Clock input (NTSC: 14.31818 MHz, PAL: 14.1875 MHz)
11	CLKO	O	Clock output
12	FLD	O	Field pulse
13	LALT	O	Line alternate pulse
14	V_{SS1}	–	GND
15	SCOF	I	Sub carrier suppress input L: OFF
16	MODE	I	NTSC/PAL mode switching $\overline{\text{NTSC}}$/PAL
17	VINT	I	Initialize input
18	PSEL	I	Phase comparator polarity switching
19	V_{DD2}	–	Inverter +5V for filter
20	COMP	O	Phase comparator output
21	AIN	I	Inverter input for filter
22	AOUT	O	Inverter output for filter
23	V_{SS2}	–	Inverter GND for filter
24	FSCI	I	$4f_{SC}$ clock input
25	FSCO	O	$4f_{SC}$ clock output
26	SC	O	Sub carrier output
27	TEST	I	Test input (L normal)
28	V_{DD1}	–	+5V

Electrical Characteristics

DC characteristics

$V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_{opr} = -20$ to $+75°C$

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current		I_{DD}	Test circuit (2)		2.0		mA
		I_{DDS}	Static state*1	0		0.1	μA
Output voltage I*2	H level	V_{OH}	$I_{OH} = -1.0$ mA	$V_{DD}-0.5$		V_{DD}	V
	L level	V_{OL}	$I_{OL} = 1.0$ mA	V_{SS}		0.4	V
Output voltage II*3	H level	V_{OH}	$I_{OH} = -0.5$ mA	$V_{DD}-0.5$		V_{DD}	V
	L level	V_{OL}	$I_{OL} = 0.5$ mA	V_{SS}		0.4	V
Input voltage	H level	V_{IH}		$0.7V_{DD}$			V
	L level	V_{IL}				$0.3V_{DD}$	V
Input leak current		I_{LI}	V_I = 0V to V_{DD}	−25		25	μA
Input leak current*4		I_{LZ}		−40		40	μA

Note) *1 $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$
*2 Output pins except "AOUT"
*3 "AOUT" pin
*4 Three state pin

I/O Capacitance

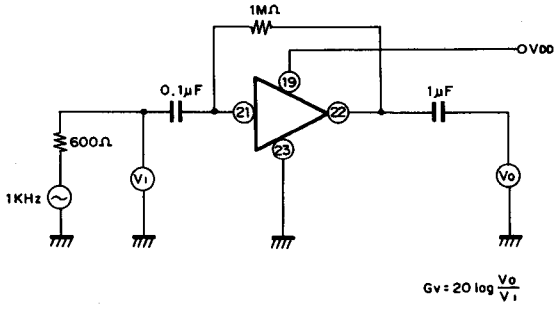
Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			12	pF
Output pin	C_{OUT}			12	pF

Test condition: $V_{DD} = V_I = 0V$, $f_M = 1$ MHz

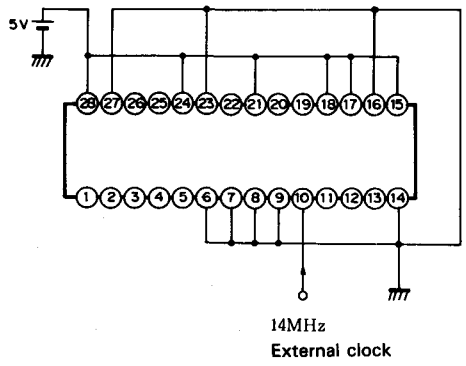
Filter amplifier characteristics

Voltage gain Gv 23dB (Typ.)

Test circuit (1)



Test circuit (2)



Description of Function

1. Generation of various sync. signals (See the Timing Chart.)
   Various sync. signals are generated from clocks.

- Clock frequencies
  NTSC: 910 fH (14.31818 MHz)
  PAL : 908 fH (14.1875 MHz)
  4 fSC (17.734475 MHz)

2. PAL 4 fSC PLL
   Using 908 fH as the master clock, the 4 fSC is put in phase. Corresponding to an external filter (passive or active), the phase comparator polarity can be switched.

Filter	PSEL	Master (908fH)	4fSC	COMP
Passive	L	Fast	Slow	H
		Slow	Fast	L
Active	H	Fast	Slow	L
		Slow	Fast	H

3. SC (SubCarrier) generation

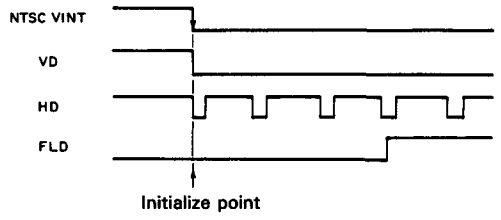
Mode	INT or EXT	SC
NTSC	INT	910fH/4
NTSC	EXT	4fSC/4
PAL	×	4fSC/4

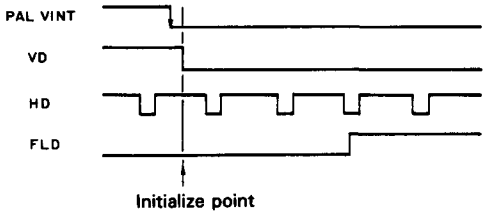
INT : INTERNAL mode (EXT = L)
EXT: EXTERNAL mode (EXT = H)

Unused counters are stopped in any of the mode.
When SC is not required, any counters on SC are stopped and SC is not output by SCOF being set to L.

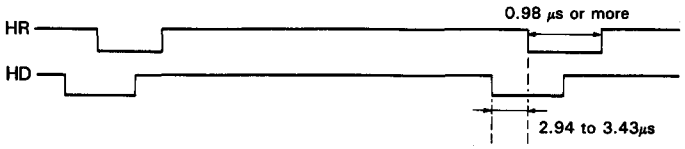
4. Initialization and Reset
   In the INT mode, the circuit is initialized with the fall of VINT. At this time, the H reset, V reset, and LALT reset are not accepted. In the EXT mode, VINT is not accepted but the H reset, V reset, and LALT reset are accepted.

- Initialization (VINT)
  When EXT is L, the fall of VINT is detected and operation is started by the circuit being initialized at the VD fall position immediately prior to field I. (The initialization is completed within 100 ns after the fall is detected.)

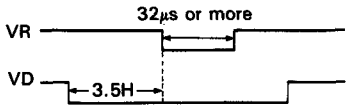




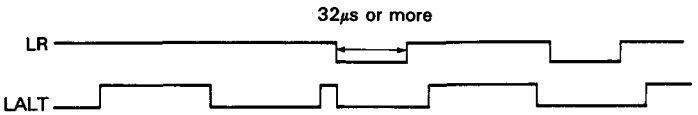
- H reset (HR)
  A reset is executed with the first fall but no reset will be done as long as the subsequent edges do not deviate by more than two clocks (0.98 μs).
  The minimum reset pulse width is 0.98 μs.
  HD is reset 2.94 to 3.43 μs in advance of HR input.



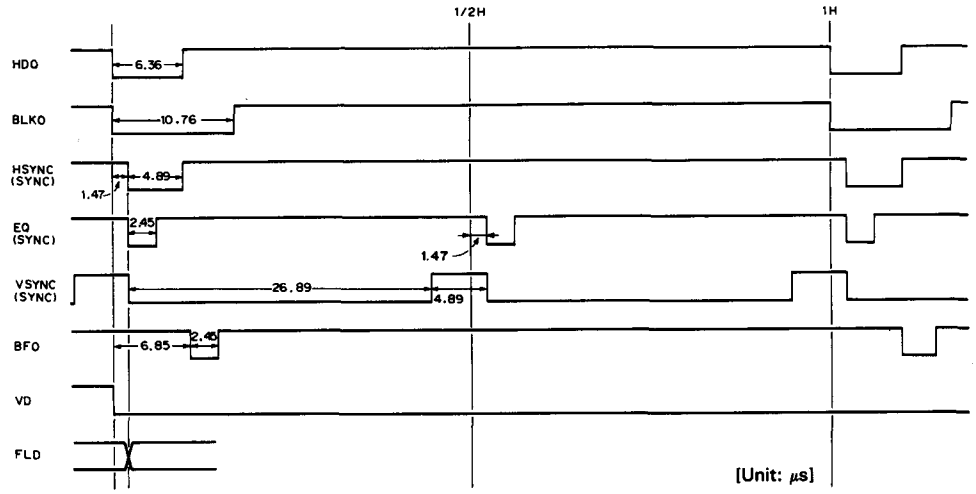
- V reset (VR)
  VD is reset 3.5H in advance of VR input.
  The minimum reset pulse width is 32 μs.



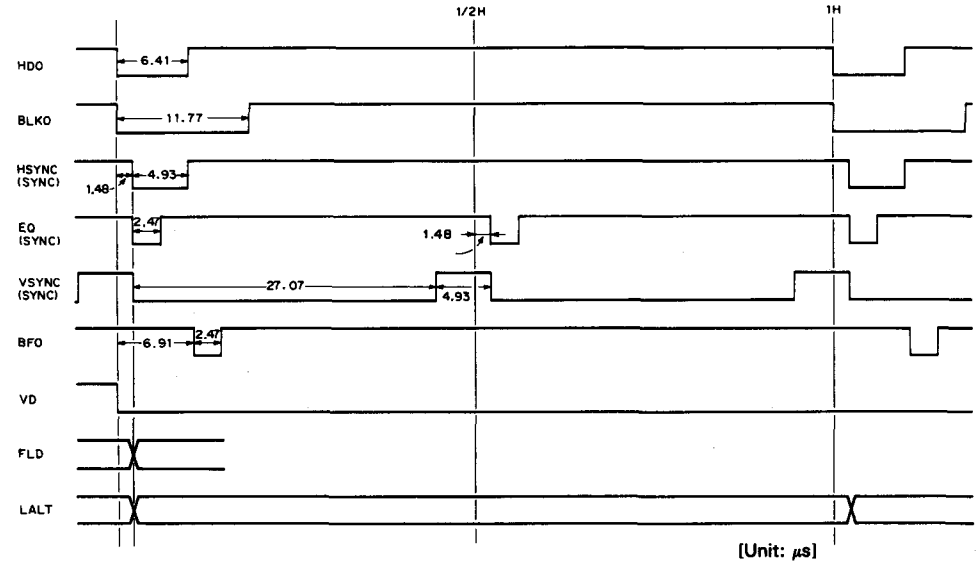
- LALT reset (LR)
  LALT is reset in the same phase as the LR input.
  The minimum reset pulse width is 32 μs.



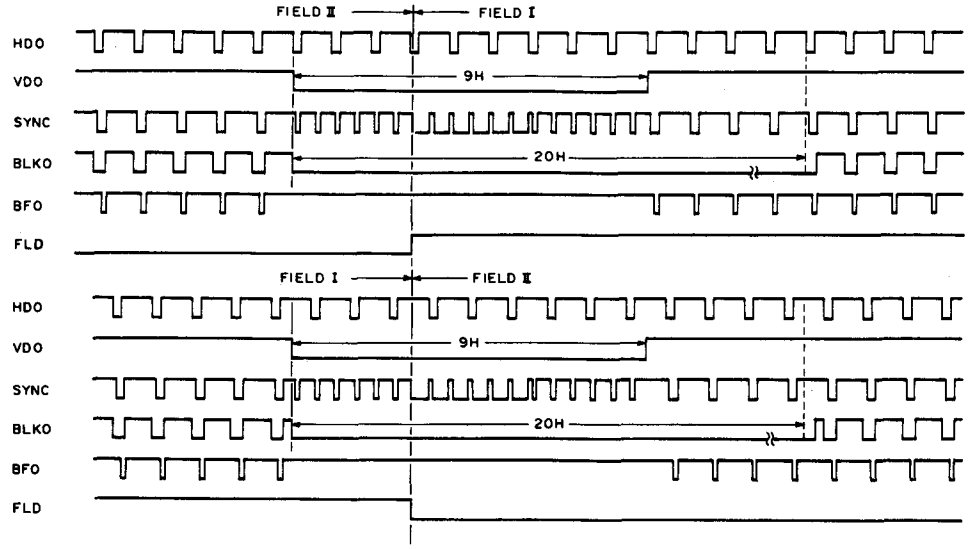
Timing Chart H (NTSC)



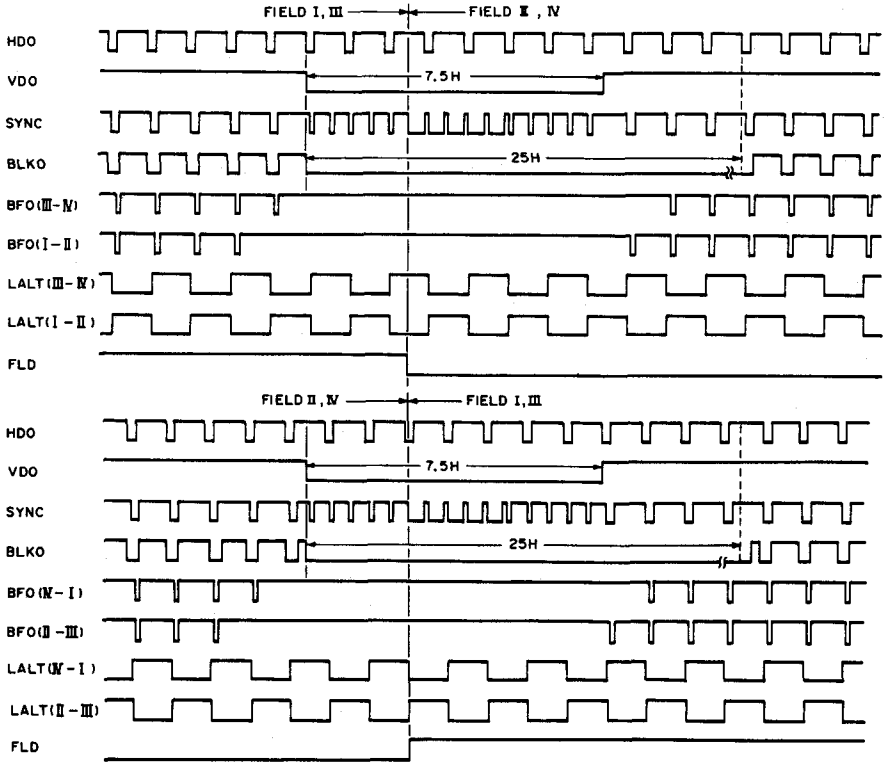
Timing Chart H (PAL)



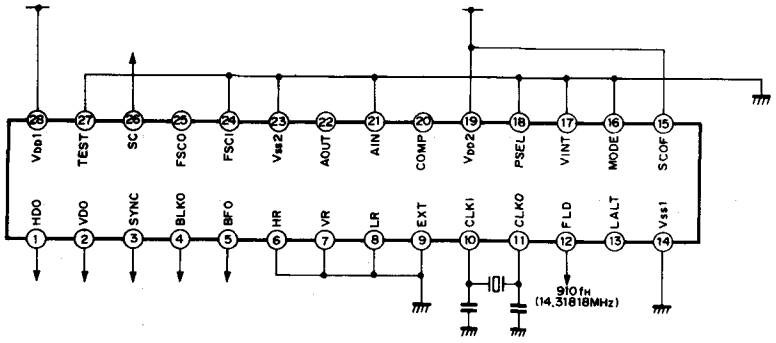
Timing Chart V (NTSC)



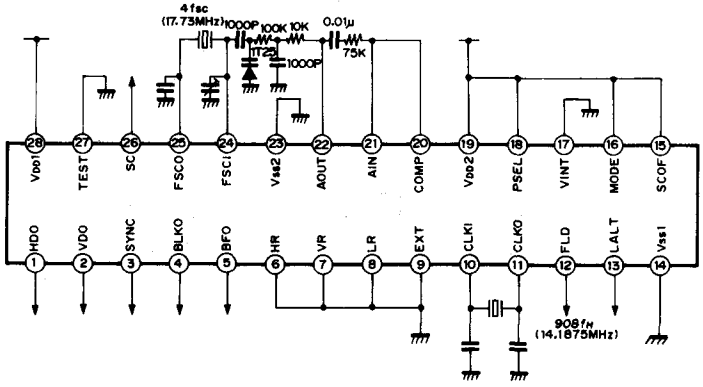
Timing Chart V (PAL)



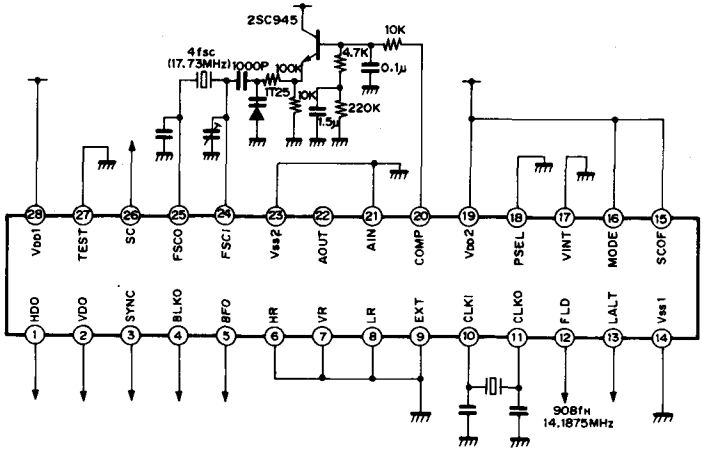
Application Circuits
NTSC (Internal mode)



PAL (Filter configuration 1, Internal mode)

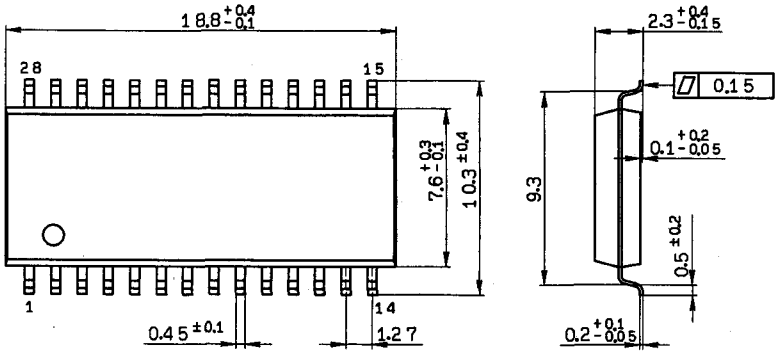


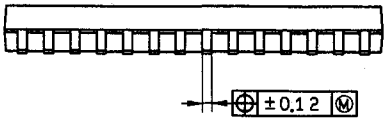
PAL (Filter configuration 2, Internal mode)



Package Outline Unit : mm

28 pin SOP (Plastic)





SONY NAME	SOP-28P-L04
EIAJ NAME	*SOP028-P-0375-D
JEDEC CODE	———

SONY

CXD1158M

Synchronizing Signal Generator for Consumer Video Camera

Description

CXD1158M is a synchronizing signal generator for video camera.

Features

- Adapts to NTSC or PAL by switching mode
- Low power consumption
- Built-in phase comparator and inverter for active filter (separate power supply for the filter inverter)
- External sync

Structure

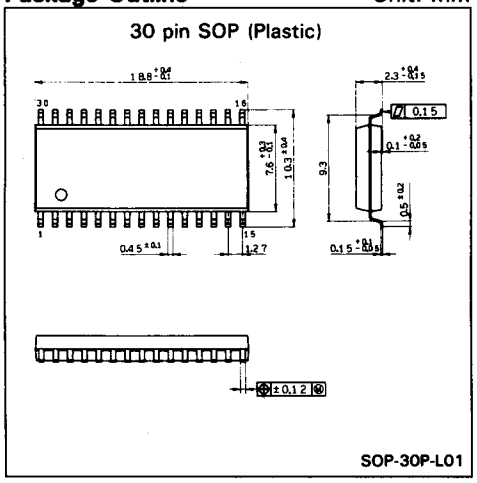
Silicon gate CMOS IC

Application

Consumer video camera

Package Outline

Unit: mm



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	V_{SS}*1	−0.3 to +7.0	V
• Input voltage	V_I	V_{SS}*1	−0.3 to V_{DD} + 0.3*2	V
• Output voltage	V_O	V_{SS}*1	−0.3 to V_{DD} + 0.3*2	V
• Operating temperature	Topr		−20 to +75	°C
• Storage temperature	Tstg		−55 to +150	°C

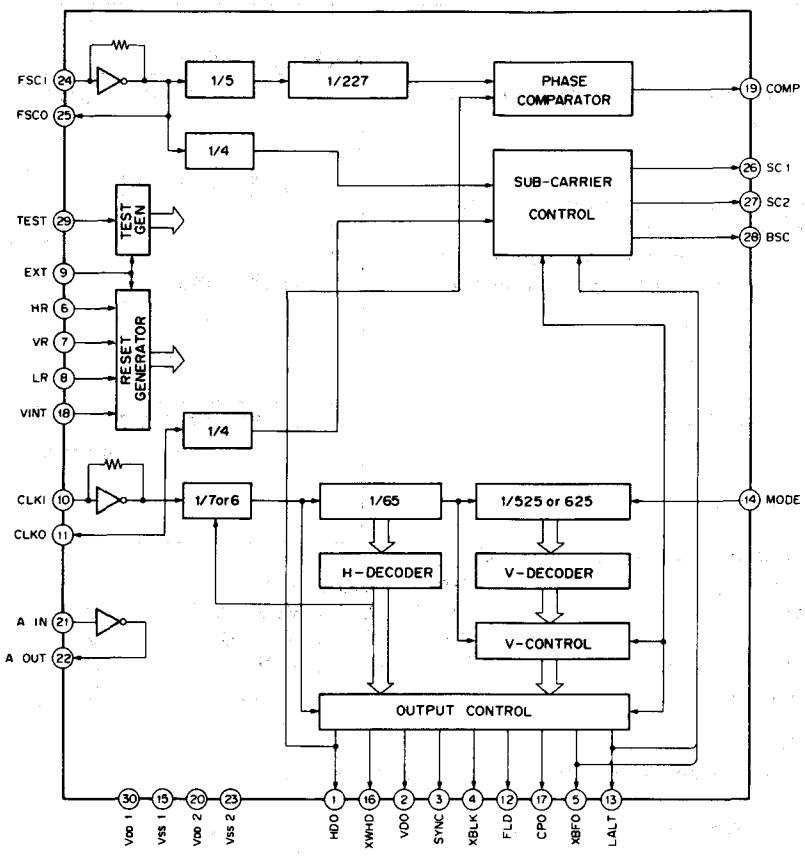
Note) *1. V_{SS} = 0V
*2. Normal value, Transient value 0.5V (20 to 30 ns)

Recommended Operating Conditions

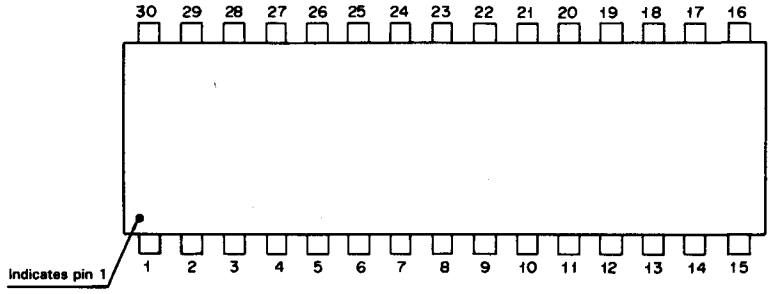
• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	−20 to +75	°C

80307-TO

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	HDO	O	Horizontal drive pulse
2	VDO	O	Vertical drive pulse
3	SYNC	O	Composite sync. pulse
4	XBLK	O	Composite blanking pulse
5	XBFO	O	Burst•flag pulse
6	HR	I	H reset input
7	VR	I	V reset input
8	LR	I	LALT reset input
9	EXT	I	$\overline{\text{INT}}$/EXT mode switching
10	CLKI	I	Clock input
11	CLKO	O	Clock output
12	FLD	O	Field pulse
13	LALT	O	Line alternate pulse
14	MODE	I	NTSC/PAL mode switching NTSC/PAL
15	$V_{SS}1$	—	GND
16	XWHD	O	Wide Horizontal drive pulse
17	CPO	O	Clamp pulse
18	VINT	I	Initialize input
19	COMP	O	Phase comparator output
20	$V_{DD}2$	—	Inverter +5V for filter
21	AIN	I	Inverter input for filter
22	AOUT	O	Inverter output for filter
23	$V_{SS}2$	—	Inverter GND for filter
24	FSCI	I	Clock input 4 f_{sc}
25	FSCO	O	Clock output 4 f_{sc}
26	SC1	O	Sub carrier 1
27	SC2	O	Sub carrier 2
28	BSC	O	Bursted sub carrier
29	TEST	I	Test input (Normally L)
30	$V_{DD}1$	—	+5V

Electrical Characteristics

DC characteristics

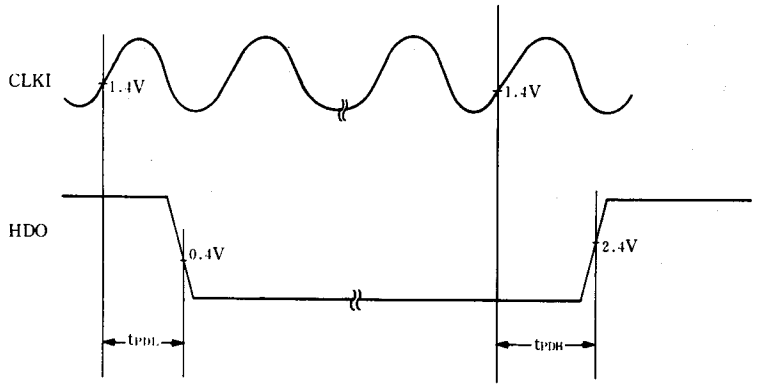
$V_{DD} = 5V \pm 10\%$ $V_{SS} = 0V$ Top = −20 to +75°C

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current		I_{DD}			2.0		mA
		I_{DDS}	Static state*1	0		0.1	mA
Output voltage I*2	H level	V_{OH}	$I_{OH} = -2mA$	$V_{DD} - 0.5$		V_{DD}	V
	L level	V_{OL}	$I_{OL} = 4mA$	V_{SS}		0.4	V
Output voltage II*3	H level	V_{OH}	$I_{OH} = -1.5mA$	2.5		V_{DD}	V
	L level	V_{OL}	$I_{OL} = 1.5mA$	V_{SS}		2.5	V
Input voltage	H level	V_{IH}		0.7 V_{DD}			V
	Level	V_{IL}				0.3 V_{DD}	V
Input leak current		I_{LI}	$V_I = 0V$ to V_{DD}	−10		10	μA
Output leak current*4		I_{OZ}		−10		10	μA

*1. $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$
*2. Output pins except "A OUT"
*3. "A OUT" pin
*4. Tri-state pin 19

AC characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
H to L Propagation delay time	t_{PDL}	$V_{OL} = 0.4V$			45	ns
L to H Propagation delay time	t_{PDH}	$V_{OH} = 2.4V$			45	ns



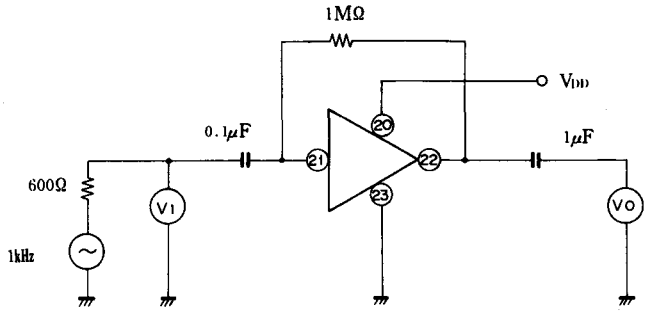
I/O capacitance

$V_{DD}V_I = 0V$, $f_M = 1MHz$

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			8	pF
Output pin	C_{OUT}			8	pF

Filter Amplifier Characteristics

Voltage gain Gv: 25dB (Typ.)



Test circuit

Description of Function

Generation of various synchronizing signals (See the Timing Chart).

Generates various synchronizing signals from Clock.

- Clock frequency:
  NTSC: 910 fH (14.31818 MHz)
  PAL: 908 fH (14.1875 MHz)
  4 fSC (17.734475 MHz)

PLL for PAL 4 fSC

Matches 4 fSC phase, with 908 fH as Master clock.
An active filter is used as filter.

908 fH	4 fSC	COMP
Forward	Back	L
Back	Forward	H

Generation of SC (Sub-Carrier)

Generates three kinds of sub-carrier.
SC1, SC2 and BBC. (Refer to the Timing Chart for phase.)

Mode	Sync.	Sub-carrier (SC)
NTSC	INT	910 fH/4
NTSC	EXT	No output
PAL	INT or EXT	4 fsc/4

INT: INTERNAL mode (EXT = L)

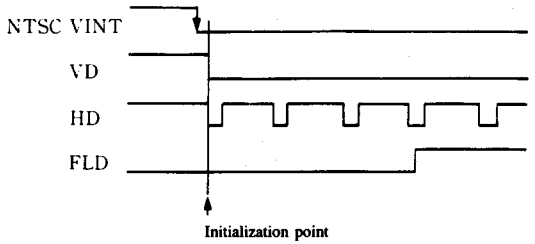
EXT: EXTERNAL mode (EXT = H)

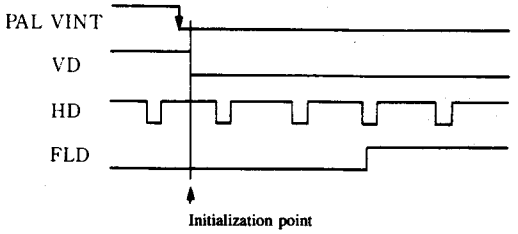
Any unused counter is stopped in any mode.

Initialize and Reset

In the INT mode, the circuit is initialized at falling edge of VINT. H reset, V reset and LALT reset are not accepted in this mode. In the EXT mode, in contrast, VINT is not accepted, while H reset, V reset and LALT reset are accepted.

- Initialize (VINT)
  Detection of VINT's falling edge causes, at the first clock, initialization at the position of falling edge of VD immediately before the ODD (1st) field to start operation. (Initialization is completed within 100 ns from the detection of falling edge.)

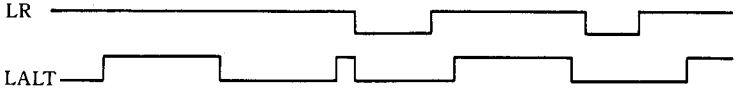




- H reset (HR)
  It is reset at the first falling edge, and not reset unless there is an offset of over 2 clocks (0.98 μs) for the next and subsequent edges. The minimum pulse duration is 0.98 μs.
  The position of reset is at 2.94 to 3.43 μs forward from HR input.

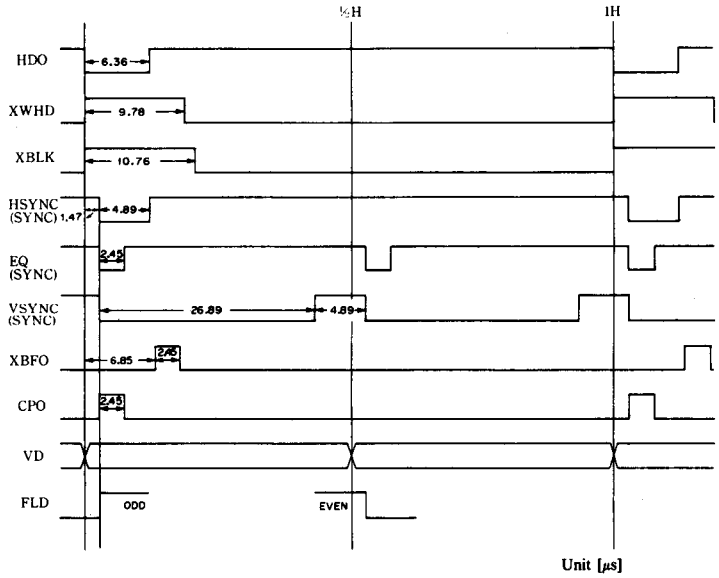
- V reset (VR)
  It is reset at a position of VD at 3.5 H forward from VR. The minimum reset pulse duration is 32 μs.

- LALT reset (LR)
  LALT is reset to the same phase as that of LR input. The minimum reset pulse duration is 32 μs.

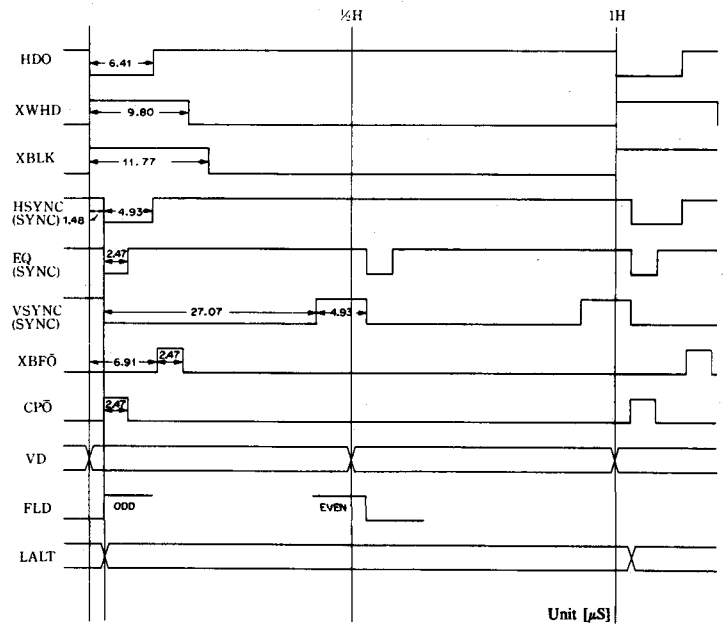


Timing Chart

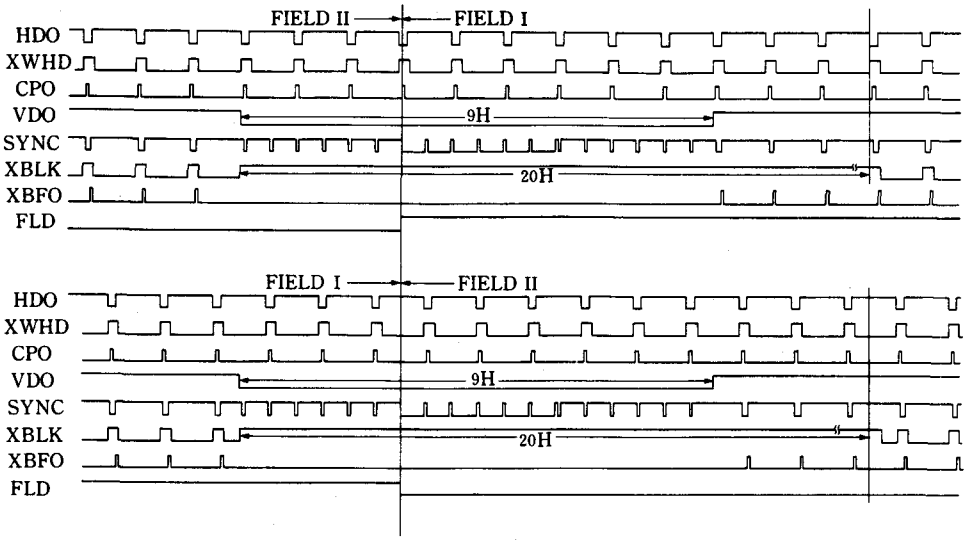
NTSC H



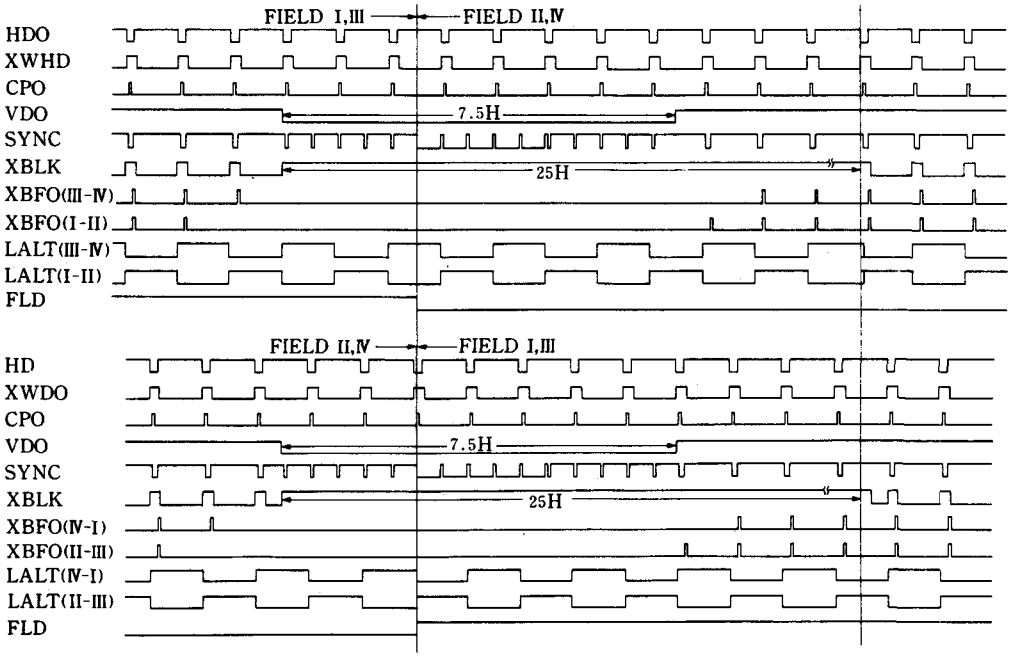
PAL H



NTSC V

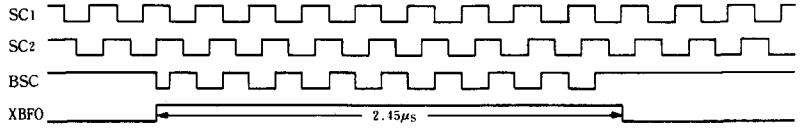

FIELD II
FIELD I
HDO
XWHD
CPO
VDO
SYNC
XBLK
XBFO
FLD
9H
20H
FIELD I
FIELD II
HDO
XWHD
CPO
VDO
SYNC
XBLK
XBFO
FLD
9H
20H

PAL V


FIELD I,III
FIELD II,IV
HDO
XWHD
CPO
VDO
SYNC
XBLK
XBFO(III-IV)
XBFO(I-II)
LALT(III-IV)
LALT(I-II)
FLD
7.5H
25H
FIELD II,IV
FIELD I,III
HD
XWDO
CPO
VDO
SYNC
XBLK
XBFO(IV-I)
XBFO(II-III)
LALT(IV-I)
LALT(II-III)
FLD
7.5H
25H

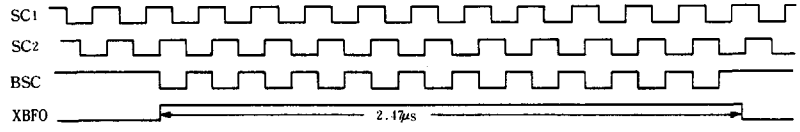
Sub Carrier

NTSC

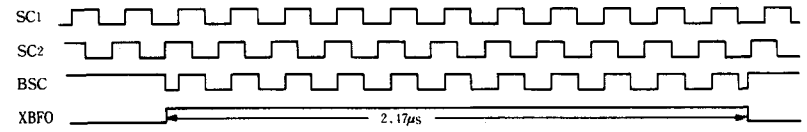


PAL

LALT=H

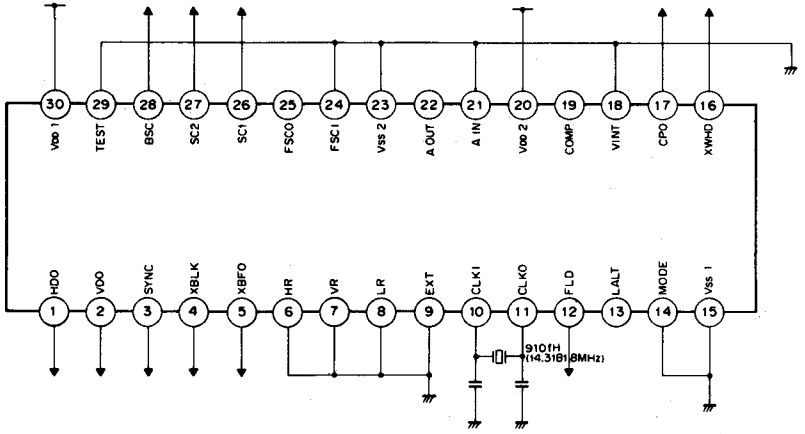


LALT=L

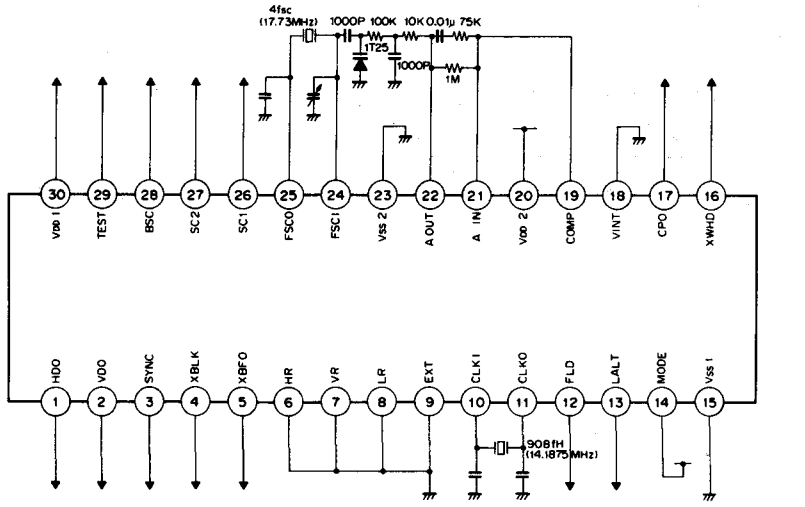


Application Circuit

NTSC (Internal mode)



PAL (Internal mode)



SONY

CXD1159Q

Sync. Signal Generator for Camera

Description

CXD1159Q is a sync. signal generator for consumer video cameras.

32 pin QFP (Plastic)

Features

- Adapts to NTSC or PAL through mode switching.
- Low power consumption.
- Phase comparator and built in inverter for active filter.
- Internal/External sync.

Functions

- Generator of various sync. signals.

Structure

Silicon gate CMOS

Application

- Video cameras

Absolute Maximum Ratings (Ta = 25°C)

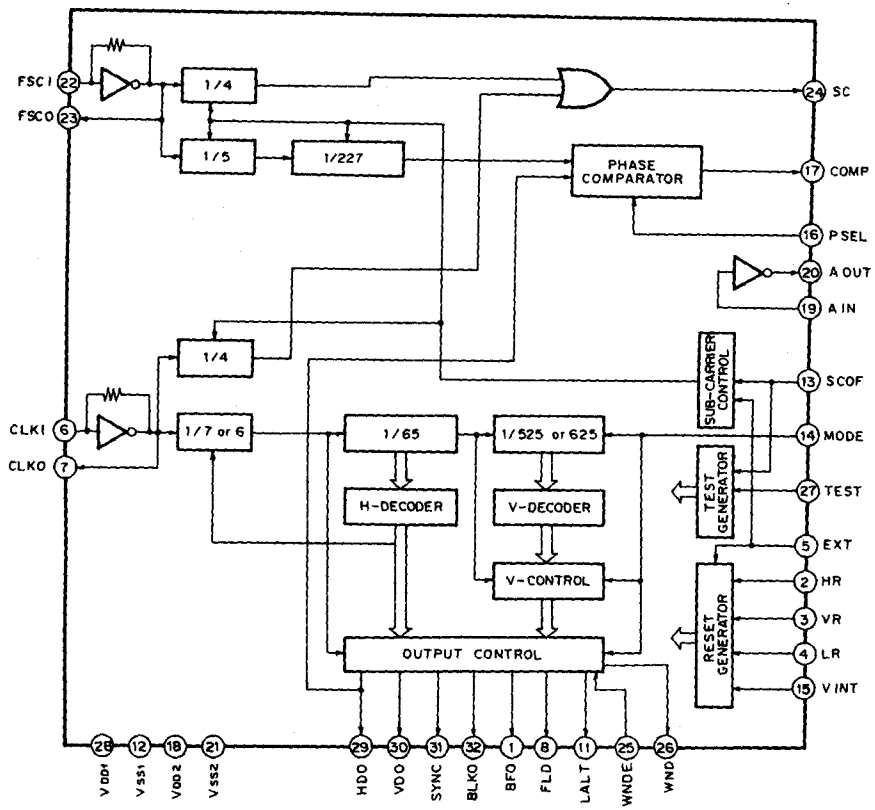
• Supply voltage	V_{DD}	V_{SS} * − 0.5 to 7.0	V
• Input voltage	V_I	V_{SS} * − 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} * − 0.5 to V_{DD} + 0.5	V
• Storage temperature	Tstg	− 55 to + 150	°C

*Vss = 0V

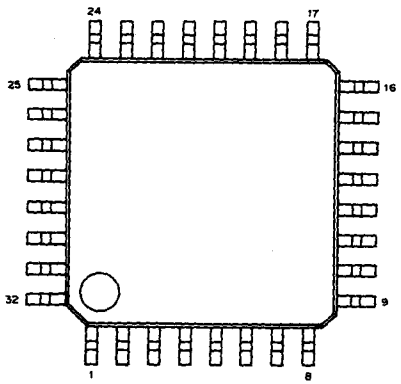
Rcommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	− 20 to + 75	°C

Block Diagram



Pin Configuration



Pin Description

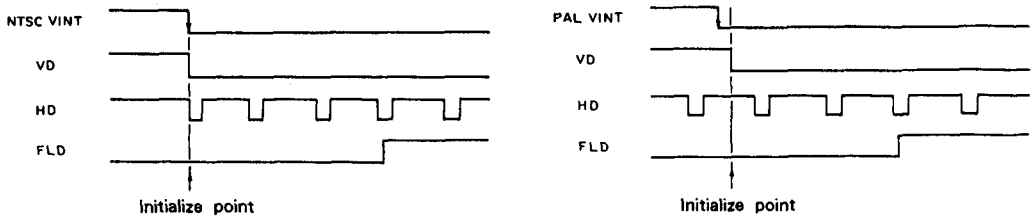
No.	Symbol	I/O	Description
1	BFO	O	Burst flag pulse
2	HR	I	H reset input
3	VR	I	V reset input
4	LR	I	LALT reset input
5	EXT	I	Internal/External mode switching $\overline{INT}$/EXT
6	CLKI	I	Clock input (NTSC : 14.31818MHz, PAL : 14.1875MHz)
7	CLKO	O	Clock output
8	FLD	O	Field pulse
9	N.C.	—	
10	N.C.	—	
11	LALT	O	Line alternate pulse
12	V_{SS1}	—	GND
13	SCOF	I	Sub carrier suppress input L : OFF
14	MODE	I	NTSC/PAL mode switching $\overline{NTSC}$/PAL
15	VINT	I	Initialize input
16	PSEL	I	Phase comparator polarity switch
17	COMP	O	Phase comparator output
18	V_{DD2}	—	+5 power supply for filter inverter
19	AIN	I	Input for filter inverter
20	AOUT	O	Output for filter inverter
21	V_{SS2}	—	GND for filter inverter
22	FSCI	I	4 fsc clock input
23	FSCO	O	4 fsc clock output
24	SC	O	Sub carrier output
25	WNDE	I	WND output enable input (at L : Enable)
26	WND	O	Window output
27	TEST	I	Test input (Normally "L")
28	V_{DD1}	—	+5V
29	HDO	O	Horizontal drive pulse
30	VDO	O	Vertical drive pulse
31	SYNC	O	Composite sync. pulse
32	BLKO	O	Composite blanking pulse

4. Initialization and Reset

In INT mode the circuit is initialized with the fall of VINT. At that time, H, V and LALT resets are not accepted. In EXT mode, VINT is not accepted, whereas H, V and LALT resets are.

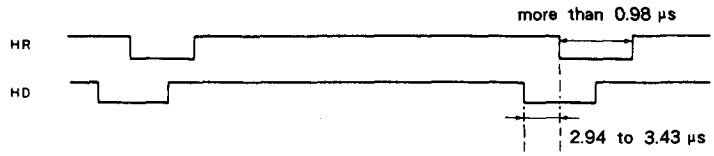
- Initialize (VINT)

  When EXT = L, VINT fall is detected and operation is started as the circuit is initialized at the VD fall position just before field 1. (Initialization is completed within 100ns after the fall is detected).



- H reset (HR)

  Reset is performed with the first fall. However reset is not done anymore unless there is a deviation of more than 2 clocks (0.98 µs) to the subsequent edges.
  The minimum reset pulse width is 0.98 µs.
  HD is reset 2.94 to 3.43 in advance of HR input.



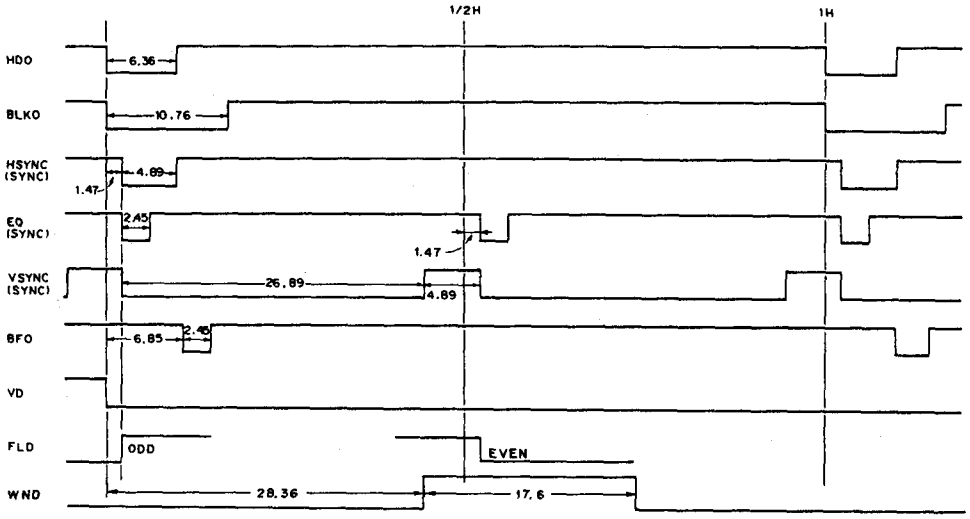
- V reset (VR)

  VD is reset 3.5H in advance of VR input.
  The minimum reset pulse width is 32 µs.

- LALT reset (LR)

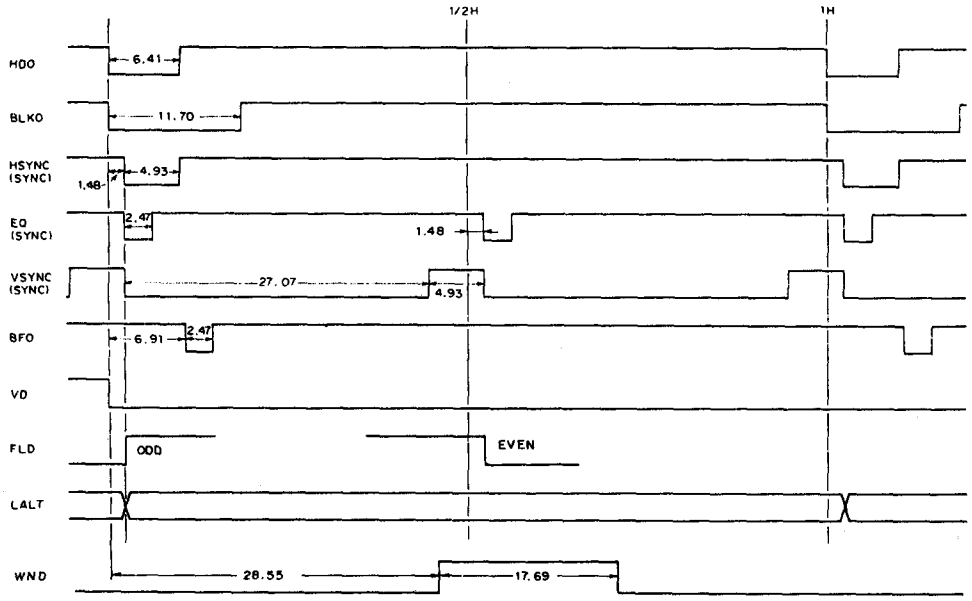
  LALT is reset in the same phase as LR input.
  The minimum reset pulse is 32 µs.

Timing Chart H (NTSC)



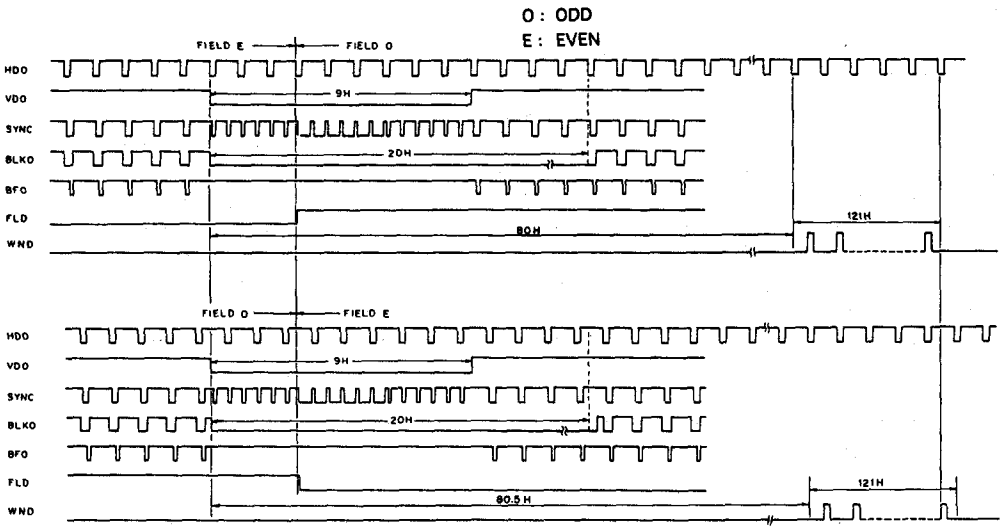
Unit : μs

Timing Chart H (PAL)

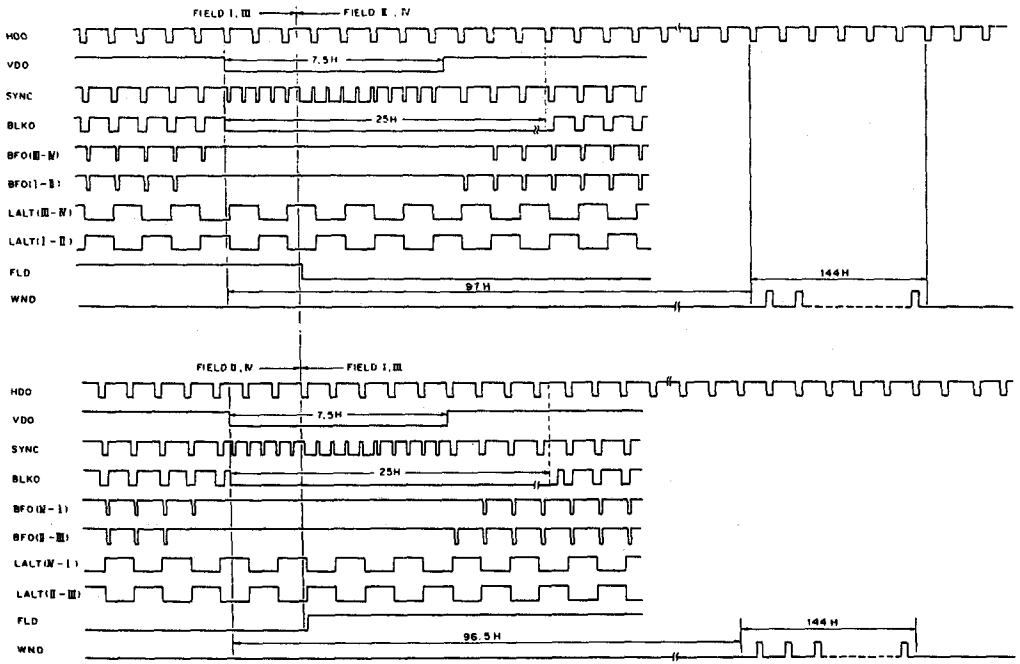


Unit : μs

Timing Chart V (NTSC)

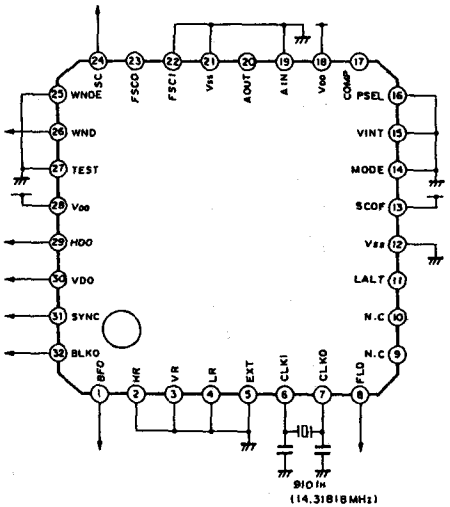


Timing Chart V (PAL)

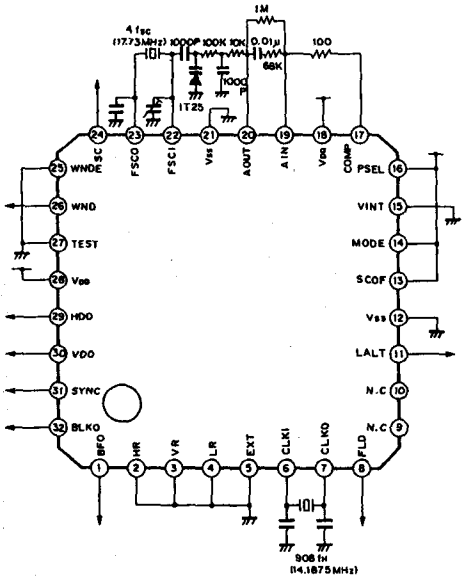


Application Circuit

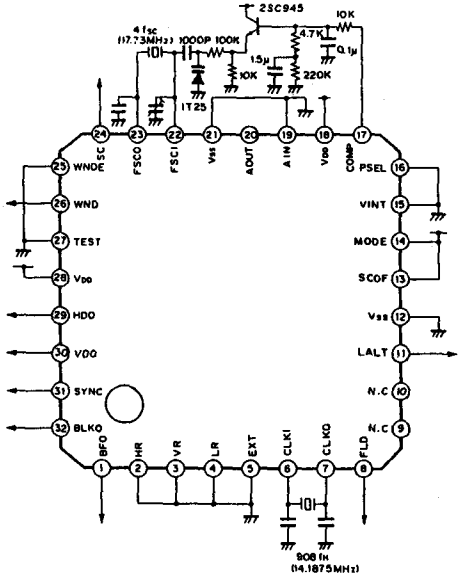
NTSC (Internal mode)



PAL (Filter configuration 2, Internal mode)

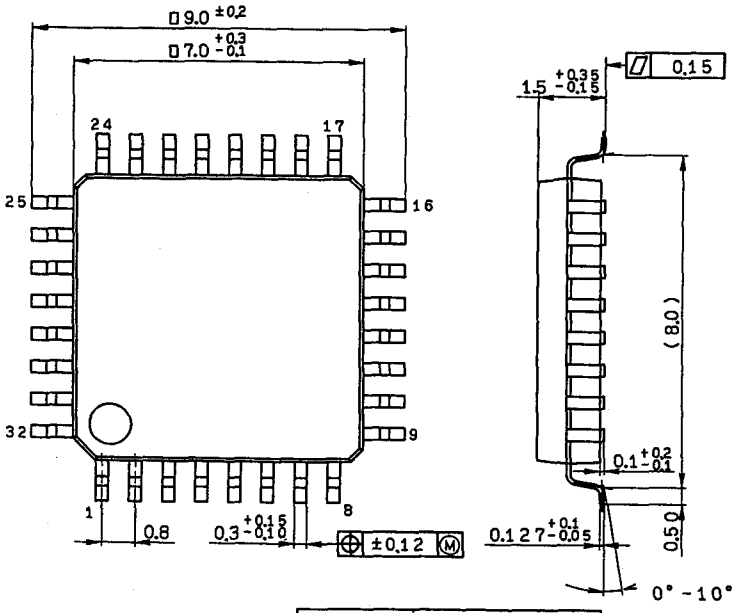


PAL (Filter configuration 1, Internal mode)



Package Outline Unit : mm

32pin QFP (Plastic) 0.2g



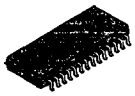
SONY NAME	QFP-32P-L01
EIAJ NAME	*QFP032-P-0707-A
JEDEC CODE	———

SONY

CXD1217M

Synchronizing Signal Generator for Video Camera

28 pin SOP (Plastic)



Description

The CXD1217M is a synchronizing signal generator for color video cameras.

Features

- Compatible with the respective systems, NTSC, PALM, PAL and SECAM
- Output is synchronized with the clock of $910f_H$ or $908f_H$
- 25Hz offset processing by PAL system
- Color framing by the respective systems, NTSC, PALM and PAL
- Possible external synchronization by H reset, V reset and line-switchover reset pins

Applications

Synchronizing signal generator for color video cameras.

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta = 25°C)

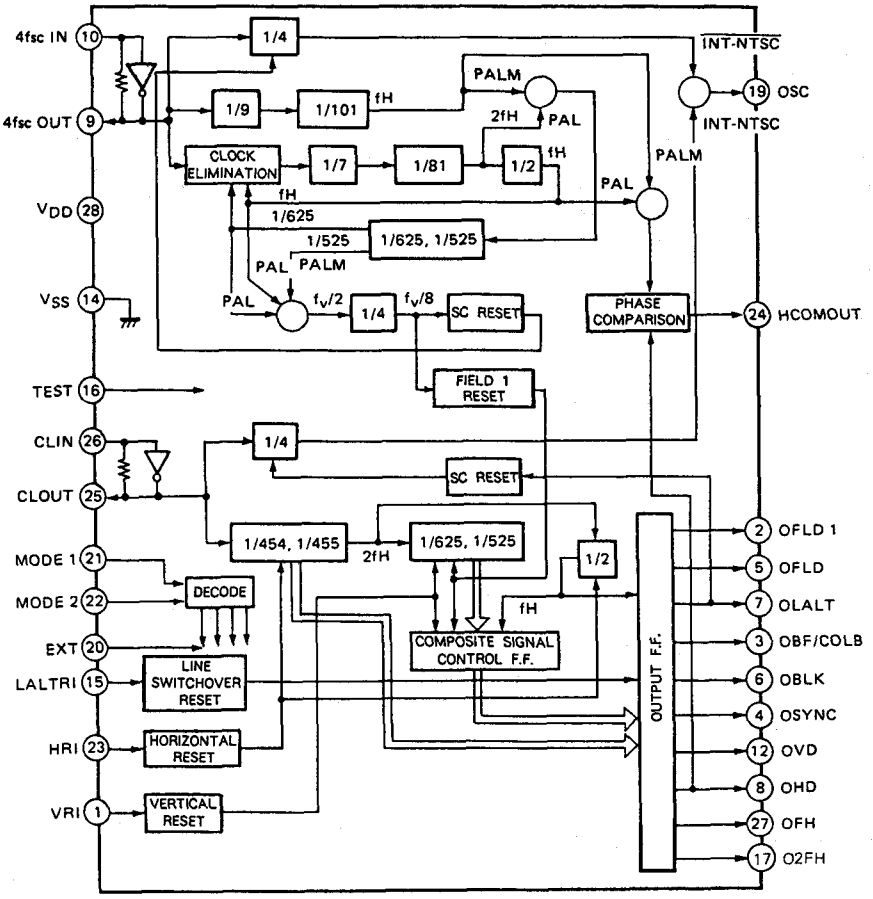
• Supply voltage	V_{DD}	Vss − 0.5 to + 7.0	V
• Input voltage	V_I	Vss − 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	Vss − 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	− 20 to + 75	°C
• Storage temperature	Tstg	− 55 to + 150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	− 20 to + 75	°C

E89626 – ST

Block Diagram and Pin Configuration



Note : Pin 19 output is (a) a signal based on Pin 26 in INT mode at NTSC.
(b) each signal is based on Pin 10 in other modes.

Pin Description

Pin No.	Symbol	I/O	Description
1	VRI	I	Vertical reset signal
2	OFLD1	O	First field output
3	OBF/COLB	O	Burst flag/color blanking output
4	OSYNC	O	Composite sync output
5	OFLD	O	Even and Odd output
6	OBLK	O	Composite blanking output
7	OLALT	O	Line alternate output
8	OHD	O	Horizontal drive output
9	4fscOUT	O	4fsc output
10	4fscIN	I	4fsc input
11	NC	—	
12	OVD	O	Vertical drive output
13	NC	—	
14	Vss	—	GND pin
15	LALTRI	I	Line alternate reset input
16	TEST	I	Test input
17	O2FH	O	$2f_H$ output (Double the frequency of Pin 27)
18	NC	—	
19	OSC	O	Sub carrier output
20	EXT	I	Internal and external synchronizing modes switchover L : Internal synchronization H : External synchronization
21	MODE1	I	System selecting input 1
22	MODE2	I	System selecting input 2
23	HRI	I	Horizontal reset input
24	HCOMOUT	O	Phase comparator output
25	CLOUT	O	Clock output
26	CLIN	I	Clock input
27	OFH	O	Horizontal frequency output
28	V_{DD}	—	Power supply pin

Electrical Characteristics

DC characteristics

(V_{DD} = 5V ± 10%, Vss = 0V, Topr = − 20 to + 75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output voltage 1	V_{OH}	I_{OH} = − 2mA	V_{DD} − 0.5		V_{DD}	V
	V_{OL}	I_{OL} = 4mA	Vss		0.4	V
Output voltage 2*1	V_{OH}	I_{OH} = − 4mA	V_{DD} − 0.5		V_{DD}	V
	V_{OL}	I_{OL} = 4mA	Vss		0.4	V
Output voltage 3*2	V_{OH}	I_{OH} = − 4mA	$V_{DD}/2$			V
	V_{OL}	I_{OL} = 8mA			$V_{DD}/2$	V
Input voltage	V_{IH}		0.7V_{DD}			V
	V_{IL}				0.3V_{DD}	V
Input current*3 (Pull-down pin)	I_{IH}	V_{IH} = V_{DD}	20	50	120	μA
Output leak current*1	I_{LZ}	At high impedance		± 30		nA
Power current supply	I_{DD}	At output pin in no-load		8		mA
Feedback resistance*4	R_{FB}	V_{DD} = 5V	250k		2.5M	Ω

*1 HCOMOUT pin
*2 4fscOUT and CLOUT pins
*3 LALTRI, TEST, EXT, MODE1 and MODE2 pins
*4 4fscOUT, 4fscIN, CLOUT and CL IN pins

I/O capacitance

(V_{DD} = V_I = 0V, f_M = 1 MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input pin	C_{IN}		—	—	9	pF
Output pin	C_{OUT}		—	—	11	pF

Description of Operation (See Block Diagram.)

The CXD1217 is applicable to 4 systems ; namely, NTSC, PAL, PALM and SECAM. In order to realize them, the following relative equations of Sub-carrier (4fscIN) and Clock (CLIN) are adopted.

	Sub carrier	Clock
NTSC	4fsc = 910fH	910fH
PAL	4fsc = 1135fH + 2fv	908fH
PALM	4fsc = 909fH	910fH
SECAM	———	908fH

As it is obvious from the above equations, the 4fsc and clock frequency do not coincide with each other in the PAL and PALM. Therefore matching of the clock frequency is carried out by providing PLL.

1. MODE specified input

The CXD1217 provides 4 inputs to specify the respective modes.

* EXT input : Set this pin to V_{DD} side, and it becomes into external synchronizing mode. At this time, the counters in connection with the PLL loop as shown in the upper part of the block diagram become into stand still state.
* MODE1 and MODE2 inputs : These are inputs for the system selection.

MODE1	MODE2	System
0	0	NTSC
0	1	SECAM
1	0	PALM
1	1	PAL

"0" → Vss
"1" → V_{DD}

* TEST input : An input to be used to measure IC. This input is normally kept opened. (Because it is dropped internally to Vss with MOS resistance.)

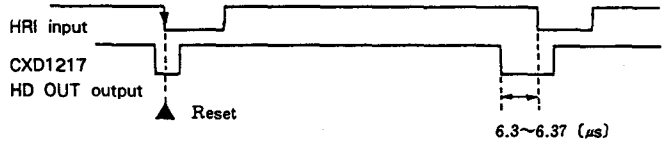
2. Reset operation

The CXD1217 has three reset inputs ; namely, HRI, VRI, LALTRI, and it works to perform reset operation when it detects falling edge. These three inputs are so designed as to take in synchronization with the IC internal clock. Therefore, it is a prerequisite that both systems should have clock frequencies that are matched as a reset operation to each other (GEN locked).

* H reset (HRI input)

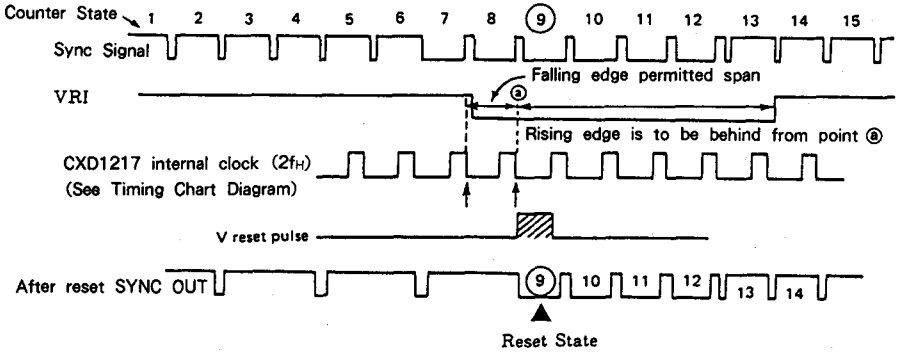
When the HRI input is continuous with H synchronization, resetting is activated with the initial falling edge, and for the subsequent edges they do not have to be reset unless they are deviated more than 2-bit (140ns) against the initial edge in the internal clock. That is, if the jitter of HRI input is less than 140ns, it is absorbed. The minimum resetting pulse width is over 0.3 µs.

The phase to be reset is the advanced point of 6.3 to 6.37 µs (=90 to 91-bit X 70ns) than the HRI input as shown in the diagram below.



• V reset (VRI input)

When the VRI is input as shown in figure below, OSYNC can be reset at the same phase with the SYNC signal.



Since the falling edge point in the diagram above (marked with ↑) is the boundary of reset, if the falling edge of the VRI input traverses that point, it causes 1/2H deviation to the reset state.

Accordingly, if resetting is applied between two similar systems whose frequency are different, the V to which resetting is applied generates jitter of 1/2H. (When the resetting is applied continuously.)

• LALT reset (LALTRI input)

Phase relation between LALTRI pulse polarity and 2FH is the same as in the case of V resetting.

Resetting operation is basically required only in the external synchronizing mode (GEN LOCK mode). However, even in the internal synchronizing mode, it sometimes requires H and V outputs whose phases are deviated against a certain output. In that case, it suffices to use two CXD1217s and conduct the operation as follows :

By varying the Delay and Shift Reg. of the above diagram, any phases of OHD2 and OVD2 can be provided against the respective OHD1 OVD1.

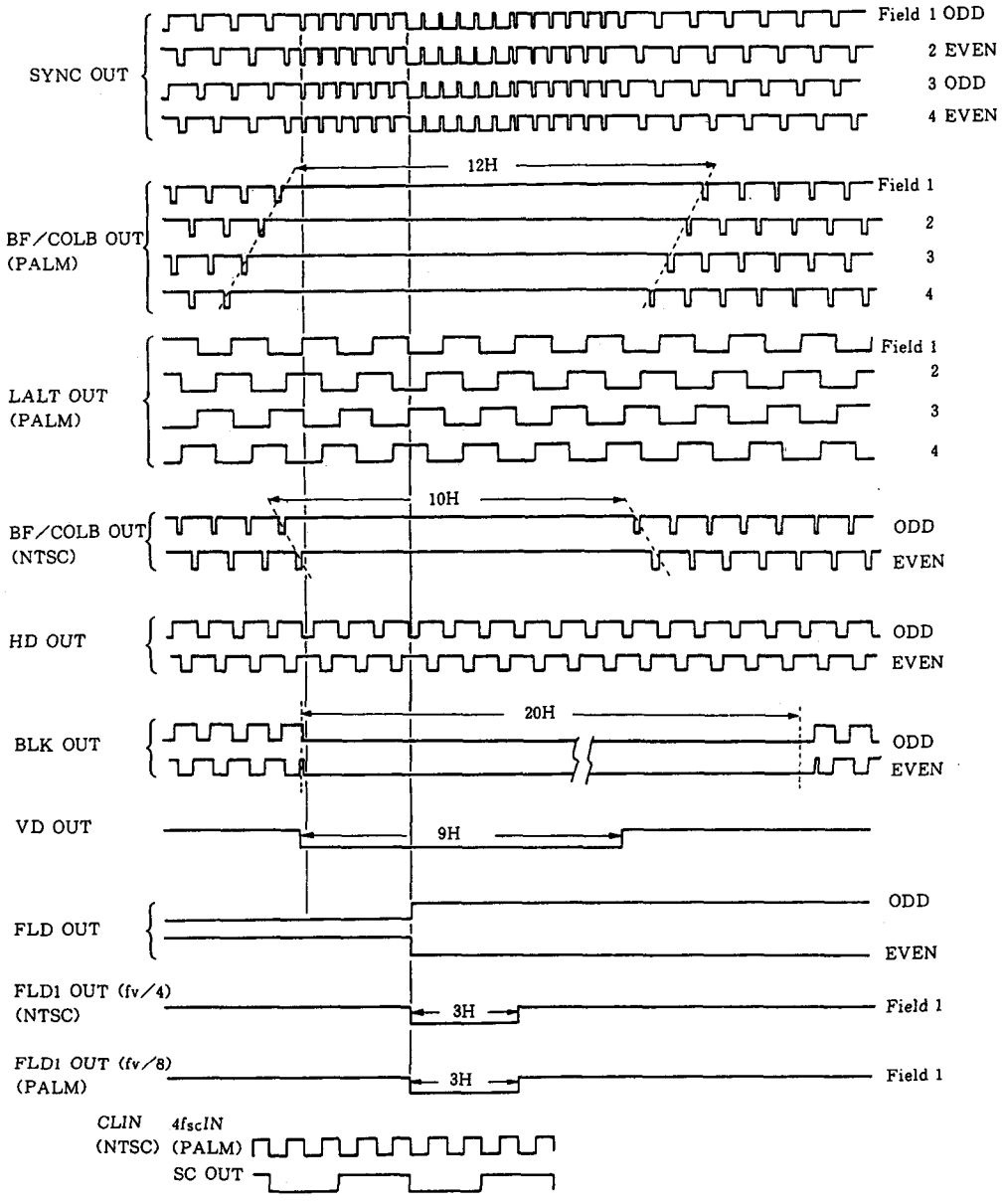
3. Color framing

In the case of internal synchronization in the individual NTSC, PAL and PALM systems, the phase relationships between SYNC of the 1st field and sub-carrier are kept stable regardless of the power supply being ON or OFF. However, as the PAL and PALM systems are comprised of PLL, the absolute values concerning the phase according to variation of the ambient temperature drifts.

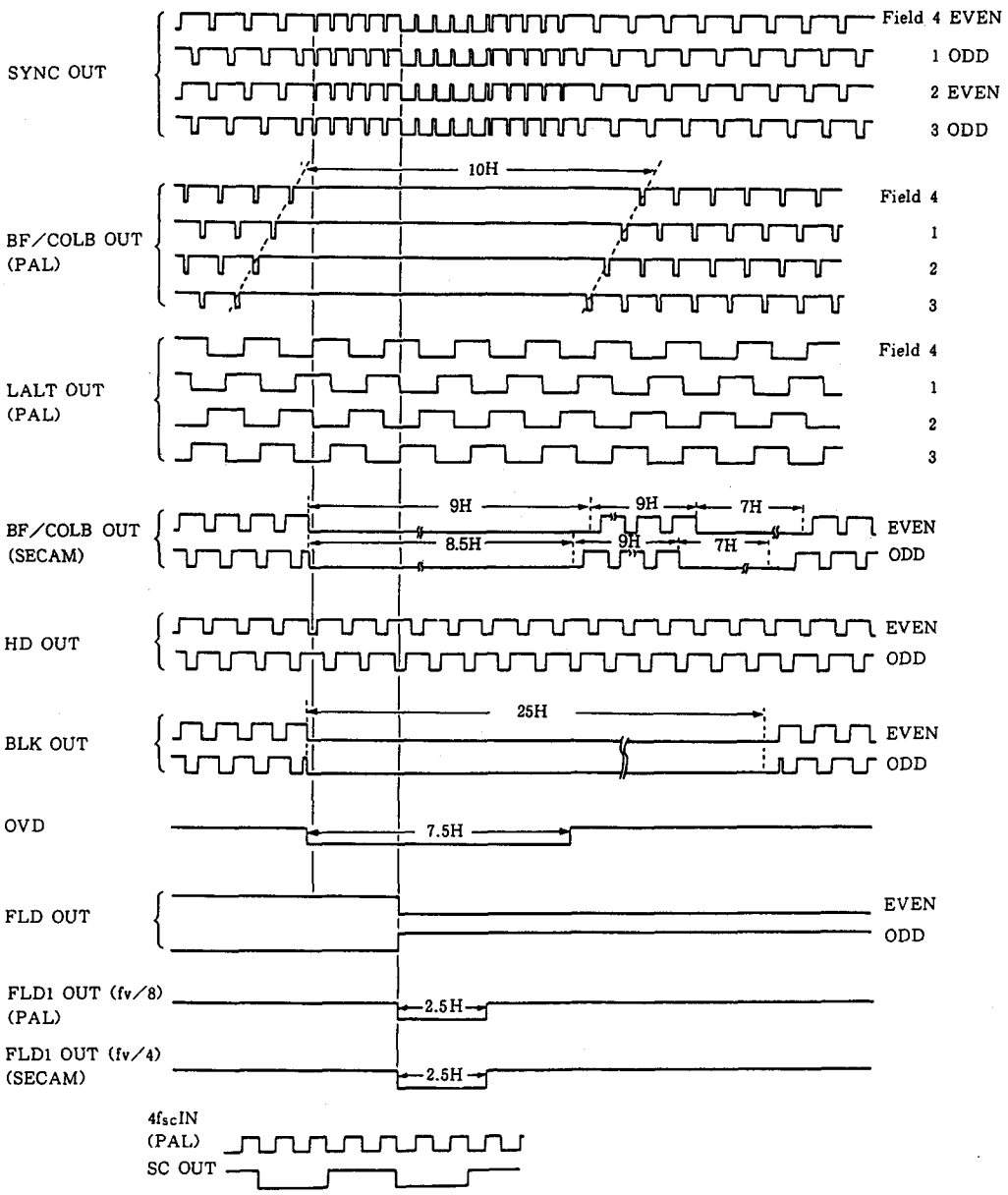
Timing Chart

Output Timing Chart Diagram

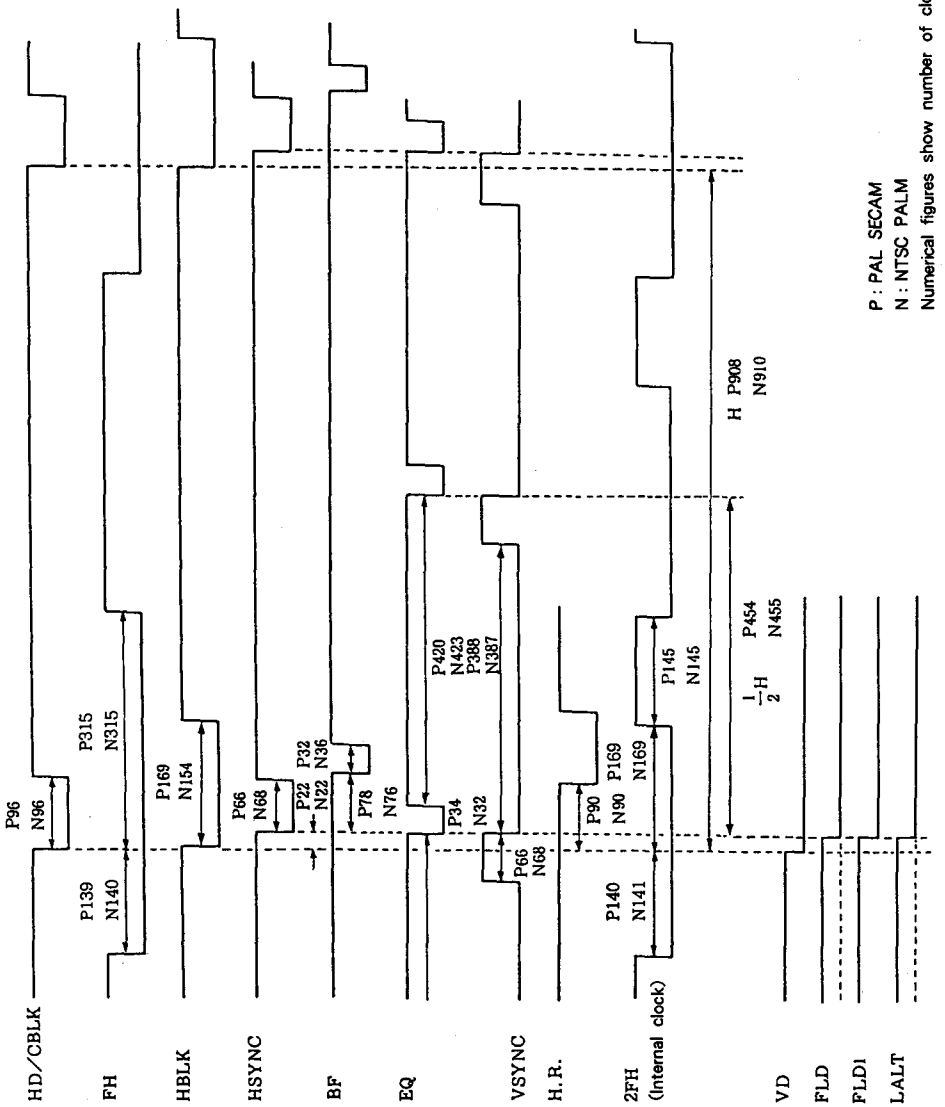
CXD1217 NTSC, PALM



CXD1217 PAL, SECAM



CXD1217 fH

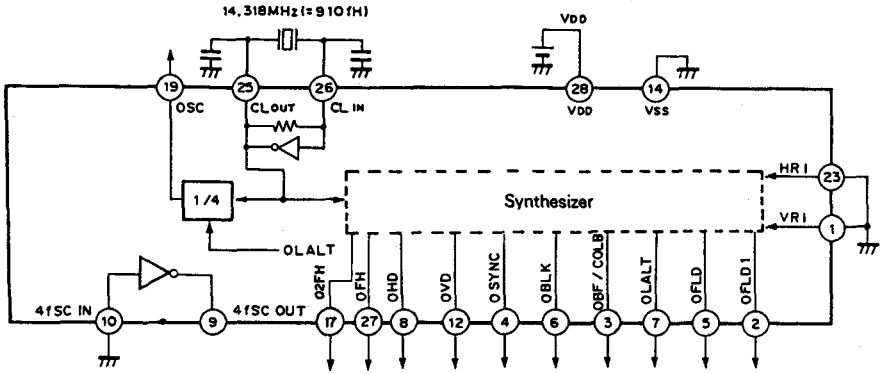

HD/CBLK
FH
HBLK
HSYNC
BF
EQ
VSYNC
H.R.
2FH (Internal clock)
VD
FLD
FLDI
LALT
P96
N96
P139
N140
P315
N315
P169
N154
P66
N68
P22
N22
P32
N36
P78
N76
P34
N32
P420
N423
P388
N387
P66
N68
P90
N90
P169
N169
P140
N141
P145
N145
H P908
N910
1/2H P454
N455
P : PAL SECAM
N : NTSC PALM
Numerical figures show number of clocks

Application Circuit

Basic connection in individual systems

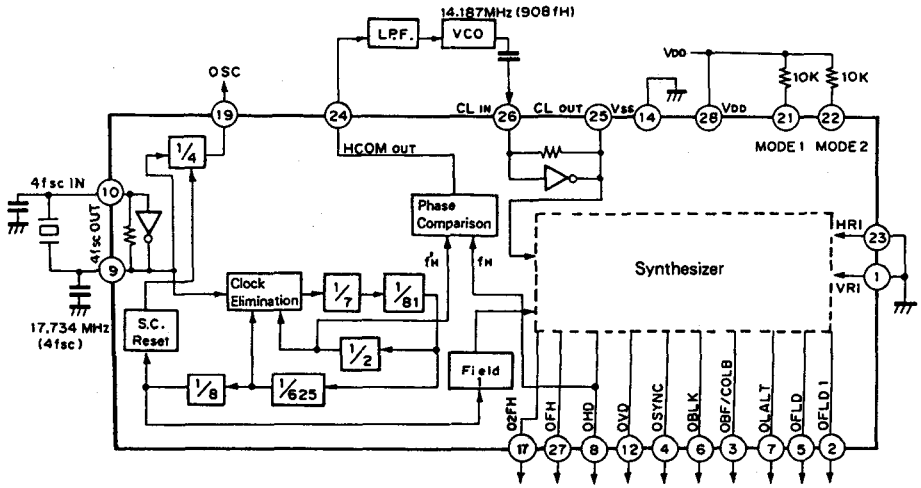
Basic connection in individual systems at internal synchronization mode (EXT input = "0") is as follows. See waveform diagram for each output.

• NTSC



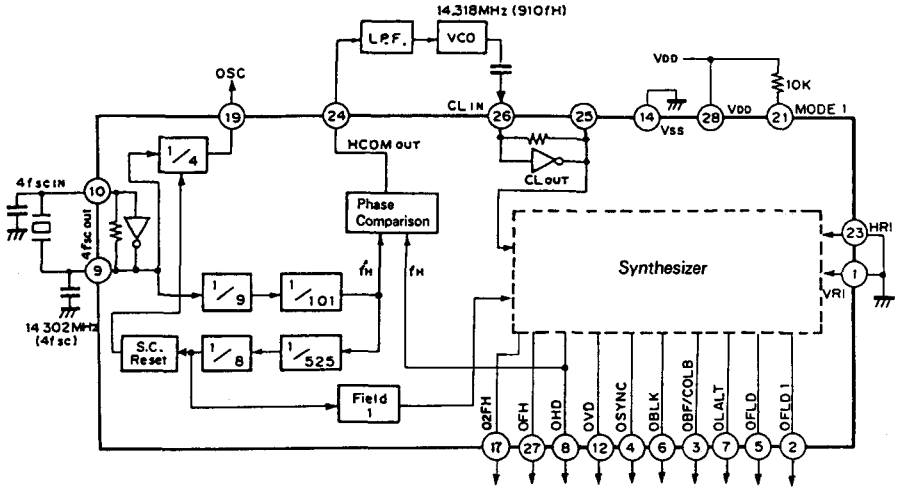
* H/2 is output for LALT OUT even in NTSC mode.
* MODE1, MODE2, EXT, TEST and LALTRI pins can be kept open.
  (If noise annoys, connect to Vss by low impedance.)

• PAL



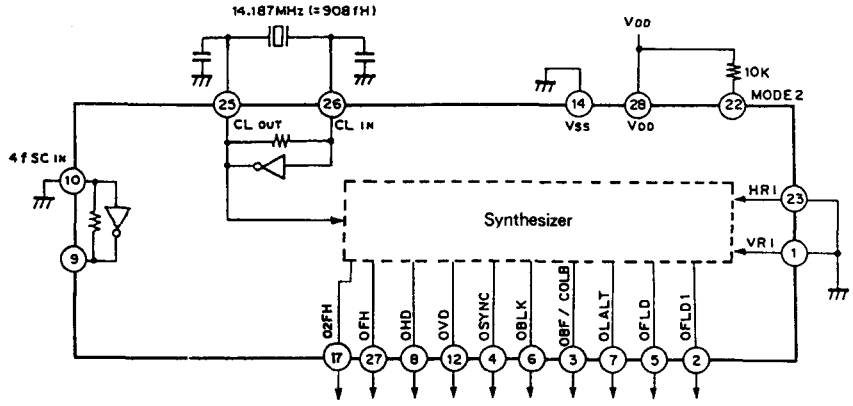
* Inverter of CLIN or CLOUT pins are usable as VCO.

• PALM



* Internal inverter is usable as VCO.

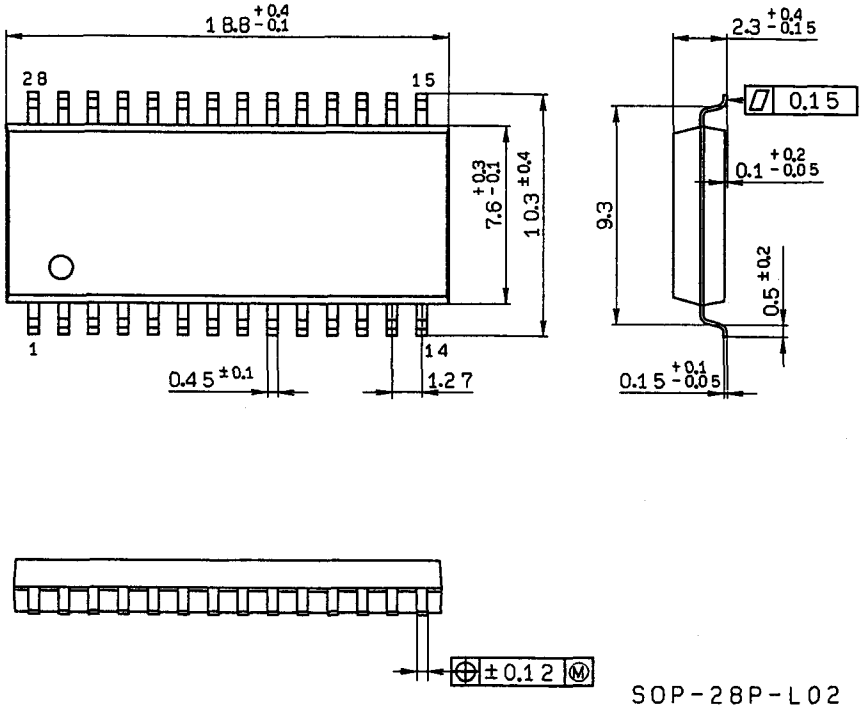
• SECAM



* COLB is output to BF/COLB OUT pin.
* S_{DR} and S_{DB} are formed in PLL using 908f_H.

Package Outline Unit : mm

28 pin SOP (Plastic) 375mil 0.6g



SOP-28P-L02

SONY

CXD1217Q

Synchronizing Signal Generator for Video Camera

Description

The CXD1217Q is a synchronizing signal generator for color video cameras.

32 pin QFP (Plastic)

Features

- Compatible with the respective systems, NTSC, PALM, PAL and SECAM
- Output is synchronized with the clock of 910f_H or 908f_H
- 25Hz offset processing by PAL system
- Color framing by the respective systems, NTSC, PALM and PAL
- Possible external synchronization by H reset, V reset and line-switchover reset pins

Applications

Synchronizing signal generator for color video cameras.

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta=25℃)

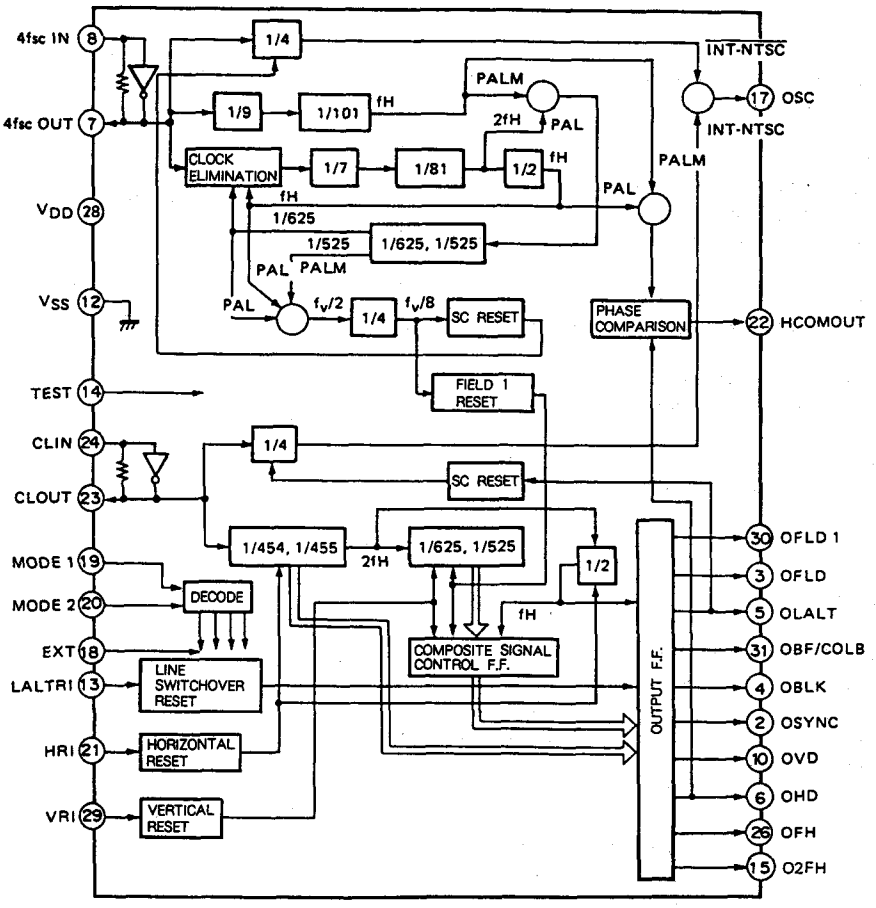
• Supply voltage	V_{DD}	Vss–0.5 to +7.0	V
• Input voltage	V_I	Vss–0.5 to V_{DD}+0.5	V
• Output voltage	V_O	Vss–0.5 to V_{DD}+0.5	V
• Operating temperature	Topr	–20 to +75	℃
• Storage temperature	Tstg	–55 to +150	℃

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	–20 to +75	℃

E90806 – ST

Block Diagram and Pin Configuration



Note: Pin 17 output is (a) a signal based on Pin 24 in INT mode at NTSC.
(b) each signal is based on Pin 8 in other modes.

Pin Description

Pin No.	Symbol	I/O	Description
1	NC	—	
2	OSYNC	O	Composite sync output
3	OFLD	O	Even and Odd output
4	OBLK	O	Composite blanking output
5	OLALT	O	Line alternate output
6	OHD	O	Horizontal drive output
7	4fscOUT	O	4fsc output
8	4fscIN	I	4fsc input
9	NC	—	
10	OVD	O	Vertical drive output
11	NC	—	
12	Vss	—	GND pin
13	LALTRI	I	Line alternate reset input
14	TEST	I	Test input
15	O2FH	O	$2f_H$ output (Double the frequency of Pin 27)
16	NC	—	
17	OSC	O	Sub carrier output
18	EXT	I	Internal and external synchronizing modes switchover L: Internal synchronization H: External synchronization
19	MODE1	I	System selecting input 1
20	MODE2	I	System selecting input 2
21	HRI	I	Horizontal reset input
22	HCOMOUT	O	Phase comparator output
23	CLOUT	O	Clock output
24	CLIN	I	Clock input
25	NC	—	
26	OFH	O	Horizontal frequency output
27	NC	—	
28	V_{DD}	—	Power supply pin
29	VRI	I	Vertical reset signal
30	OFLD1	O	First field output
31	OBF/COLB	O	Burst flag/color blanking output
32	NC	—	

Electrical Characteristics

DC characteristics

(V_{DD}=5V ± 10%, Vss=0V, Topr=–20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output voltage 1	V_{OH}	I_{OH}=–2mA	V_{DD}–0.5		V_{DD}	V
	V_{OL}	I_{OL}=4mA	Vss		0.4	V
Output voltage 2 *1	V_{OH}	I_{OH}=–4mA	V_{DD}–0.5		V_{DD}	V
	V_{OL}	I_{OL}=4mA	Vss		0.4	V
Output voltage 3 *2	V_{OH}	I_{OH}=–4mA	V_{DD}/2			V
	V_{OL}	I_{OL}=8mA			V_{DD}/2	V
Input voltage	V_{IH}		0.7V_{DD}			V
	V_{IL}				0.3V_{DD}	V
Input current *3 (Pull-down pin)	I_{IH}	V_{IH}=V_{DD}	20	50	120	µA
Output leak current *1	I_{LZ}	At high impedance		± 30		nA
Power current supply	I_{DD}	At output pin in no-load		8		mA
Feedback resistance *4	R_{FB}	V_{DD}=5V	250k		2.5M	Ω

*1 HCOMOUT pin
*2 4fscOUT and CLOUT pins
*3 LALTRI, TEST, EXT, MODE1 and MODE2 pins
*4 4fscOUT, 4fscIN, CLOUT and CL IN pins

I/O capacitance

(V_{DD}=V_I=0V, f_M=1 MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input pin	C_{IN}		—	—	9	pF
Output pin	C_{OUT}		—	—	11	pF

Description of Operation (See Block Diagram.)

The CXD1217 is applicable to 4 systems; namely, NTSC, PAL, PALM and SECAM. In order to realize them, the following relative equations of Sub-carrier (4fscIN) and Clock (CLIN) are adopted.

	Sub carrier	Clock
NTSC	4fsc=910fH	910fH
PAL	4fsc=1135fH+2fV	908fH
PALM	4fsc=909fH	910fH
SECAM	———	908fH

As it is obvious from the above equations, the 4fsc and clock frequency do not coincide with each other in the PAL and PALM. Therefore matching of the clock frequency is carried out by providing PLL.

1. MODE specified input

The CXD1217 provides 4 inputs to specify the respective modes.

* EXT input: Set this pin to VDD side, and it becomes into external synchronizing mode. At this time, the counters in connection with the PLL loop as shown in the upper part of the block diagram become into stand still state.
* MODE1 and MODE2 inputs: These are inputs for the system selection.

MODE1	MODE2	System
0	0	NTSC
0	1	SECAM
1	0	PALM
1	1	PAL

"0" → Vss
"1" → VDD

* TEST input: An input to be used to measure IC. This input is normally kept opened. (Because it is dropped internally to Vss with MOS resistance.)

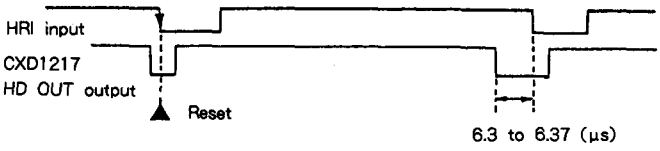
2. Reset operation

The CXD1217 has three reset inputs; namely, HRI, VRI, LALTRI, and it works to perform reset operation when it detects falling edge. These three inputs are so designed as to take in synchronization with the IC internal clock. Therefore, it is a prerequisite that both systems should have clock frequencies that are matched as a reset operation to each other (GEN locked).

* H reset (HRI input)

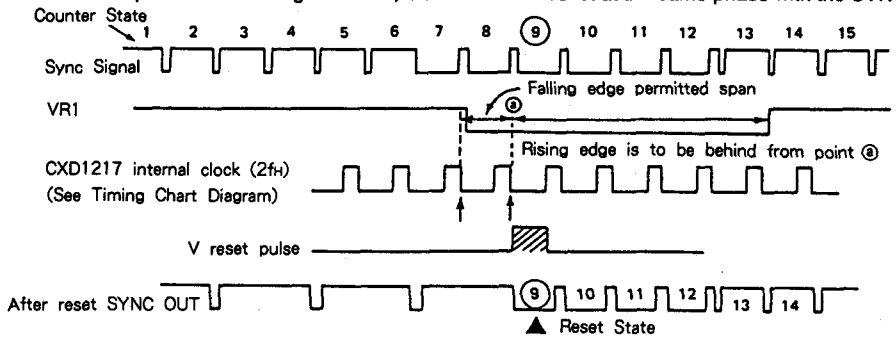
When the HRI input is continuous with H synchronization, resetting is activated with the initial falling edge, and for the subsequent edges they do not have to be reset unless they are deviated more than 2-bit (140ns) against the initial edge in the internal clock. That is, if the jitter of HRI input is less than 140ns, it is absorbed. The minimum resetting pulse width is over 0.3 µs.

The phase to be reset is the advanced point of 6.3 to 6.37 µs (=90 to 91-bit X 70ns) than the HRI input as shown in the diagram below.



• V reset (VRI input)

When the VRI is input as shown in figure below, OSYNC can be reset at the same phase with the SYNC signal.

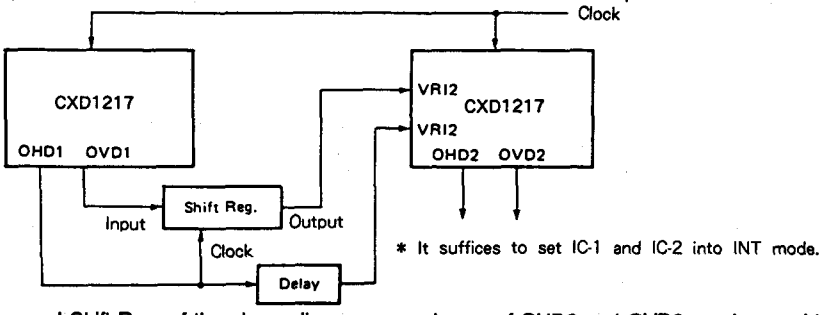


Since the falling edge point in the diagram above (marked with ↑) is the boundary of reset, if the falling edge of the VRI input traverses that point, it causes 1/2H deviation to the reset state.
Accordingly, if resetting is applied between two similar systems whose frequency are different, the V to which resetting is applied generates jitter of 1/2H. (When the resetting is applied continuously.)

• LALT reset (LALTRI input)

Phase relation between LALTRI pulse polarity and 2FH is the same as in the case of V resetting.

Resetting operation is basically required only in the external synchronizing mode (GEN LOCK mode). However, even in the internal synchronizing mode, it sometimes requires H and V outputs whose phases are deviated against a certain output. In that case, it suffices to use two CXD1217s and conduct the operation as follows:



By varying the Delay and Shift Reg. of the above diagram, any phases of OHD2 and OVD2 can be provided against the respective OHD1 OVD1.

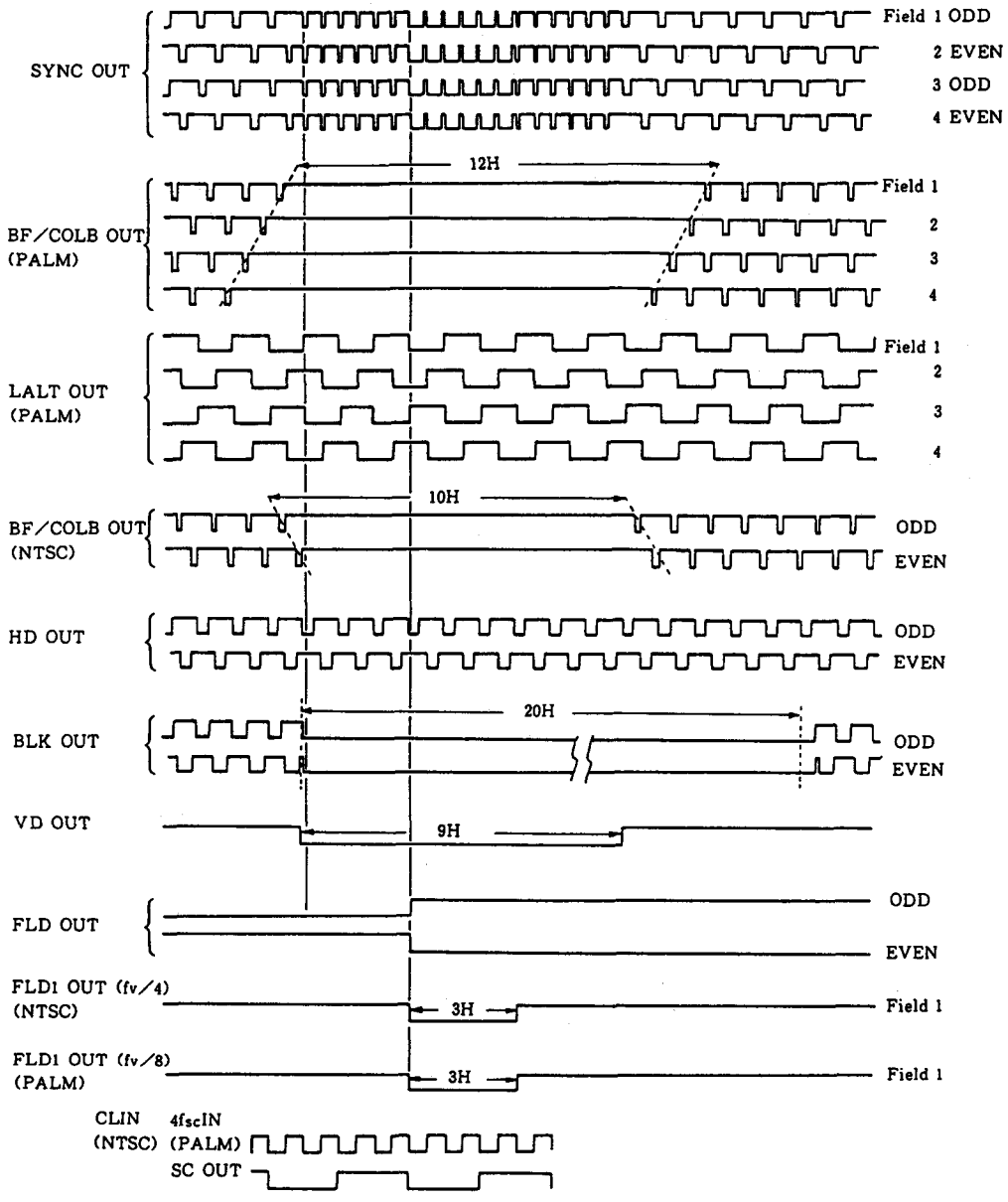
3. Color framing

In the case of internal synchronization in the individual NTSC, PAL and PALM systems, the phase relationships between SYNC of the 1st field and sub-carrier are kept stable regardless of the power supply being ON or OFF. However, as the PAL and PALM systems are comprised of PLL, the absolute values concerning the phase according to variation of the ambient temperature drifts.

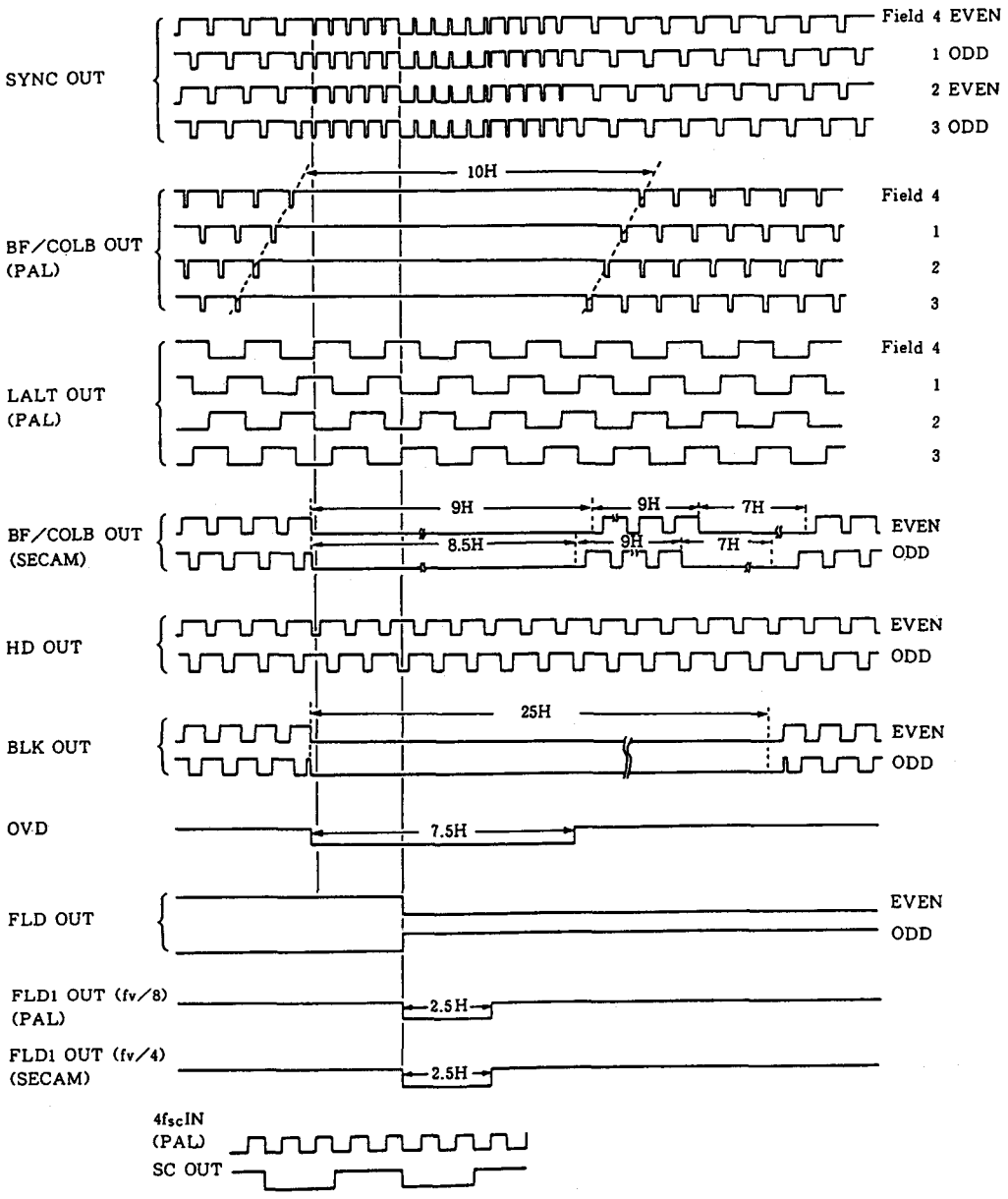
Timing Chart

Output Timing Chart Diagram

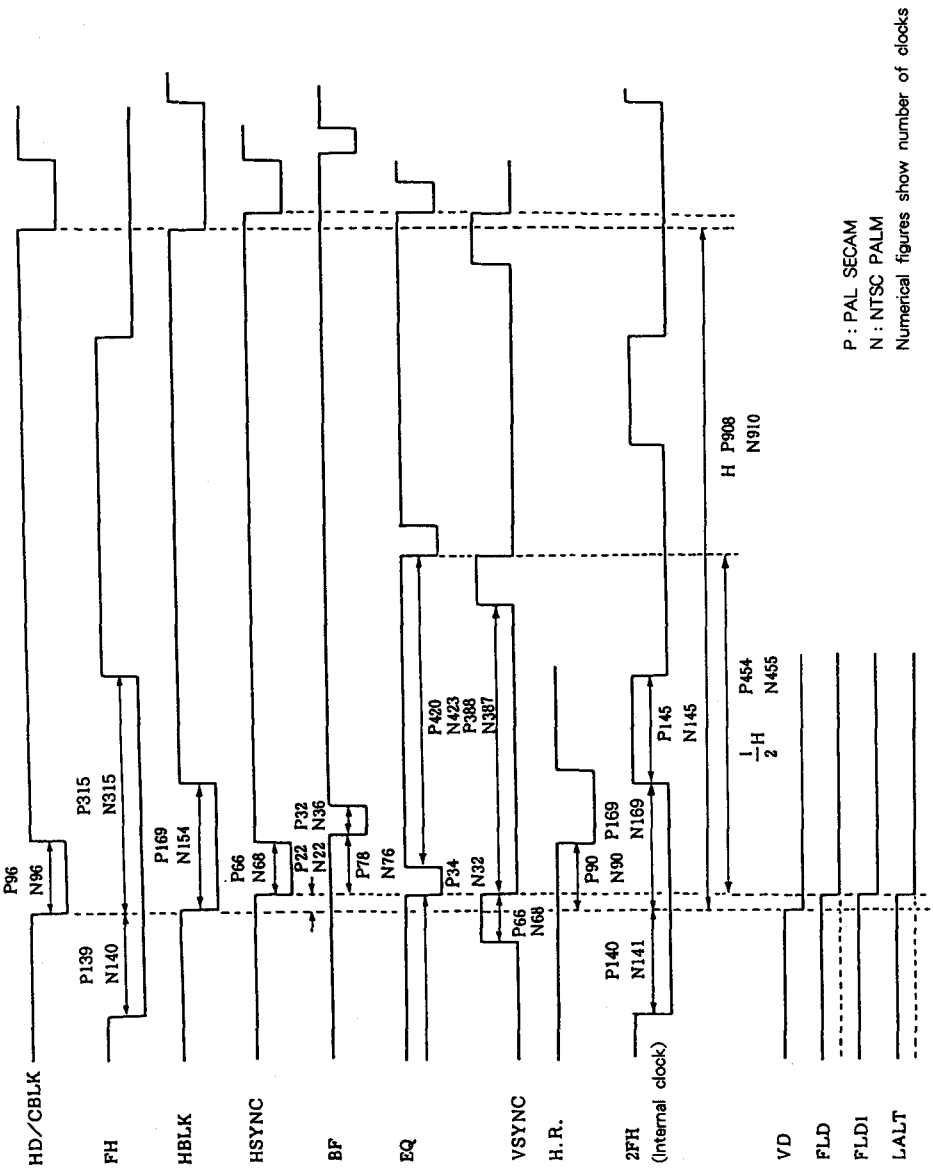
CXD1217 NTSC, PALM



CXD1217 PAL, SECAM



CXD1217 fH

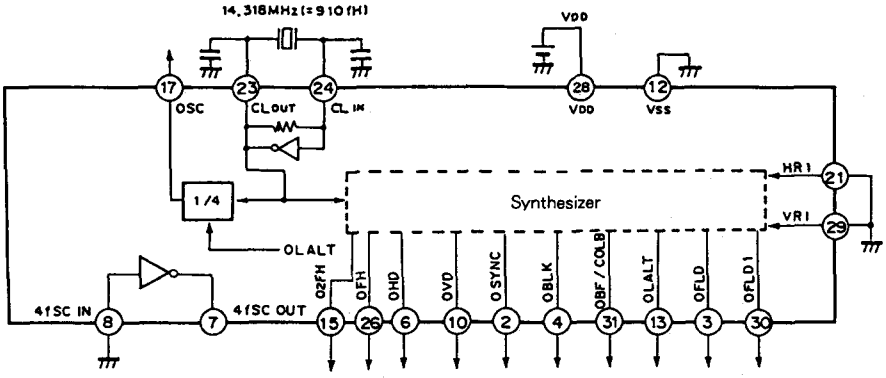

HD/CBLK
FH
HBLK
HSYNC
BF
EQ
VSYNC
H.R.
2FH
(Internal clock)
VD
FLD
FLD1
LALT
P96
N96
P315
N315
P139
N140
P169
N154
P66
N68
P22
N22
P32
N36
P78
N76
P34
N32
P420
N423
P388
N387
P66
N68
P90
N90
P169
N169
P140
N141
P145
N145
H P908
N910
1/2H P454
N455
P : PAL SECAM
N : NTSC PALM
Numerical figures show number of clocks

Application Circuit

Basic connection in individual systems

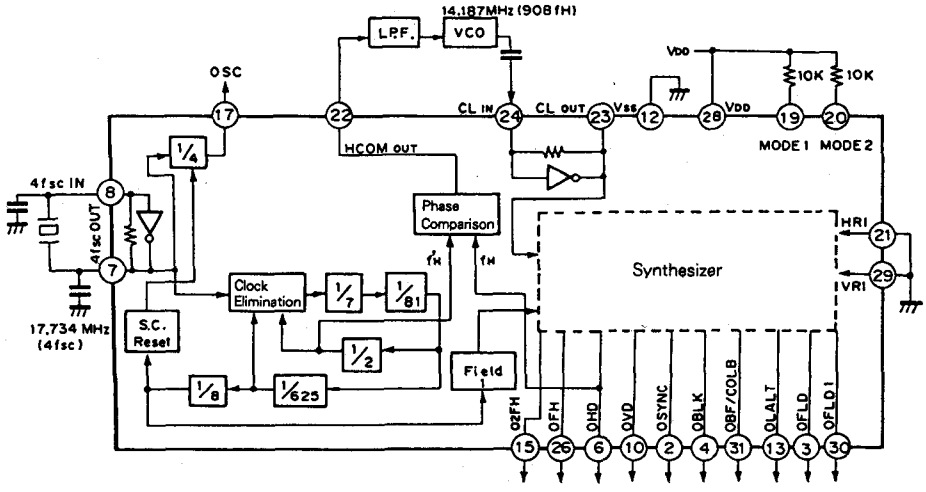
Basic connection in individual systems at internal synchronization mode (EXT input="0") is as follows. See waveform diagram for each output.

• NTSC



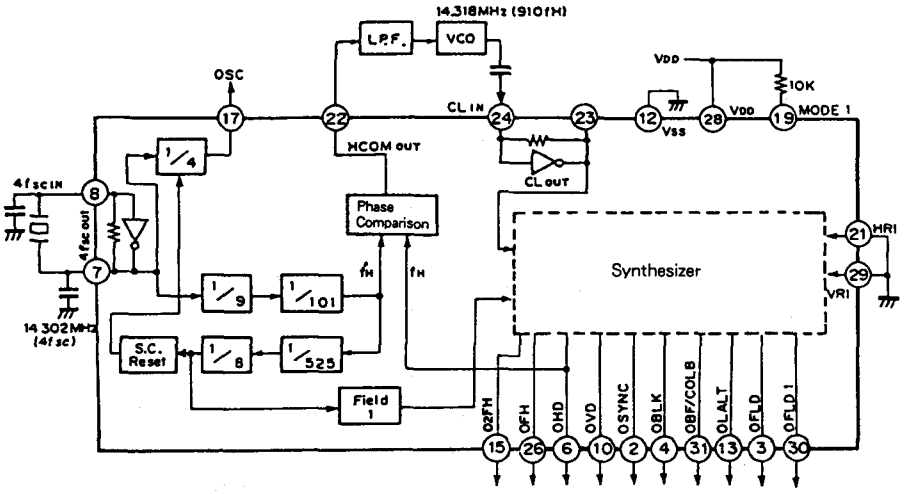
* H/2 is output for LALT OUT even in NTSC mode.
* MODE1, MODE2, EXT, TEST and LALTRI pins can be kept open.
(If noise annoys, connect to Vss by low impedance.)

• PAL



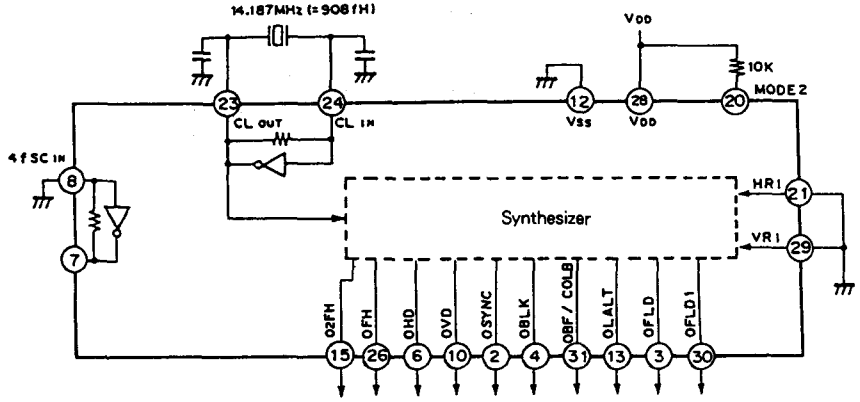
* Inverter of CLIN or CLOUT pins are usable as VCO.

• PALM



* Internal inverter is usable as VCO.

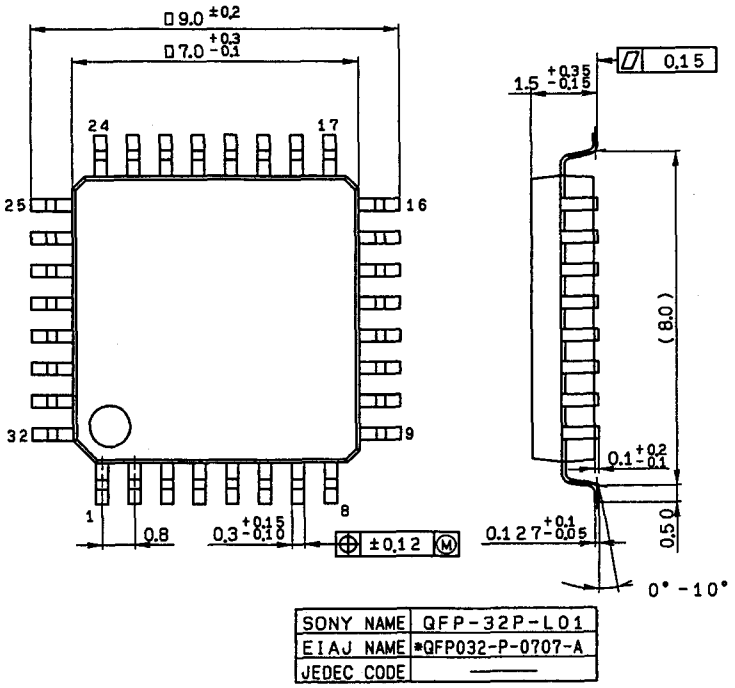
• SECAM



* COLB is output to BF/COLB OUT pin.
* S_{DR} and S_{DB} are formed in PLL using 908f_H.

Package Outline Unit : mm

32pin QFP (Plastic) 0.2g



SONY NAME	QFP-32P-L01
EIAJ NAME	*QFP032-P-0707-A
JEDEC CODE	———

SONY® CXD1035BQ-Z

CCD Camera Scanning System Timing Signal Generator

48pin QFP (Plastic)

Description

CXD1035BQ-Z is a CMOS type LSI developed for use with the scanning system of both ICX022AK (NTSC) and ICX024AK (PAL).

This IC is employed in conjunction with either CXD1030M or CXD1158M (synchronized signal generator).

Features

- Generates drive pulses for imagers (ICX022AK, ICX024AK).
- Generates signal processing pulse for color cameras.
- Switchover of NTSC/PAL modes is possible.
- Blemish compensation is possible (through usage of external ROM).

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta=25°C, Vss=0V)

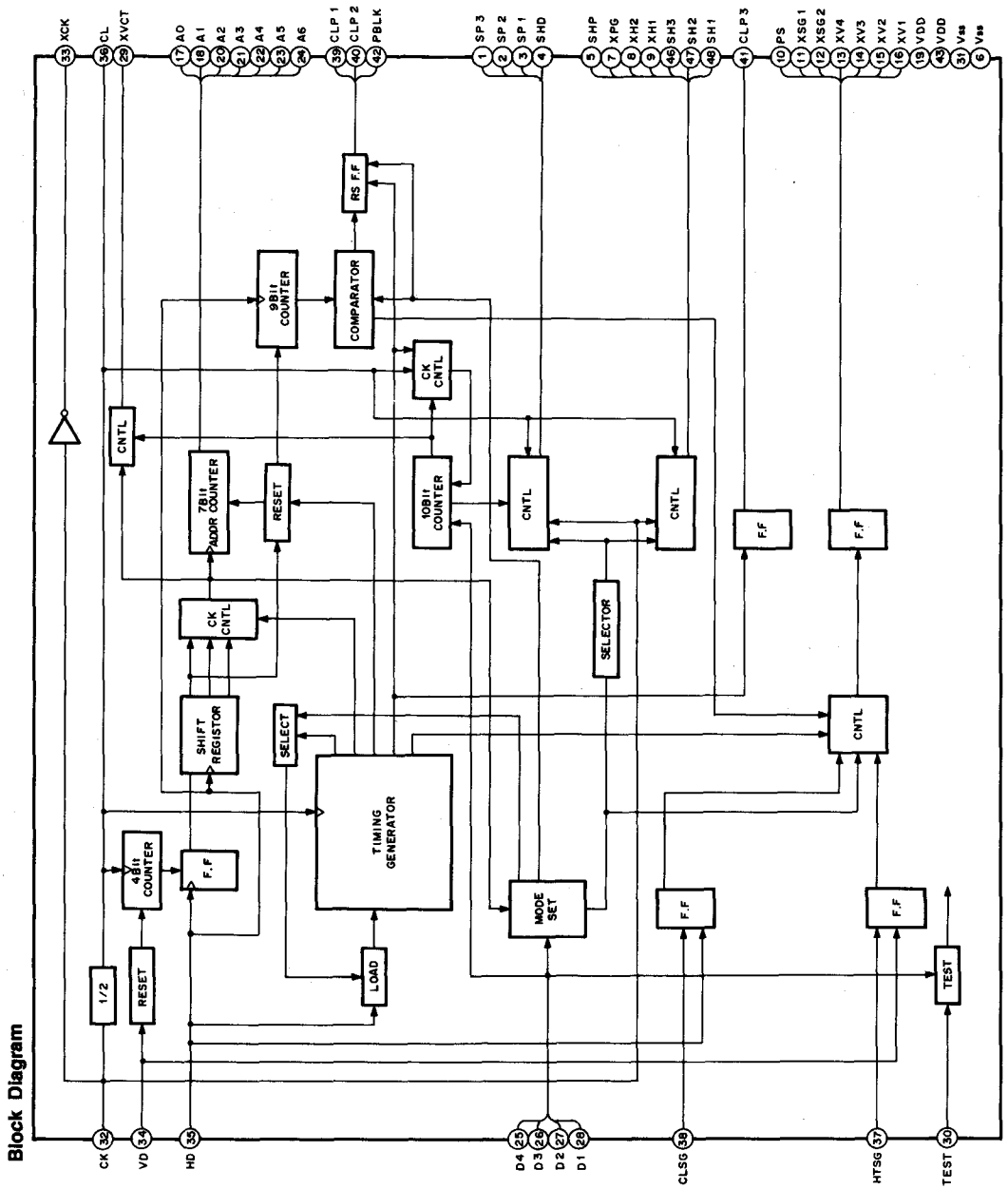
• Supply voltage	V_{DD}	$V_{SS}-0.5$	to	6.0	V
• Input voltage	V_I	$V_{SS}-0.5$	to	$V_{DD}+0.5$	V
• Output voltage	V_O	$V_{SS}-0.5$	to	V	V
• Operating temperature	Topr	−25	to	+85	°C
• Storage temperature	Tstg	−40	to	+125	°C
• Allowable power dissipation	P_D		500		mW

Recommended Operating Conditions

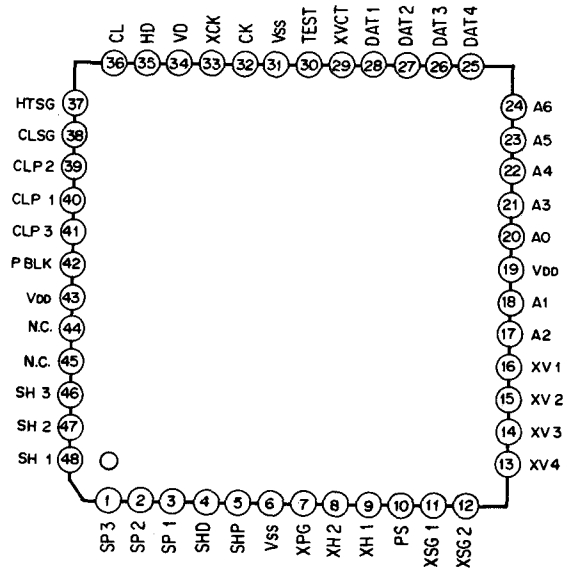
• Supply voltage	V_{DD}	4.75	to	5.25	V
• Operating temperature	Topr	−20	to	+75	°C

E89Z23-YA

Block Diagram



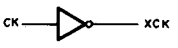
Pin Configuration (Top View)



Pin Name

No.	I/O	Symbol	No.	I/O	Symbol	No.	I/O	Symbol	No.	I/O	Symbol
1	O	SP3	13	O	XV4	25	I	DAT4	37	I	HTSG
2	O	SP2	14	O	XV3	26	I	DAT3	38	I	CLSG
3	O	SP1	15	O	XV2	27	I	DAT2	39	O	CLP2
4	O	SHD	16	O	XV1	28	I	DAT1	40	O	CLP1
5	O	SHP	17	O	A2	29	O	XVCT	41	O	CLP3
6	–	Vss	18	O	A1	30	I	TEST	42	O	PBLK
7	O	XPG	19	–	VDD	31	–	Vss	43	–	VDD
8	O	XH2	20	O	A0	32	I	CK	44	–	N.C.
9	O	XH1	21	O	A3	33	O	XCK	45	–	N.C.
10	O	PS	22	O	A4	34	I	VD	46	O	SH3
11	O	XSG1	23	O	A5	35	I	HD	47	O	SH2
12	O	XSG2	24	O	A6	36	O	CL	48	O	SH1

Pin Description

Symbol	I/O	Description
XV1 to XV4	O	Drive pulses for the imagers (ICX022, ICX024) through CCD drivers.
XSG1, 2	O	
XPG	O	
XH1, 2	O	
A0 to A6	O	Address output for external ROM. A6 is MSB.
D4 to D1	I	External ROM data input pin.
XVCT	O	ROM (MB7144) power supply switching pulse.
TEST	I	Test pin. Normally GND.
CK	I	Clock input. NTSC : 28.6364 MHz PAL : 28.3750 MHz
XCK	O	CK inversion output 
VD, HD	I	Synchronizing signal input. Latched by falling edge of CL (Pin 36).
CL	O	Clock output for synchronized signal generator. Half CK's frequency.
PBLK	O	Horizontal and vertical effective area of CCD imager output. Used for pre-blanking.
PS	O	Power save for V driver IC.
CLP1, 2, 3	O	Clamping pulse.
SH1, 2, 3	O	Sampling pulse for signal processor.
SP1, 2, 3	O	Sampling pulse for color separation.
SHD	O	Sampling pulse for imager output signal.
SHP	O	Sampling pulse for pre-charge level.
HTSG, CLSG	I	Test pin. Nomrally GND.
V_{SS}	I	Ground pin.
V_{DD}	I	+5V power supply pin.

Electrical Characteristics

DC characteristics

V_{DD}=5V±5%, V_{SS}=0V, Topr=20 to +75°C

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply current		I_{DDS}	Static state*	0		0.1	mA
Input voltage	H level	V_{OH}	I_{OH} = –0.4 mA	4.2		V_{DD}	V
	L level	V_{OL}	I_{OL} = 3.2 mA	V_{SS}		0.4	V
Output voltage	H level	V_{IH}		2.4			V
	L level	V_{IL}				0.8	V
Input leakage current		I_{LI}	V_I = 0V to V_{DD}	–10		+10	µA

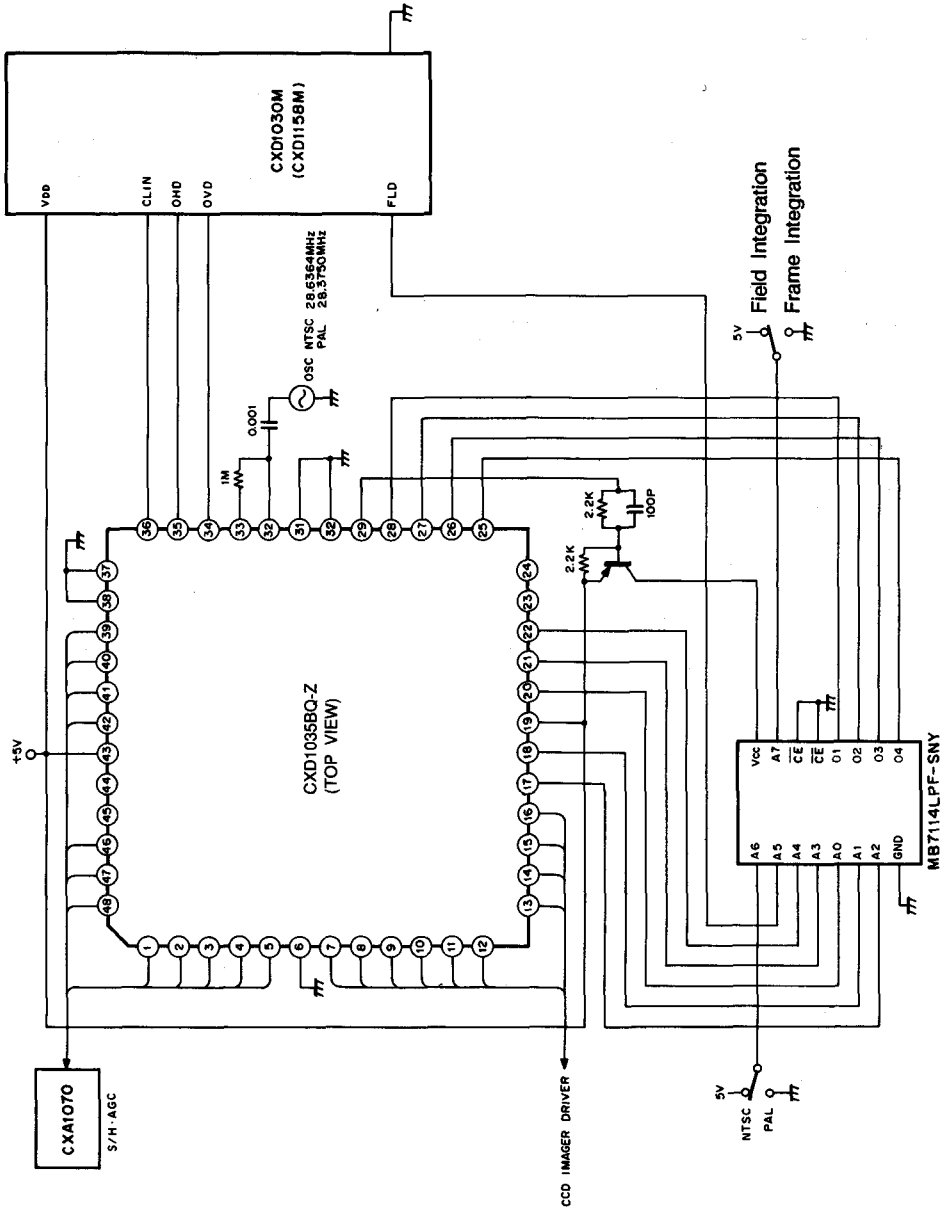
* **Note)** V_{IH} = V_{DD}, V_{IL} = V_{SS}

I/O characteristics

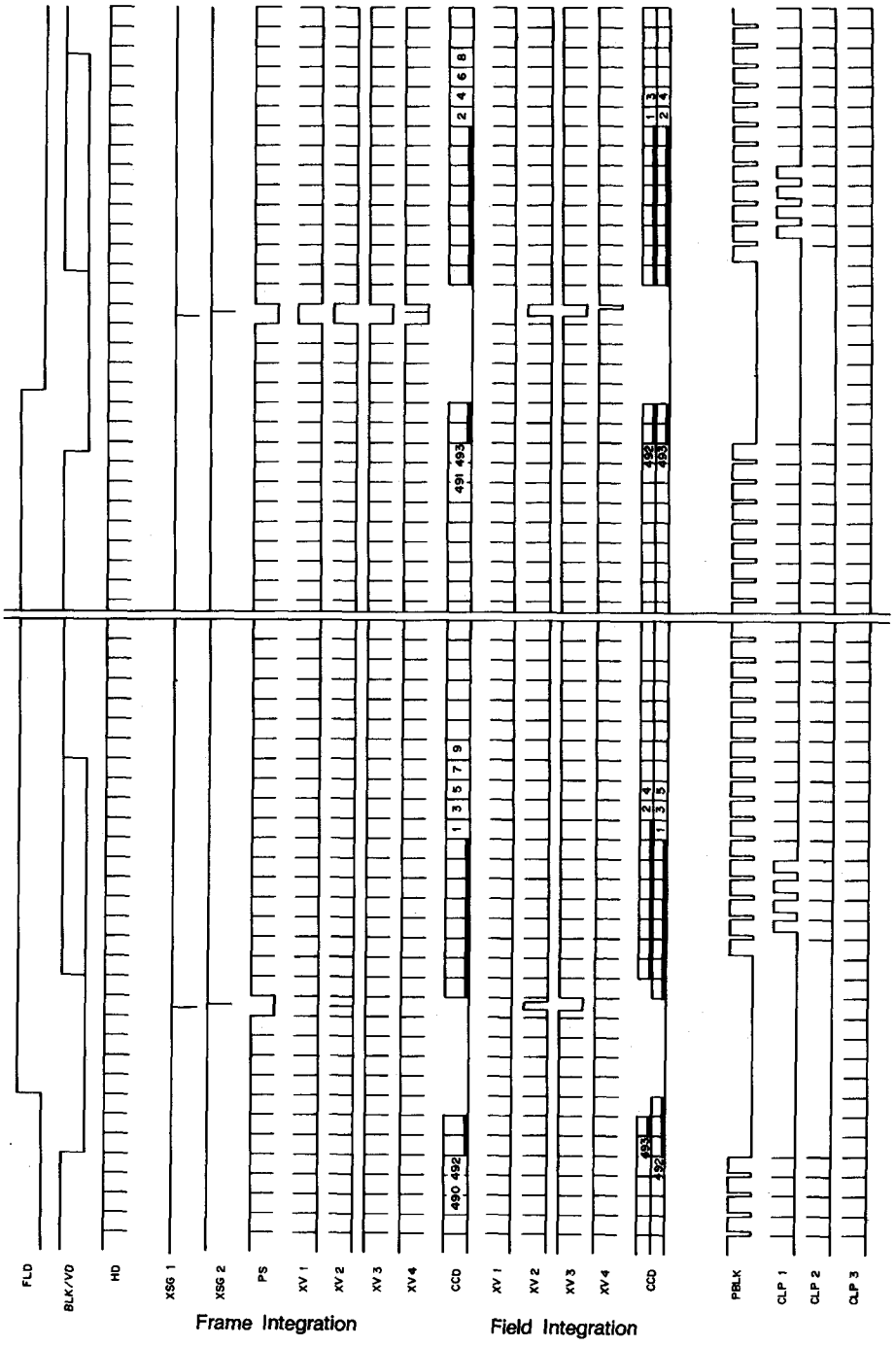
Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			9	pF
Output pin	C_{OUT}			9	pF

Test condition: V_{DD}=V_I=0V, f_M=1MHz

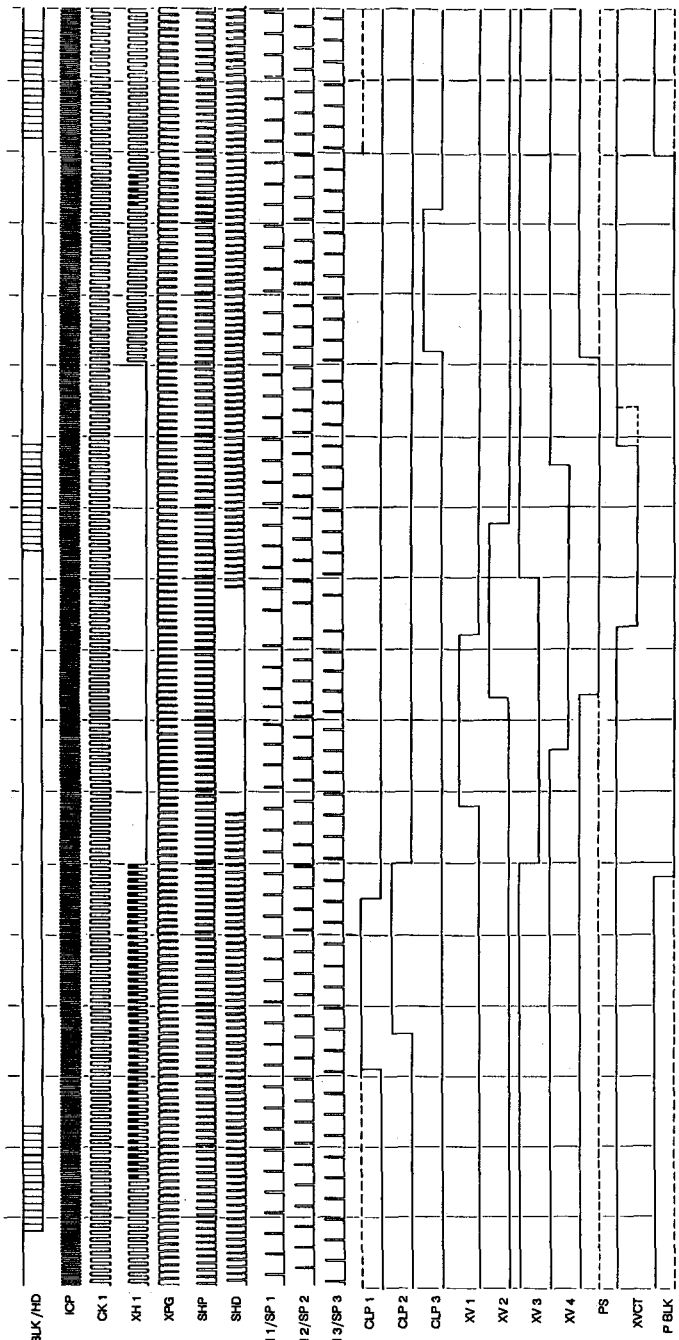
Application Circuit



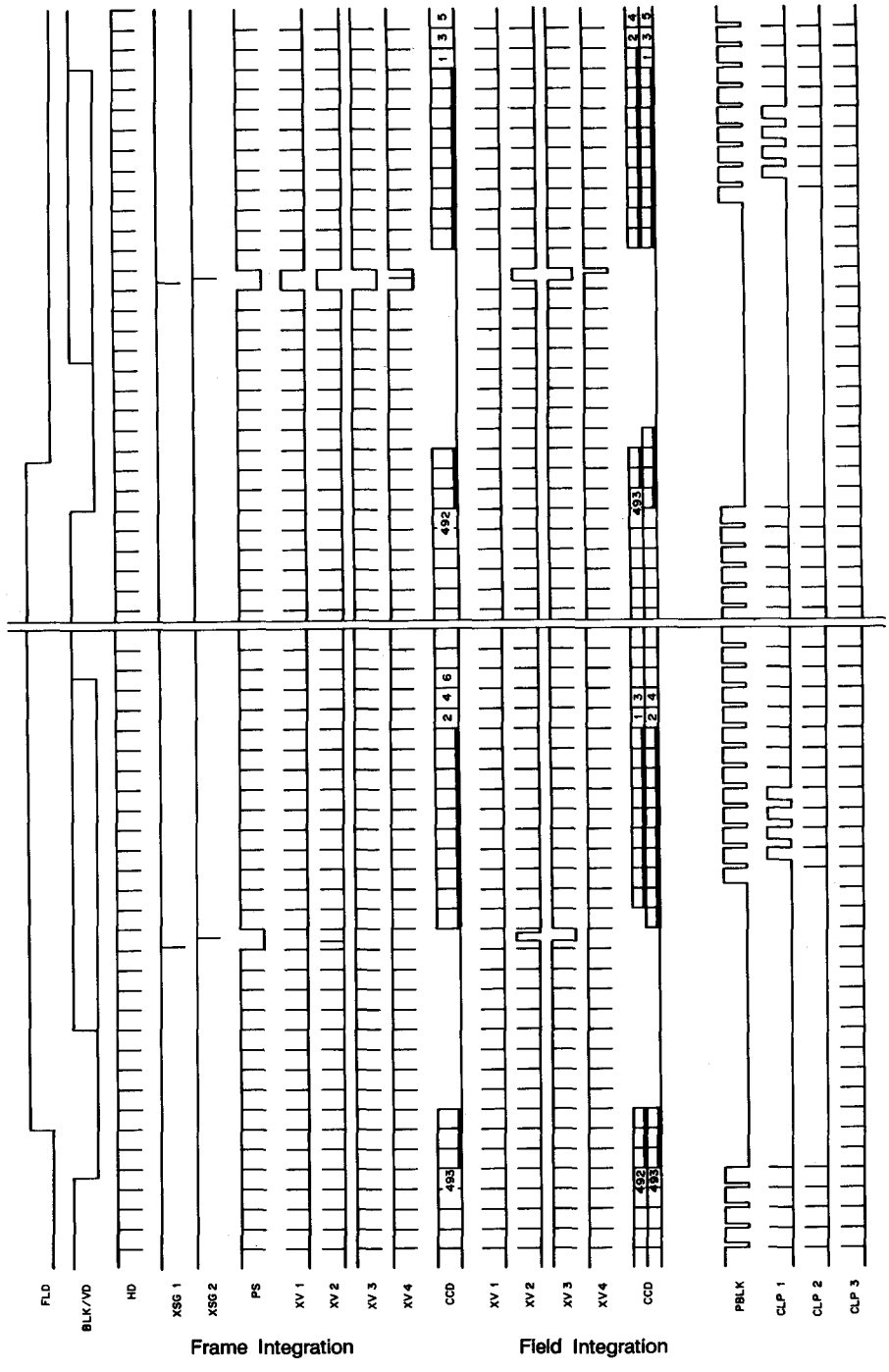
NTSC V Direction



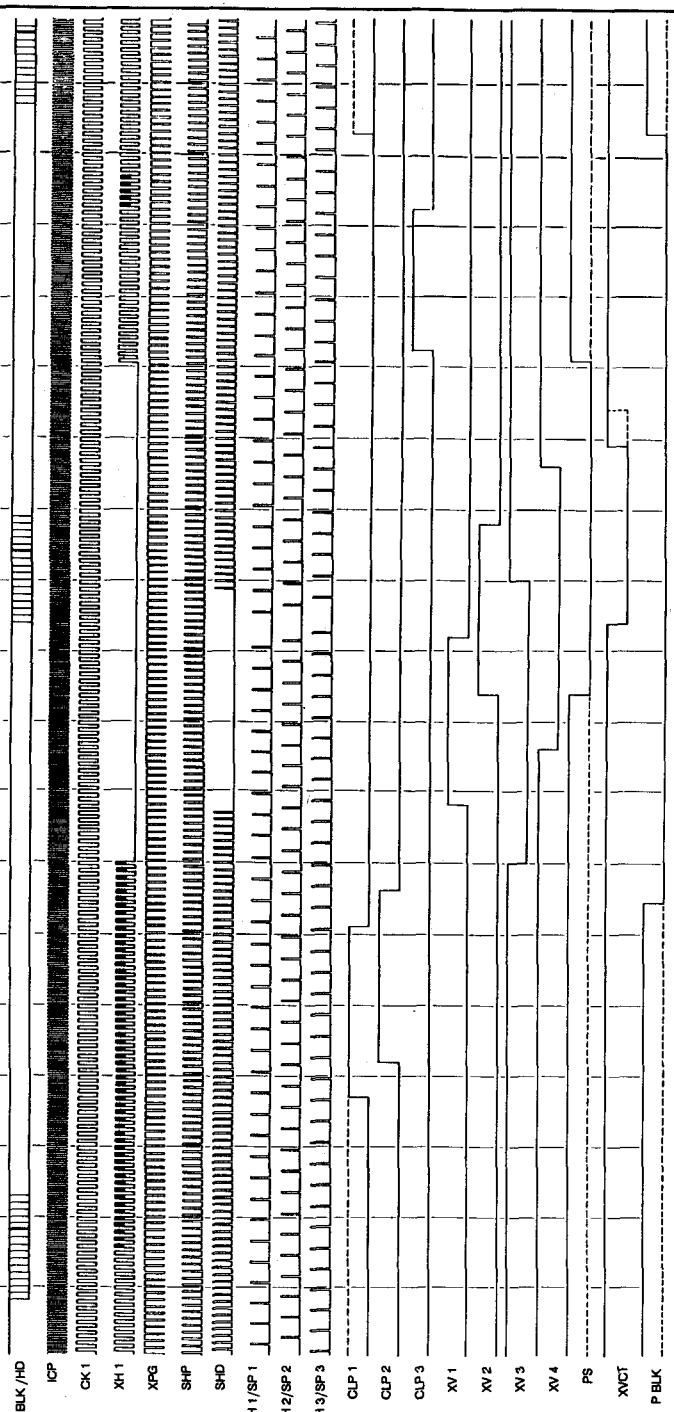
NTSC H Direction



PAL V Direction

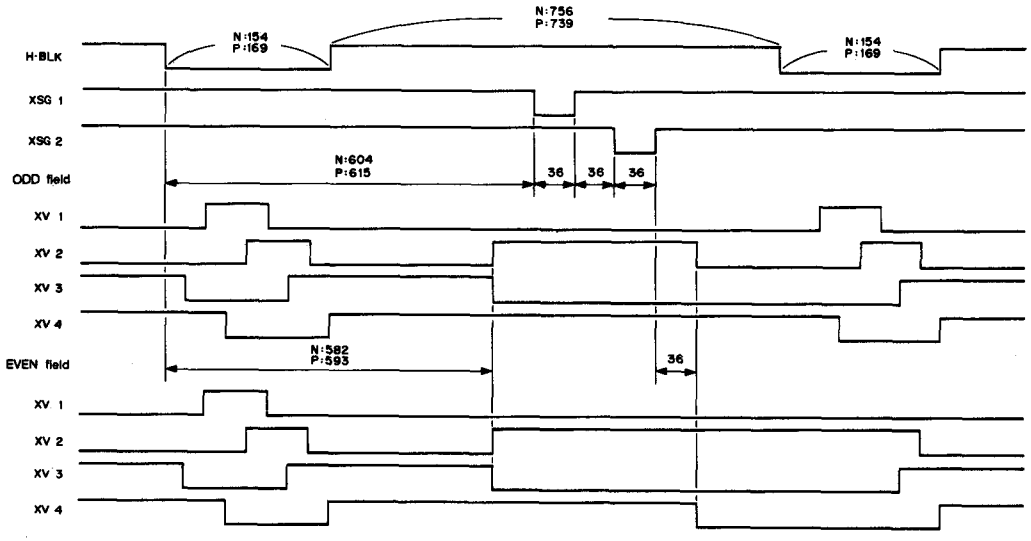


PAL H Direction

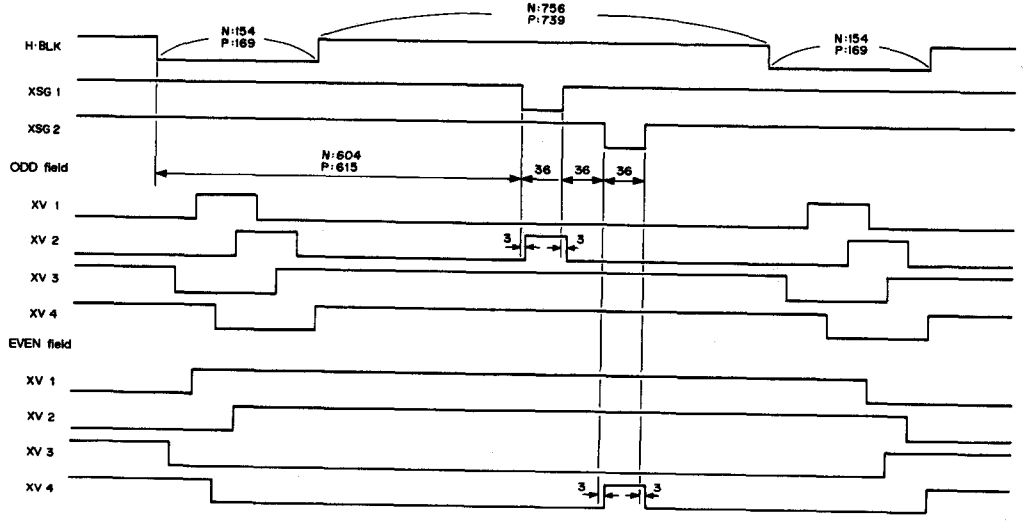


Readout Period

Field Integration mode



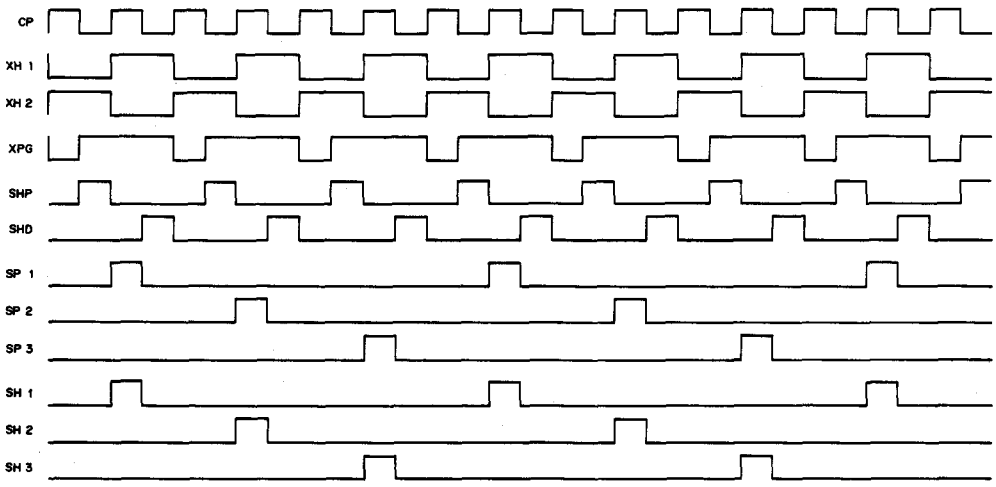
Frame Integration mode



Note) Number: Clock (1 clock = 70ns)

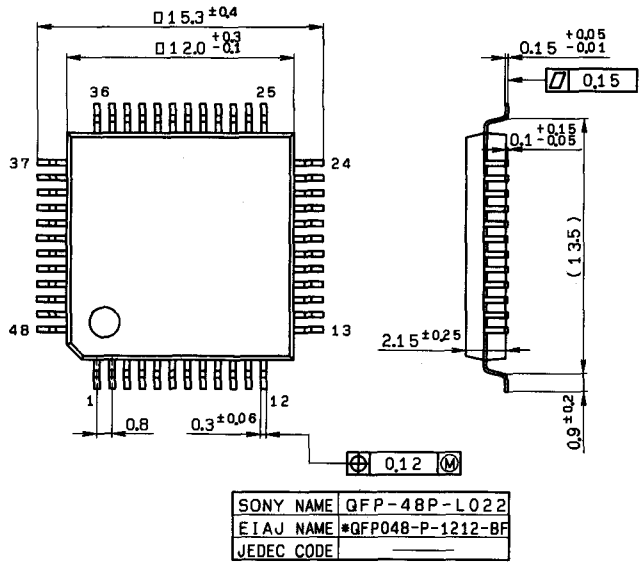
N:NTSC
P:PAL

H clock • Signal Processing Pulse Phase



Package Outline Unit: mm

48pin QFP (Plastic) 0.7g



SONY NAME	QFP-48P-L022
EIAJ NAME	*QFP048-P-1212-BF
JEDEC CODE	———

SONY CXD1149Q/R

Timing Signal Generator for Scanning Systems of CCD Cameras (For ICX022AN/024AN)

Description

The CXD1149Q/R is a CMOS LSI chip designed for use in the scanning system for the ICX022AN (NTSC)/ICX024AN (PAL) image sensor. Use this chip in combination with the CXD1030M/ CXD1158M synchronizing signal generator.

CXD1149R
48pin VQFP (Plastic)

CXD1149Q
48pin QFP (Plastic)

Features

- Generation of pulses for driving the ICX022AN/ ICX024AN image sensor
- Generation of pulses for processing checkered coding signals
- Switchable between NTSC and PAL modes
- Electronic shutter control function
- Built-in clock oscillation inverter

Applications

- CCD color cameras (NTSC/PAL)

Absolute Maximum Ratings (Ta=25°C, V_{SS}=0 V)

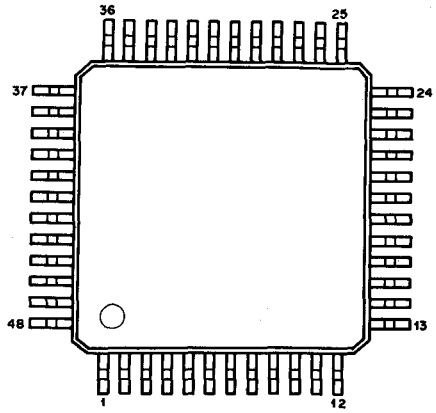
• Storage temperature	T_{stg}	−55 to +150	°C
• Ambient temperature	T_{opr}	−20 to +75	°C
• Supply voltage	V_{CC}	(V_{SS}−0.5) to +7.0	V
• Input voltage	V_I	(V_{SS}−0.5) to (V_{DD}+0.5)	V
• Output voltage	V_O	(V_{SS}−0.5) to (V_{DD}+0.5)	V

Recommended Operating Condition

• Supply voltage	V_{CC}	+4.75 to +5.25	V

E89190-HP

Pin Configuration (Top View)

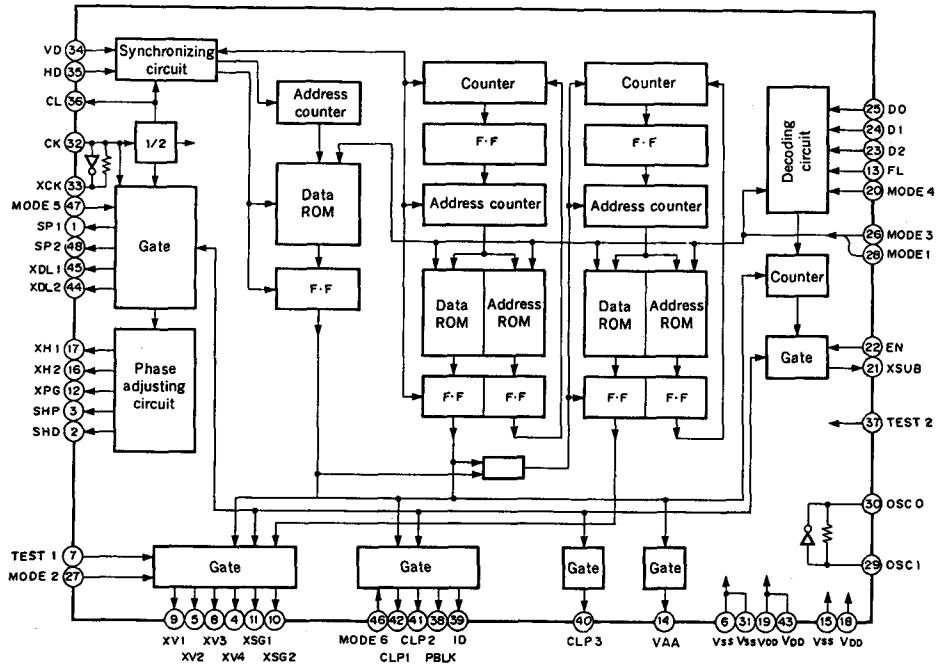


Pin Description

Pin No.	Symbol	I/O	Description
1	SP1	O	Color separation S/H pulse
2	SHD	O	CCD data output S/H pulse
3	SHP	O	CCD precharge level S/H pulse
4	XV4	O	Clock pulse for V register
5	XV2	O	Clock pulse for V register
6	V_{SS}	—	GND
7	TEST1	I	GND, pull-down
8	XV3	O	Clock pulse for V register
9	XV1	O	Clock pulse for V register
10	XSG2	O	Sensor charge readout pulse
11	XSG1	O	Sensor charge readout pulse
12	XPG	O	CCD output reset pulse
13	FL	I	Electronic shutter flickerless, Low: Flickerless, High: Normal, pull-up
14	VAA	O	Vertical blanking cleaning pulse
15	V_{SS}	—	GND
16	XH2	O	Clock pulse for H register
17	XH1	O	Clock pulse for H register
18, 19	V_{DD}	—	Power supply
20	MODE4	I	Electronic shutter speed input switch, Low: Serial input, High: Parallel input, pull-up
21	XSUB	O	Sensor charge sweep-out pulse
22	EN	I	Electronic shutter on/off, Low: Off, High: On, pull-up

Pin No.	Symbol	I/O	Description
23	D2	I	Electronic shutter speed switching input, pull-up
24	D1	I	Electronic shutter speed switching input, pull-up
25	D0	I	Electronic shutter speed switching input, pull-up
26	MODE3	I	NTSC/PAL switching, Low: NTSC, High: PAL, pull-down
27	MODE2	I	Frame/field switching, High: Frame, Low: Field, pull-down
28	MODE1	I	GND, pull-down
29	OSCI	I	Input to oscillation inverter
30	OSCO	O	Output to oscillation inverter
31	V_{SS}	—	GND
32	CK	I	Input to duty-control inverter
33	XCK	O	Output to duty-control inverter
34	VD	I	Vertical synchronizing signal input
35	HD	I	Horizontal synchronizing signal input
36	CL	O	Clock output for sync generator
37	TEST2	I	GND, pull-down
38	PBLK	O	Pre-blanking pulse
39	ID	O	Line identifying pulse
40	CLP3	O	Clamp pulse
41	CLP2	O	Clamp pulse
42	CLP1	O	Clamp pulse
43	V_{DD}	—	Power supply
44	XDL2	O	Clock pulse for delay line
45	XDL1	O	Clock pulse for delay line
46	MODE6	I	PBLK control pulse, Low: Narrow, High: Wide, pull-down
47	MODE5	I	GND, pull-down
48	SP2	O	Color separation S/H pulse

Block Diagram and Pin Configuration



Electrical Characteristics

DC Characteristics $V_{DD}=5V\pm5\%$, $V_{SS}=0V$, $T_{opr}=-20$ to $+75°C$

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage	High level	V_{IH}		$0.7V_{DD}$			V
	Low level	V_{IL}				$0.3V_{DD}$	V
Input voltage (FL, EN, D0 to D2) *Schmitt trigger	High level	V_{T+}		$0.8V_{DD}$			V
	Low level	V_{T-}				$0.2V_{DD}$	V
	Hysteresis	$V_{T+}-V_{T-}$		0.7	0.9		V
Output voltage	High level	V_{OH}	$I_{OH}=-2mA$	$V_{DD}-0.5$			V
	Low level	V_{OL}	$I_{OL}=4mA$			0.4	V
Output voltage (oscillation cell) (OSCO, XCK)	High level	V_{OH}	$I_{OH}=-1mA$	$V_{DD}/2$			V
	Low level	V_{OL}	$I_{OL}=1mA$			$V_{DD}/2$	V
Input leak current			$V_I=0V\sim V_{DD}$	−10		10	μA
Oscillation cell feedback resistance		R_{FB}		500K	2M	5M	Ω

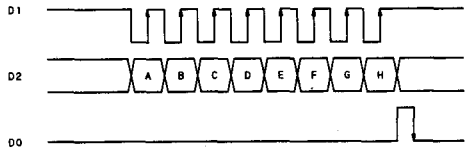
Input/Output Capacitance

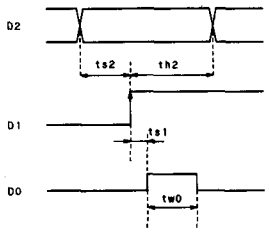
Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			9	PF
Output pin	C_{OUT}			11	PF

Test conditions: $V_{DD}=V_I=0V$, f=1MHz

AC Characteristics

During serial input mode





Symbol	Item	MIN
t_s2	D2 setup time for the rise of D1	20ns
t_h2	D2 hold time for the rise of D1	20ns
t_s1	D1 rise setup time for the rise of D0	20ns
t_w0	D0 pulse width	20ns

Description of Operation

The CXD1149Q/R is provided with input pins which enable various modes to be set. They are previously pulled up or down internally, so that even when the input pins are left open, the modes are preset. (The pull-up/pull-down resistance is about 100kΩ.)

Pin name	Pin No.	Preset value	Function	
			When input=High	When input=Low
MODE2	27	L	FRM	FLD
MODE3	26	L	PAL	NTSC
MODE4	20	H	(Electronic shutter speed input format)	
			Parallel input	Serial input
MODE5	47	L	TEST pin (Normally Low)	
MODE6	46	L	(PBLK control pulse width switching)	
			Wide	Narrow
EN	22	H	Electronic shutter ON	OFF
FL	13	H	Electronic shutter normal	Electronic shutter flickerless
D2	23	H	Electronic shutter speed control (Details to be described later.)	
D1	24	H		
D0	25	H		

The operation state is presented in the attached timing charts as listed below:

- NTSC Vertical timing chart
- PAL Vertical timing chart
- NTSC Horizontal timing chart
- PAL Horizontal timing chart

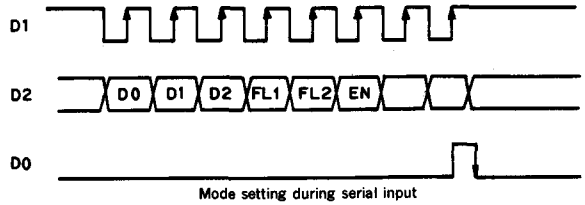
• Electronic Shutter Speed Control

	External pin							Internal register								Shutter speed XSUB㉑
	P/S	EN	CRNT	FL	D2	D1	D0			EN	FL2	FL1	D2	D1	D0	
	↑⑳	↑㉒	↓㉖	↑⑬	↑㉓	↑㉔	↑㉕	D7	D6	D5	D4	D3	D2	D1	D0	
Parallel mode P/S=H	H	H		H	L	L	L									NORMAL
	H	H		H	L	L	H									1/125
	H	H		H	L	H	L									1/250
	H	H		H	L	H	H									1/500
	H	H		H	H	L	L									1/1000
	H	H		H	H	L	H									1/2000
	H	H		H	H	H	L									1/4000
	H	H		H	H	H	H									1/10000
	H	H	L	L												1/100
	H	H	H	L												1/120
	H	L														H
Serial mode P/S=L FL=H EN=H	L	H		H						H		H	L	L	L	NORMAL
	L	H		H						H		H	L	L	H	1/125
	L	H		H						H		H	L	H	L	1/250
	L	H		H						H		H	L	H	H	1/500
	L	H		H						H		H	H	L	L	1/1000
	L	H		H						H		H	H	L	H	1/2000
	L	H		H						H		H	H	H	L	1/4000
	L	H		H						H		H	H	H	H	1/10000
	L	H	H	H						H	H	L				1/100
	L	H	H	H						H	H	L				1/120
	L	H	L	H						H	H	L				1/100
	L	H	L	H						H	L	L				1/120
	L	H		H						L						H
Serial mode parallel CTL P/S=L	L	H	L	L												1/100
	L	H	H	L												1/120
	L	L														H

MODE 3 CR/NT
MODE 4 P/S

Symbols used: P: Parallel input, S: Serial input
CR: PAL, NT: NTSC

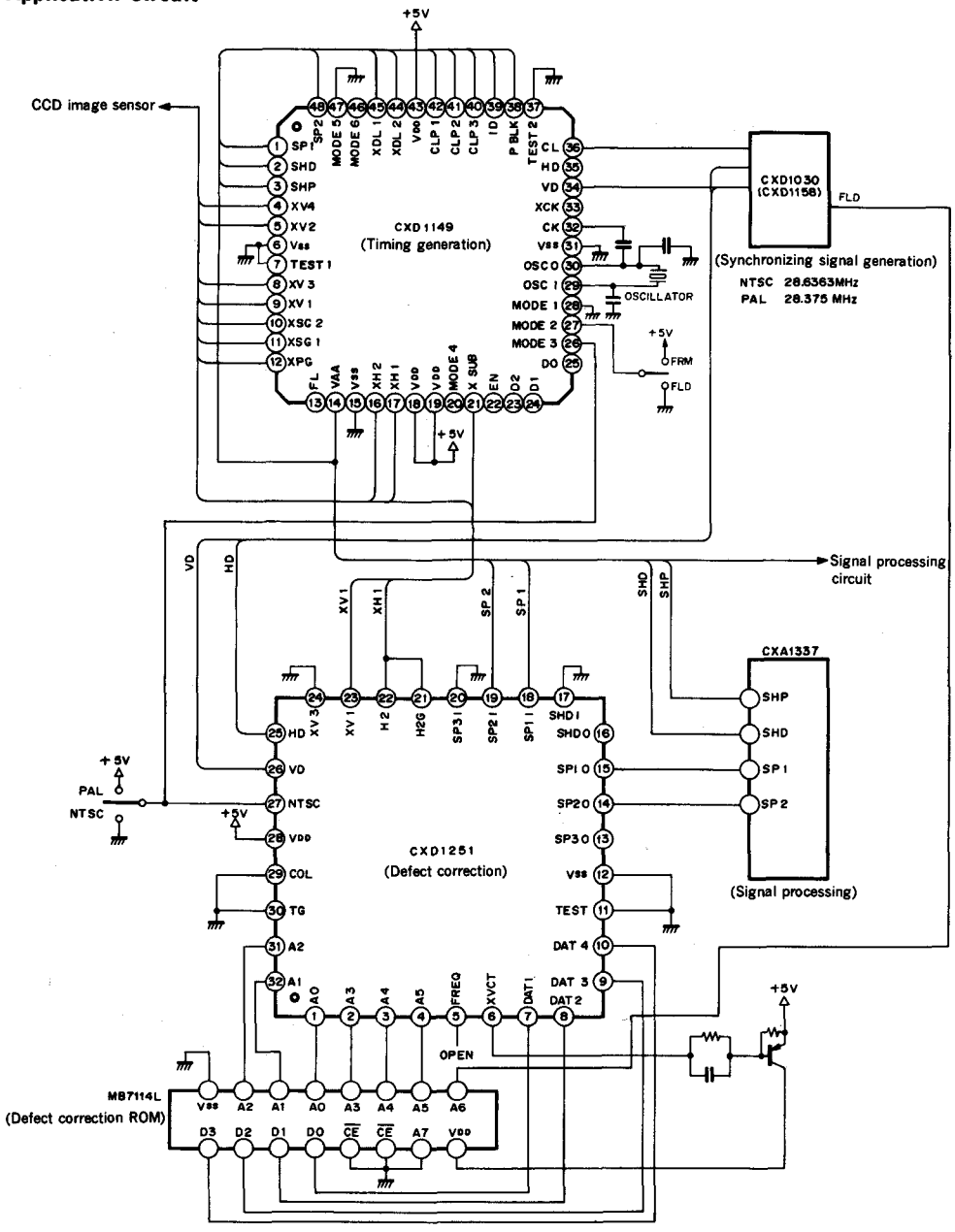
Note) When serial input is used (MODE 4=Low)



Mode setting during serial input

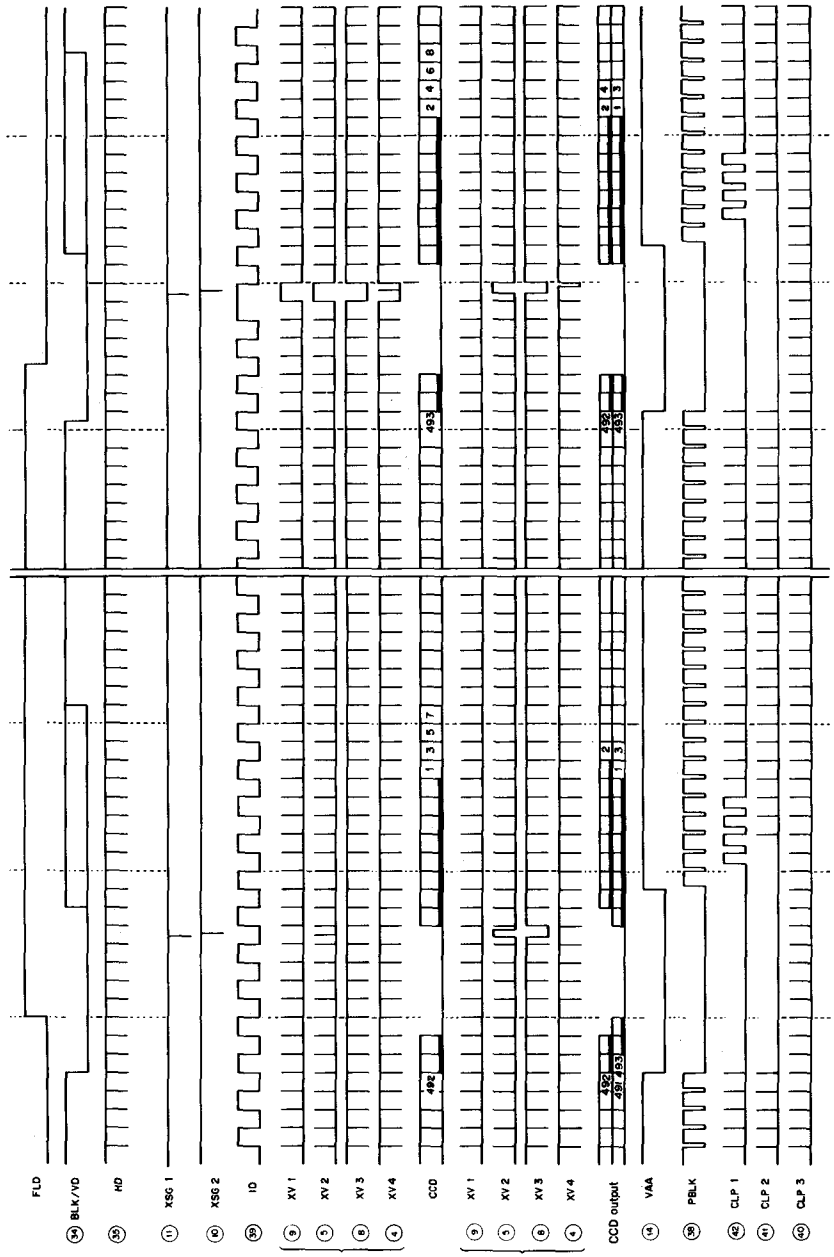
The D2 data is latched in a register at the rise ⌐ of D1 and read in at the fall ¬ of D0.
It is then used to control the shutter speed, as described in the above table.

Application Circuit

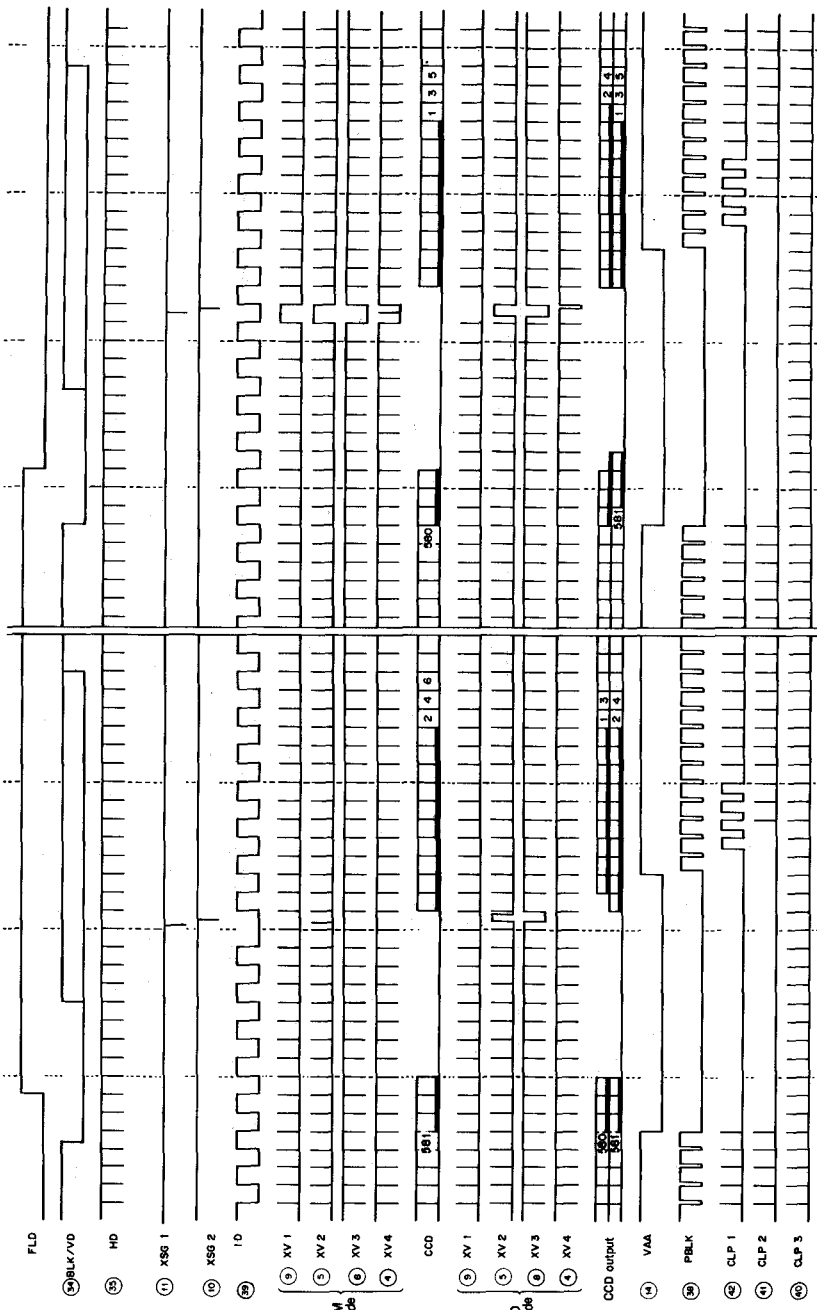


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

NTSC Vertical Timing Chart

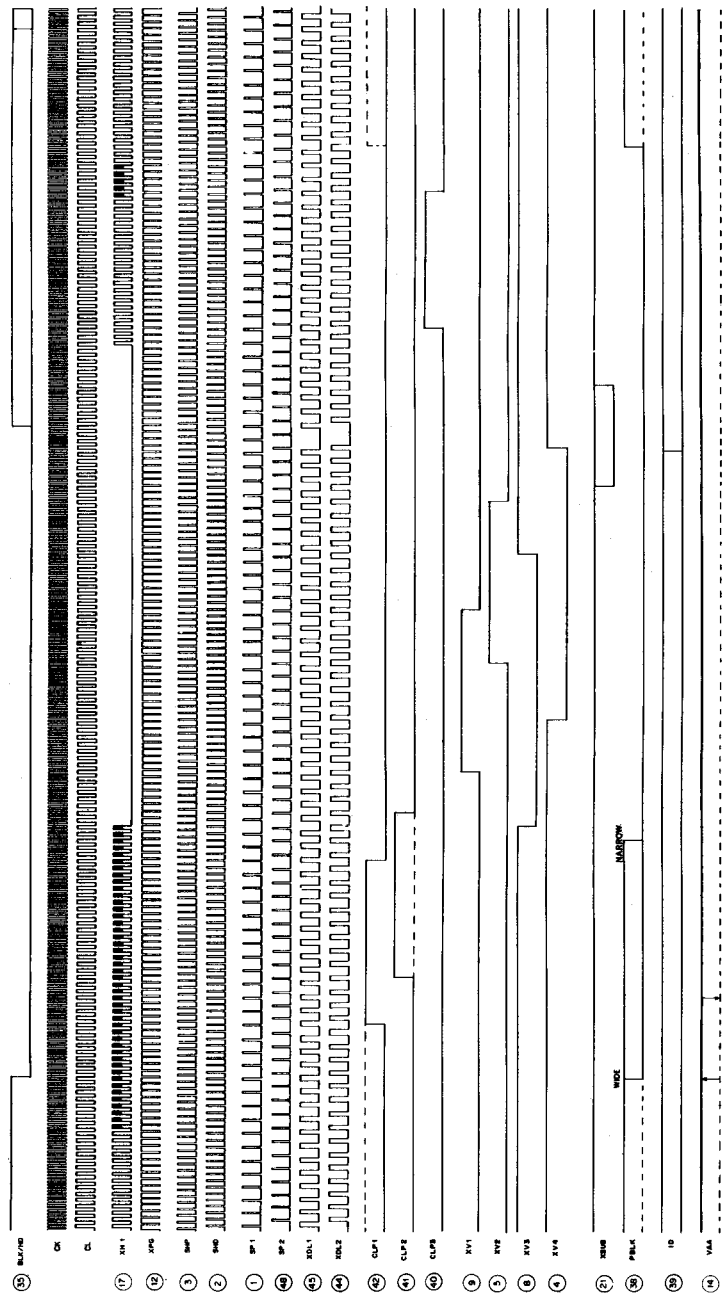


PAL Vertical Timing Chart



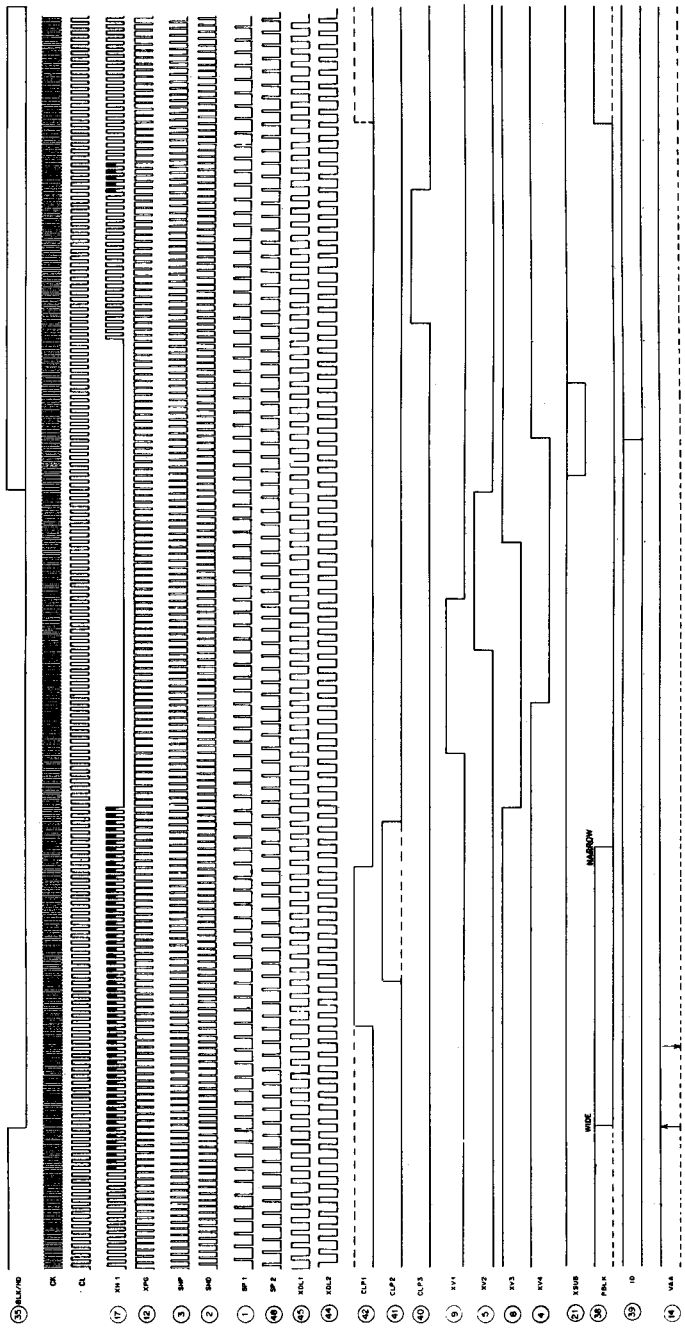
NTSC Horizontal Timing Chart

*VAA (↑ : Follows HD, ↓ : Follows VD)

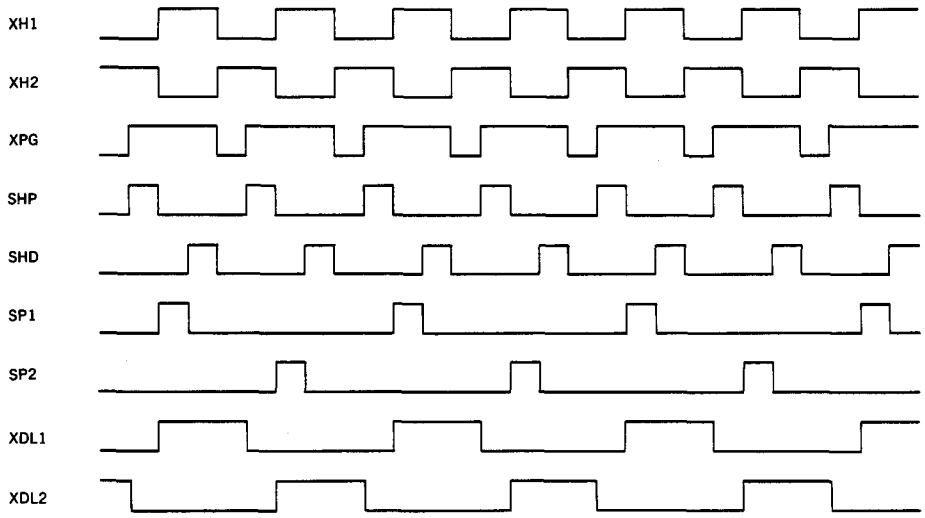


PAL Horizontal Timing Chart

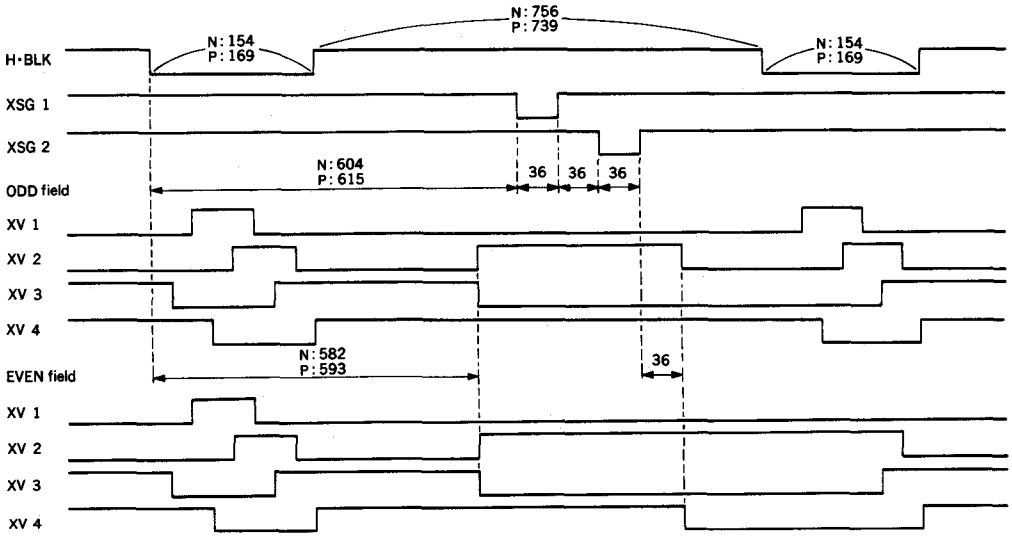
*VAA (↑ : Follows HD, ↓ : Follows VD)



Phase Relationship between H Clock and Signal Processing Pulses



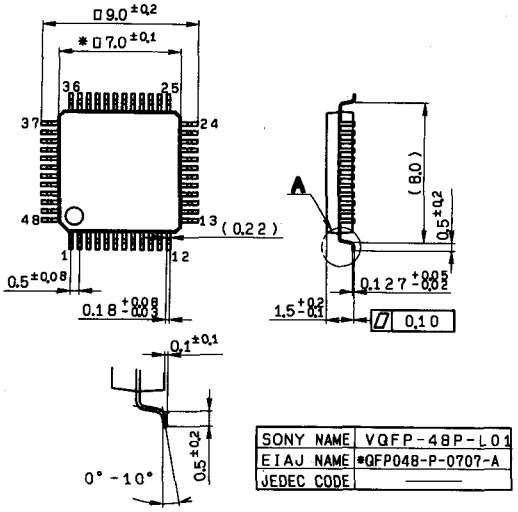
Readout Period Details



Package Outline **Unit : mm**

CXD1149R

48pin VQFP (Plastic) 0.2g

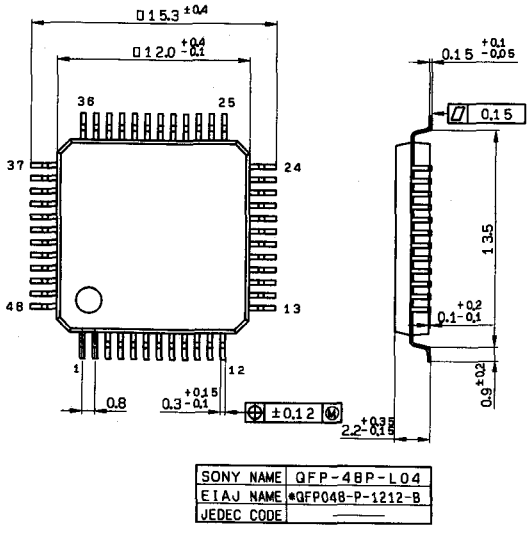


Detailed diagram of A

Note) Dimensions marked with * does not include resin residue.

CXD1149Q

48pin QFP (Plastic) 0.7g



SONY®

CXD1156Q/R

Timing Generator IC for ICX026/027

Description

CXD1156Q/R is a timing generator IC for CCD imagers ICX026AK/AL and ICX027AK/AL.

48pin QFP (Plastic)

48pin VQFP (Plastic)

Features

- NTSC/CCIR
- Field accumulation mode
- Color/Black and White mode
- 1/60 to 1/10,000 sec. variable speed, built-in electronic shutter.
- Built-in horizontal driver.
- Initialize operation at every field.

Functions

Timing generation for CCD imagers.

Structure

Silicon gate CMOS

Application

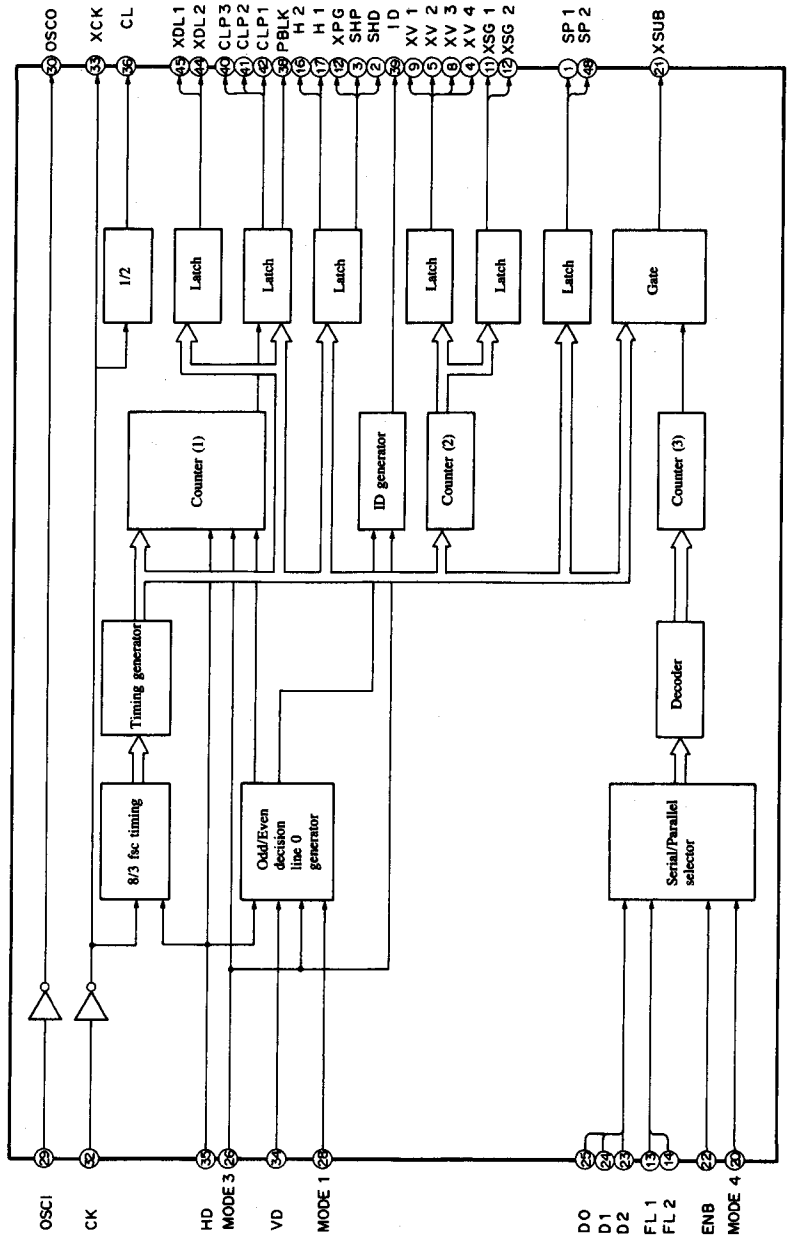
CCD camera system

Absolute Maximum Ratings (Ta = 25°C, Vss = 0V)

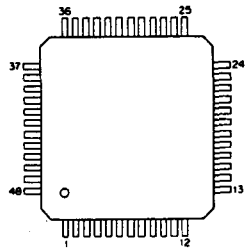
• Supply voltage	V_{DD}	$V_{SS}-0.5$ to $+7.0$	V
• Input voltage	V_I	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
• Output voltage	V_O	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
• Operating temperature	T_{opr}	-20 to $+75$	°C
• Storage temperature	T_{stg}	-55 to $+150$	°C

E89X12-YA

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	SP1	O	Color separation pulse ('L' in B/W mode)
2	SHD	O	Data sample hold pulse
3	SHP	O	Precharge level sample hold pulse
4	XV4	O	Vertical scanning clock
5	XV2	O	Vertical scanning clock
6	Vss	–	GND
7	TEST1	I	GND
8	XV3	O	Vertical scanning clock
9	XV1	O	Vertical scanning clock
10	XSG2	O	Sensor charge read out pulse
11	XSG1	O	Sensor charge read out pulse
12	XPG	O	Precharge gate pulse
13	FL1	I	Mode select L: Flicker less H: Normal, (pull up)
14	FL2	I	Mode select L: 60Hz H: 50Hz, (pull up)
15	Vss2	–	GND for driver
16	H2	O	Horizontal scanning clock
17	H1	O	Horizontal scanning clock
18	VDD2	–	+5V supply pin for driver
19	VDD	–	+5V
20	MODE4	I	Mode select L: Serial input H: Parallel input, (pull up)
21	XSUB	O	Discharge pulse
22	ENB	I	Enable signal L: Normal H: Electronic shutter (pull up)
23	D2	I	Shutter speed setting (schmitt input), (pull up)
24	D1	I	Shutter speed setting (schmitt input), (pull up)
25	D0	I	Shutter speed setting (schmitt input), (pull up)
26	MODE3	I	Mode select L: NTSC H: PAL., (pull down)
27	TEST2	I	GND
28	MODE1	I	Mode select L: Color H:B/W, (pull down)
29	OSCI	I	Ocsillation input oscillation frequency. NTSC: 28.6364 MHz CCIR: 28.3750 MHz
30	OSCO	O	Oscillation output
31	Vss	–	GND
32	CK	I	Duty control inverter input
33	XCK	O	Duty control inverter output

No.	Symbol	I/O	Description
34	VD	I	Vertical drive pulse
35	HD	I	Horizontal drive pulse
36	CL	O	4 fsc clock output (Sync generator clock input)
37	TEST0	I	GND
38	PBLK	O	Blanking cleaning pulse
39	ID	O	Line discrimination pulse
40	CLP3	O	Clamp pulse
41	CLP2	O	Clamp pulse
42	CLP1	O	Clamp pulse
43	V_{DD}	–	+5V
44	XDL2	O	Delay line pulse ('L' in B/W mode)
45	XDL1	O	Delay line pulse ('L' in B/W mode)
46	TEST3	I	GND
47	TEST4	I	GND
48	SP2	O	Color separation pulse ('L' in B/W mode)

Recommended Operating Conditions

Electrical characteristics (DC characteristics)

Item		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		V_{DD}	4.75	5.0	5.25	V
I/O voltage		V_I, V_O	V_{SS}		V_{DD}	V
Input voltage (Logical value) CMOS input cell		V_{IH}	0.7V_{DD}			V
		V_{IL}			0.3V_{DD}	
Schmitt trigger input voltage (D0, D1, D2)		V_{T+}	0.8V_{DD}			V
		V_{T-}			0.2V_{DD}	
		$V_{T+}-V_{T-}$	0.7	0.9		
Input rising, falling time		tr,tf	0		500	ns
Operating temperature		Ta	−20		+75	°C
Output voltage 1	I_{OH} = −2mA	V_{OH1}	*3			V
	I_{OL} = 4mA	V_{OL1}			0.4	V
*1 Output voltage 2	I_{OH} = −4mA	V_{OH2}	*3			V
	I_{OL} = 8mA	V_{OL2}			0.4	V
*2 Output voltage 3	I_{OH} = −8mA	V_{OH3}	*3			V
	I_{OL} = 8mA	V_{OL3}			0.4	V

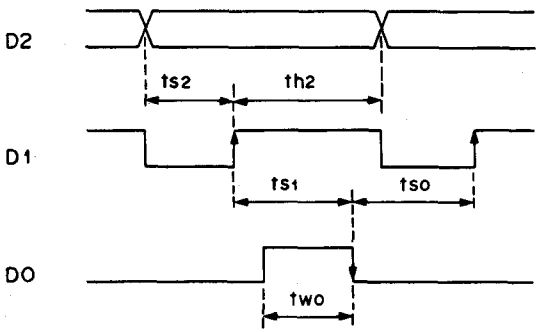
*1. Pin 12 (XPG).
*2. Pins 16 and 17 (H1,H2)
*3. V_{DD}−0.5

Oscillation I/O Electrical Characteristics (OSCI, OSCO, CK, XCK)

Item		Symbol	Min.	Typ.	Max.	Unit
Logical threshold value		V_{th}		$V_{DD}/2$		V
Input voltage		V_{IH}	0.7V_{DD}			V
		V_{IL}			0.3V_{DD}	V
Feedback resistor	V_{IN} = V_{SS} or V_{DD}	R_{FB}	500k	2M	5M	Ω
Output voltage	I_{OH} = −1mA	V_{OH}	$V_{DD}/2$			V
	I_{OL} = 1mA	V_{OL}			$V_{DD}/2$	V

AC Characteristics

Serial input mode



Symbol	Item	MIN.	MAX.
ts2	D2 set up time vs. D1 rising edge	20nS	—
th2	D2 hold time vs. D1 rising edge	20nS	—
ts1	D1 rising edge set up time vs. D0 falling edge	20nS	—
tw0	D0 pulse width	20nS	50μS
ts0	D0 falling edge set up time vs. D1 rising edge	20nS	—

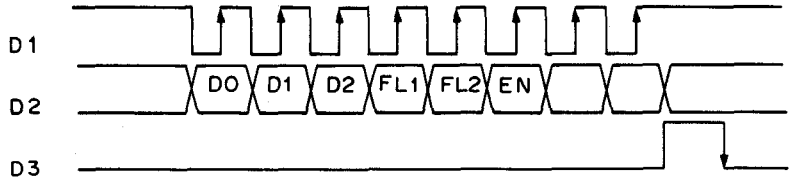
Mode Setting

1. Parallel input (mode 4 = 'H')

Table-1

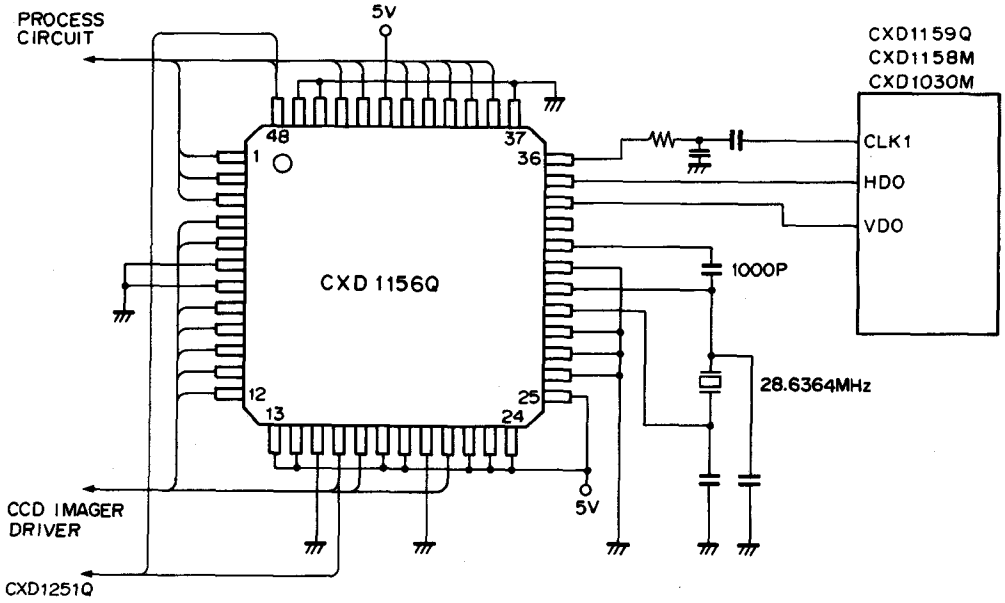
ENB	MODE 3	MODE 4	FL1	FL2	D2	D1	D0	Shutter speed
H	L	H	H		L	L	L	1/60
H	L	H	H		L	L	H	1/125
H	L	H	H		L	H	L	1/250
H	L	H	H		L	H	H	1/500
H	L	H	H		H	L	L	1/1000
H	L	H	H		H	L	H	1/2000
H	L	H	H		H	H	L	1/4000
H	L	H	H		H	H	H	1/10000
H	H	H	H		L	L	L	1/60
H	H	H	H		L	L	H	1/125
H	H	H	H		L	H	L	1/250
H	H	H	H		L	H	H	1/500
H	H	H	H		H	L	L	1/1000
H	H	H	H		H	L	H	1/2000
H	H	H	H		H	H	L	1/4000
H	H	H	H		H	H	H	1/10000
H	L		L	H				1/100
H	L		L	L				1/120
H	H		L	H				1/100
H	H		L	L				1/120
L								NORMAL

2. Serial input mode (mode 4 = 'L')



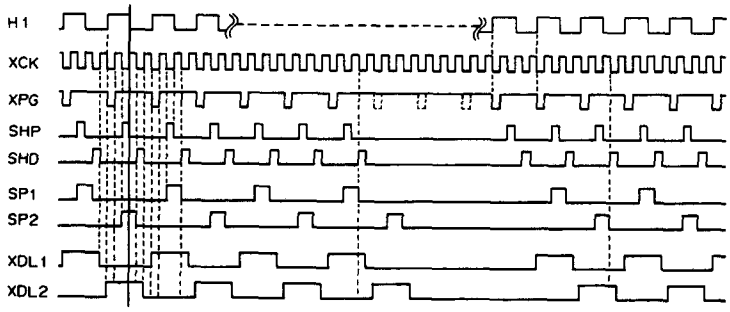
D2 data is latched by the register with the rising edge of D1, and taken inside with the falling edge of D0.

Application Circuit (NTSC mode, color mode)

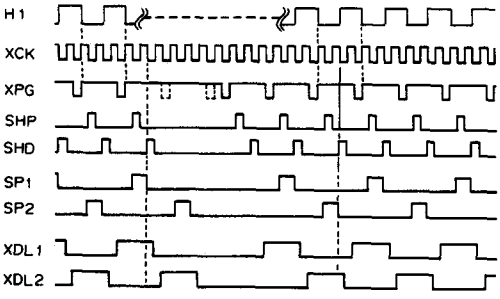


Timing Chart 1. [High speed timing]

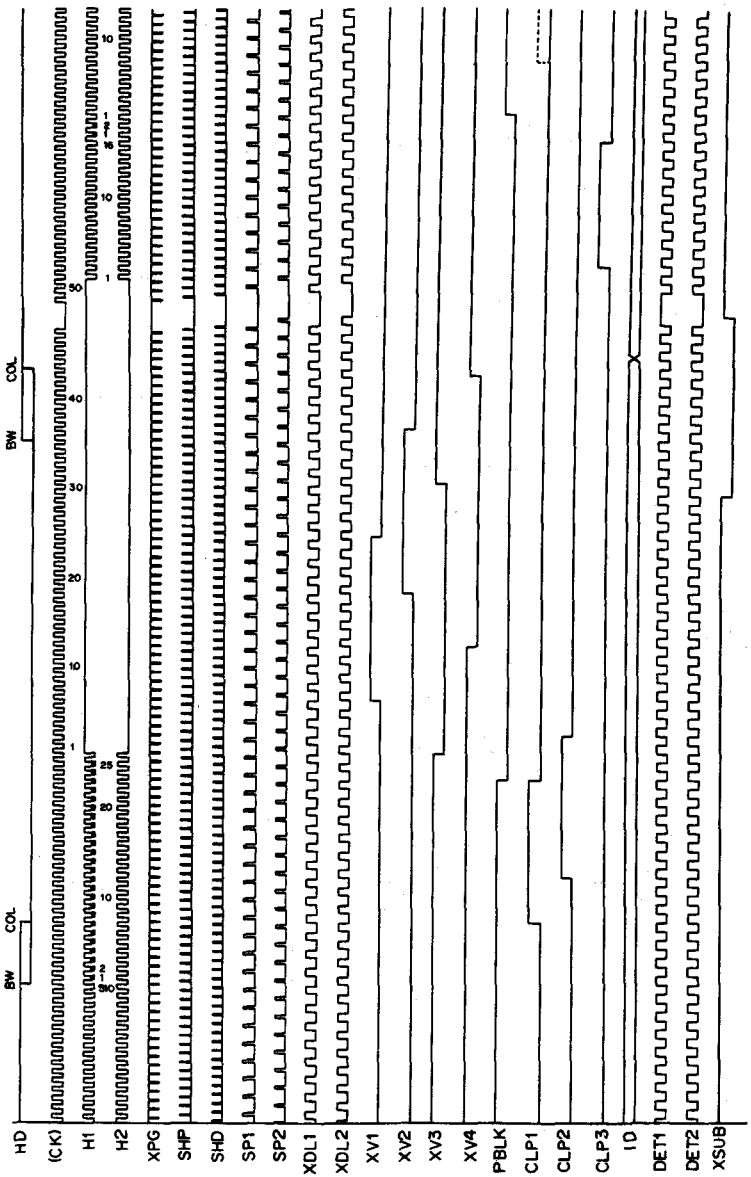
NTSC



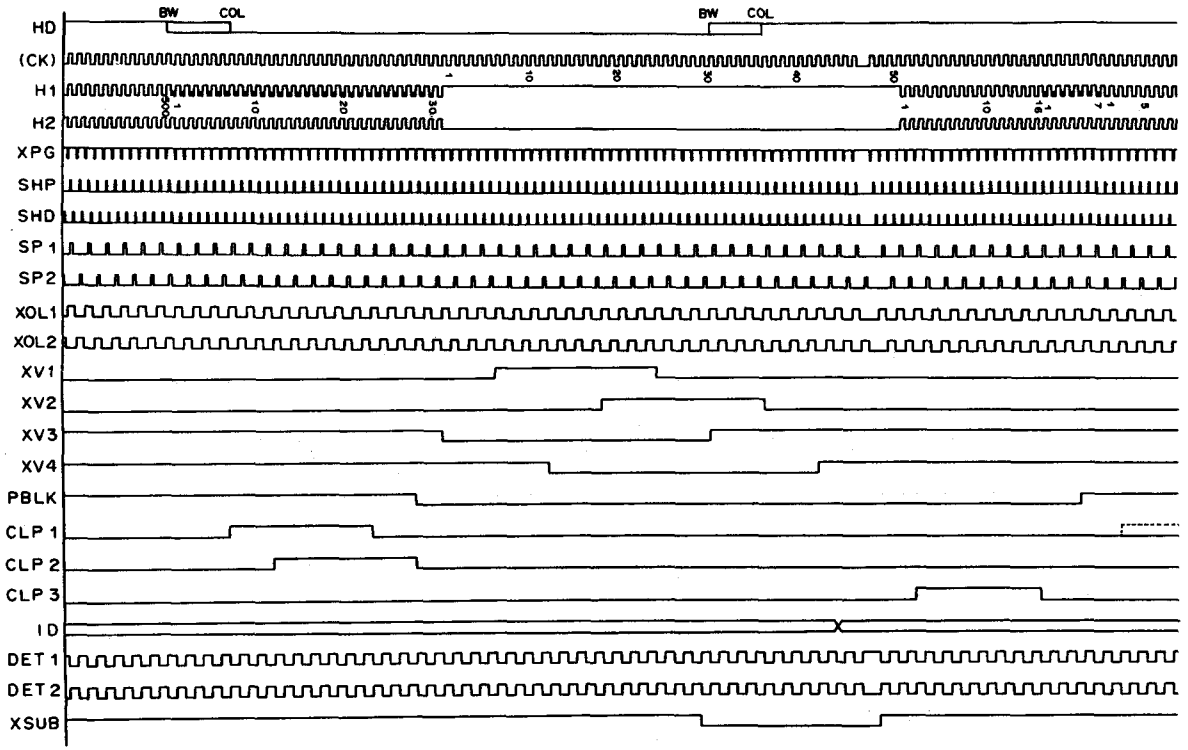
CCIR



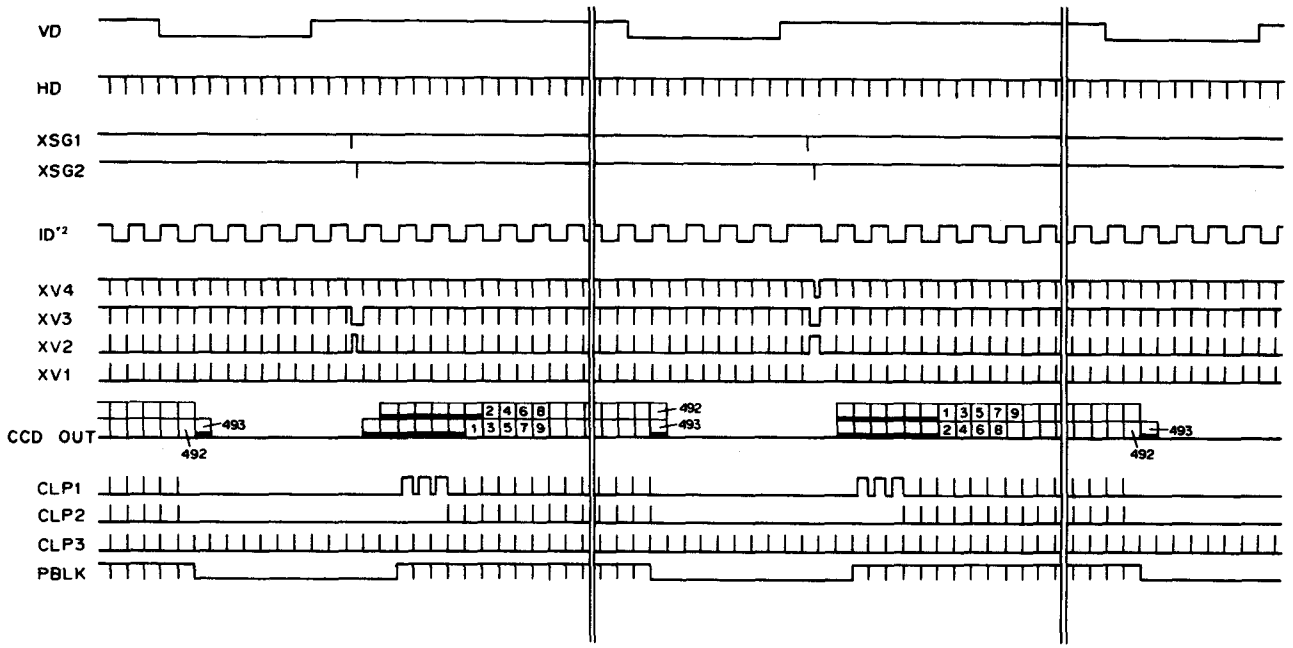
Timing Chart 2. [NTSC mode]



Timing Chart 3. [CCIR mode]

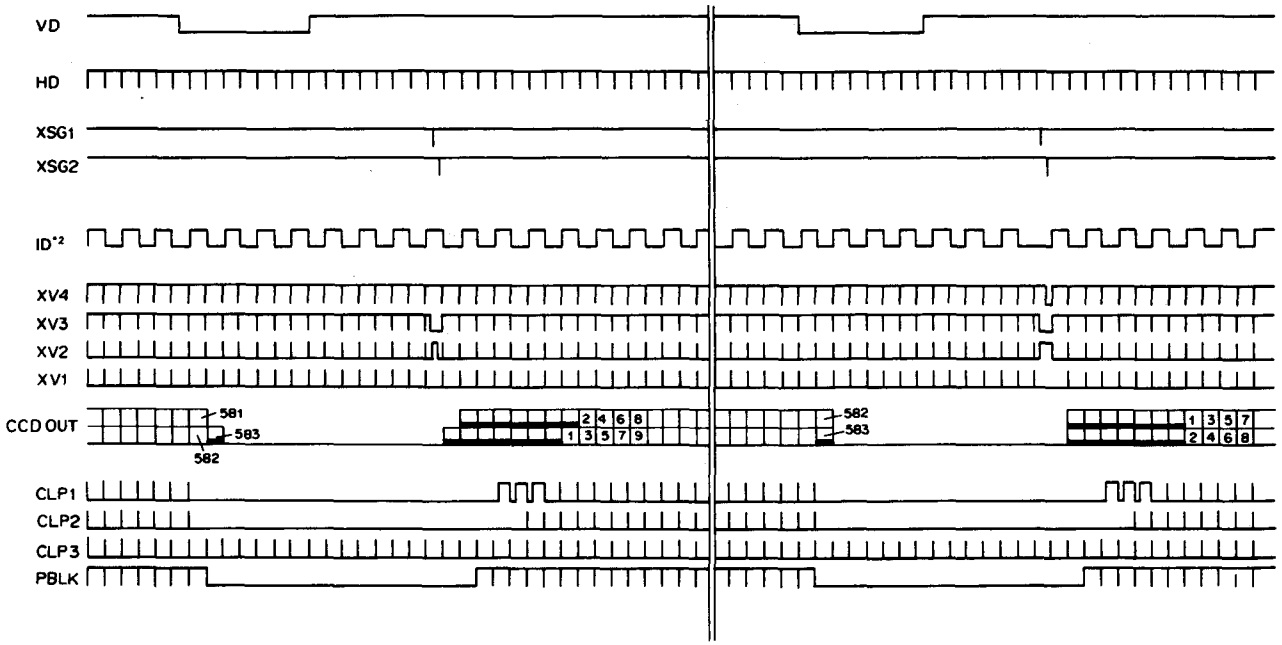


Timing Chart 4. [NTSC (Low speed timing) B/W mode]*1



Note) ***1.** 1 H advance of the output signal to VD/HD in color mode.
***2.** 0 level in monochrome mode.

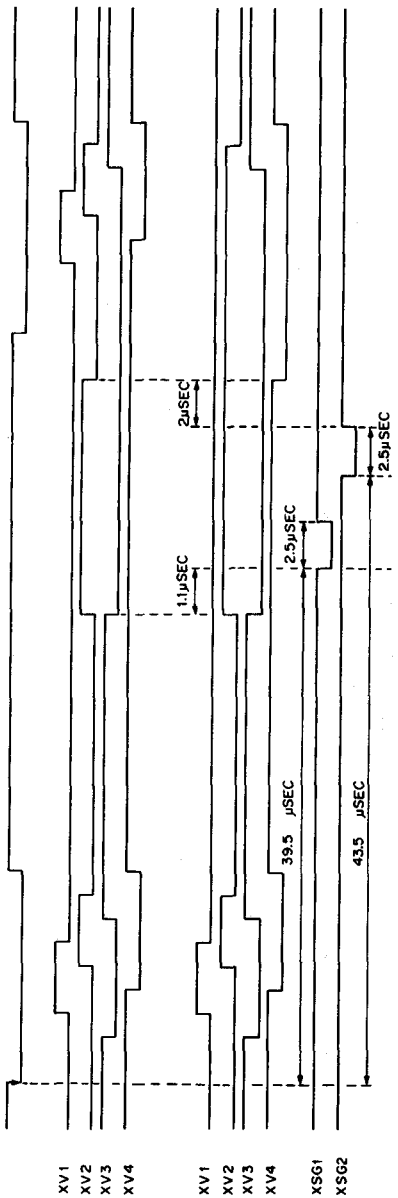
Timing Chart 5. [CCIR (Low speed timing)]*1



Note) ***1.** 1 H advance of the output signal to VD/HD in color mode.

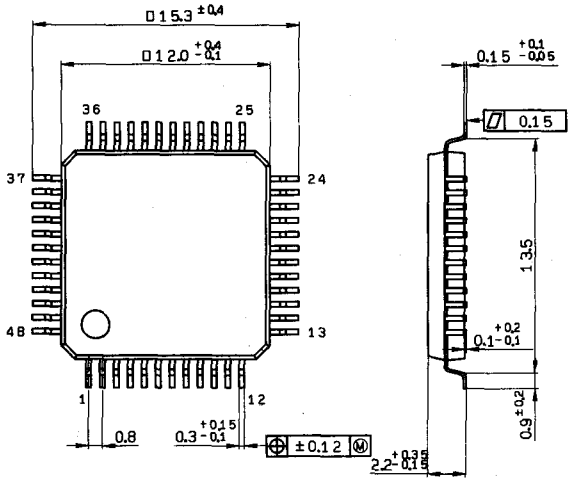
***2.** 0 level in monochrome mode.

Timing Chart 6. [XV1 to XV4 modulation]



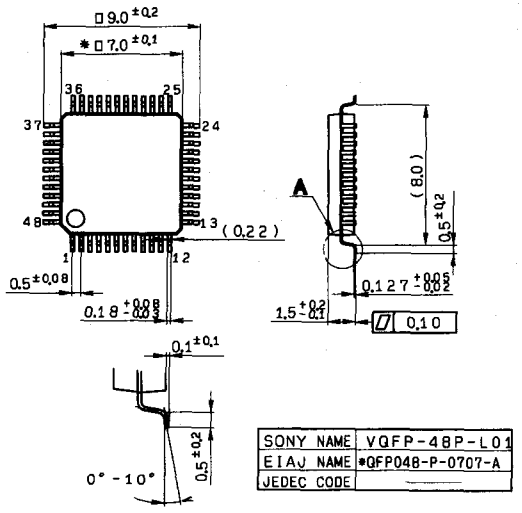
Package Outline Unit: mm

48pin QFP (Plastic) 0.7g



SONY NAME	QFP-48P-L04
EIAJ NAME	*QFP048-P-1212-B
JEDEC CODE	

48pin VQFP (Plastic) 0.2g



SONY NAME	VQFP-48P-L01
EIAJ NAME	*QFP048-P-0707-A
JEDEC CODE	

Detaild diagram of **A**

Note) Dimensions marked with * do not include residual resin.

SONY CXD1252AR/AQ

Timing Generator IC

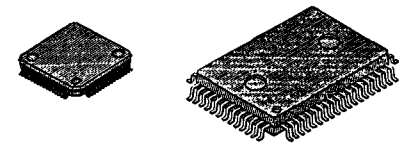
Description

The CXD1252A generates the timing pulses necessary for ICX038/039 and 3rd generation signal processing ICs.

Features

- QFP/VQFP package
- NTSC/PAL
- Field accumulation mode
- Complementary color mosaic filter coding
- Built-in electronic shutter
- Built-in blemish compensation circuit
- Built-in −4 to 5V driver (LH1)
- Built-in 0 to 5V driver (H1, H2)
  Also as an electronic shutter function,
- Shutter speed control
  (Serial input/Parallel input)
- Corresponds to all shutter speeds (Serial input)
- Compatible with low speed shutter/high speed shutter

64pin VQFP (Plastic) 64pin QFP (Plastic)



- Flickerless compatible
- Compatible with continuously variable shutter

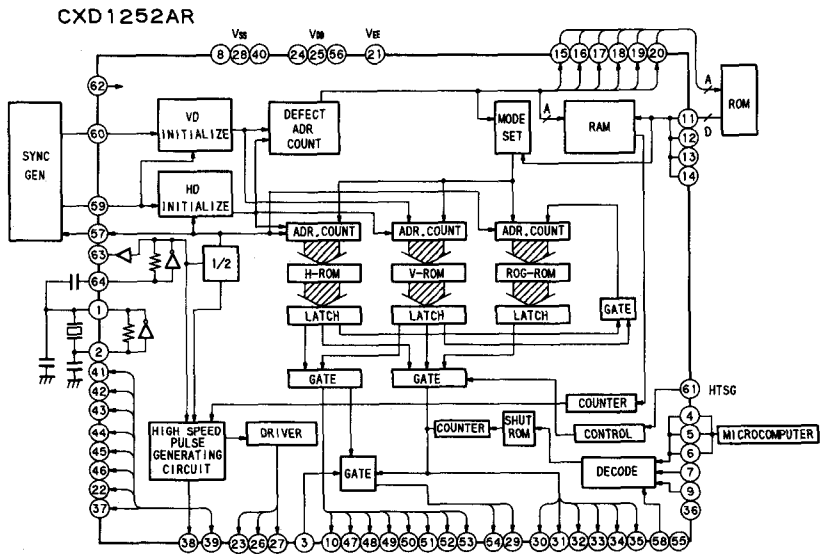
Applications

CCD camera system

Structure

Silicon gate CMOS IC

Block Diagram



E89Y15-HP

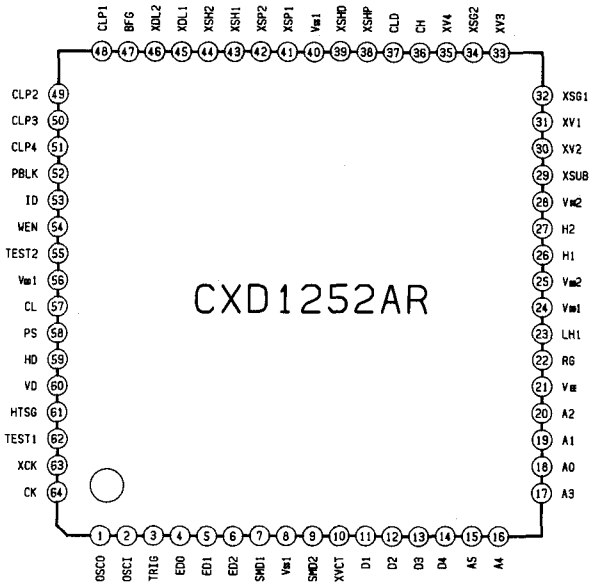
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	V_{SS}−0.5 to +7.0	V
• Input voltage	V_I	V_{SS}−0.5 to V_{DD}+0.5	V
• Output voltage	V_O	V_{SS}−0.5 to V_{DD}+0.5	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−55 to +150	°C
• Supply voltage	V_{EE}	−5 to V_{SS}	V

Recommended Operating Conditions

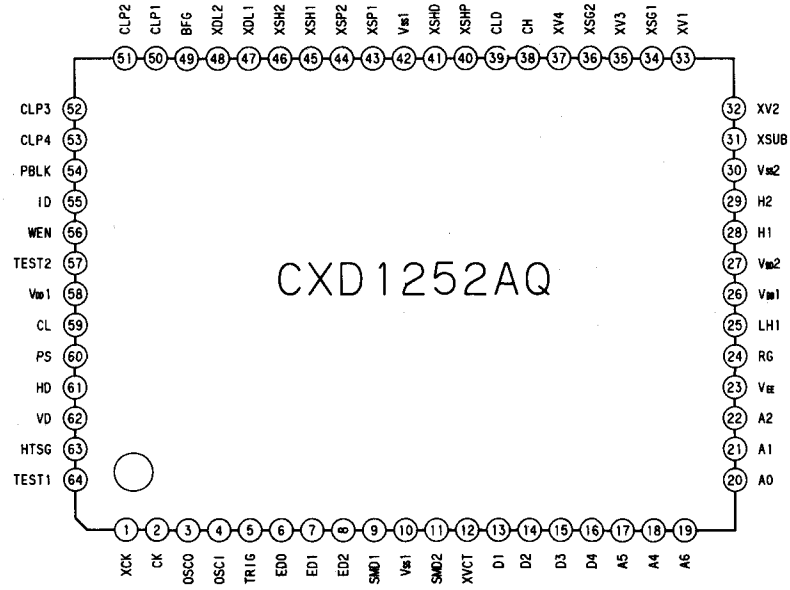
• Supply voltage	V_{DD}	4.75 to 5.25	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Supply voltage	V_{EE}	−4.2 to −3.8	V

Pin Configuration (1)



Mode	Pin	PRESET	L		H	
D1	11	L	ROM OFF		ROM ON	
D2	12	L	Normally Low			
D3	13	L	Normally Low			
D4	14	L	NTSC		PAL	
CH	36	L	Normally Low			
TEST2	55	L	Normally Low			
PS	58	H	Serial input		Parallel input	
HTSG	61	H	XSG1, 2OFF		Normal	
TEST1	62	L	Normally Low			
ED0	4	H	Shutter Speed			
ED1	5	H				
ED2	6	H				
SMD1	7	H	L	L	H	H
SMD2	9	H	L	H	L	H
MODE			Flickerless	High Speed Shutter	Low Speed Shutter	Shutter OFF

Pin Configuration (2)



Mode	Pin	PRESET	L		H	
D1	13	L	ROM OFF		ROM ON	
D2	14	L	Normally Low			
D3	15	L	Normally Low			
D4	16	L	NTSC		PAL	
CH	38	L	Normally Low			
TEST2	57	L	Normally Low			
PS	60	H	Serial input		Parallel input	
HTSG	63	H	XSG1, 2OFF		Normal	
TEST1	64	L	Normally Low			
EDO	6	H	Shutter Speed			
ED1	7	H				
ED2	8	H				
SMD1	9	H	L	L	H	H
SMD2	11	H	L	H	L	H
MODE			Flickerless	High Speed Shutter	Low Speed Shutter	Shutter OFF

Pin Description

Pin No. (VQFP)	Pin No. (QFP)	Symbol	I/O	Description
1	3	OSCO	O	Inverter output pin for oscillation
2	4	OSCI	I	Inverter input pin for oscillation
3	5	TRIG	I	Continuously variable shutter control pin (Pull-up resistance)
4	6	ED0	I	Shutter speed control pin (Details given later) (Pull-up resistance)
5	7	ED1	I	
6	8	ED2	I	
7	9	SMD1	I	Shutter mode setting pin (Pull-up resistance) (Details given later)
8	10	V_{SS}	—	GND
9	11	SMD2	I	Shutter mode setting pin (Pull-up resistance) (Details given later)
10	12	XVCT	O	Power supply control pin of external ROM
11	13	D1	I	Data input pin used when external ROM is employed / In case the external ROM is not employed (Pull-down resistance) / "Normally at L"
12	14	D2	I	"Normally at L"
13	15	D3	I	"Normally at L"
14	16	D4	I	L: NTSC H: PAL
15	17	A5	O	Address output pin to external ROM
16	18	A4	O	
17	19	A3	O	
18	20	A0	O	
19	21	A1	O	
20	22	A2	O	
21	23	V_{EE}	—	Negative power supply for LH1 (−4 V)
22	24	RG	O	Reset gate pulse output pin
23	25	LH1	O	Clock pulse output for CCD horizontal final register
24	26	V_{DD1}	—	Power supply pin
25	27	V_{DD2}	—	Power supply pin (For H1 and H2)
26	28	H1	O	Clock pulse output pin for CCD horizontal register drive
27	29	H2	O	Clock pulse output pin for CCD horizontal regester drive
28	30	V_{SS2}	—	GND (For H1 and H2)
29	31	XSUB	O	CCD discharge pulse output pin
30	32	XV2	O	Clock pulse output pin for CCD vertical register drive
31	33	XV1	O	Clock pulse output pin for CCD vertical register drive
32	34	XSG1	O	CCD sensor charge read out pulse output pin
33	35	XV3	O	Clock pulse output pin for CCD vertical register drive
34	36	XSG2	O	CCD sensor charge read out pulse output pin
35	37	XV4	O	Clock pulse output pin for CCD vertical register drive
36	38	CH	I	"Normally at L"
37	39	CLD	O	Delay clock
38	40	XSHP	O	Precharge level sample and hold pulse
39	41	XSHD	O	Data sample and hold pulse

Pin No. (VQFP)	Pin No. (QFP)	Symbol	I/O	Description
40	42	V_{SS1}	—	GND
41	43	XSP1	O	Color separation sample and hold pulse
42	44	XSP2	O	Color separation sample and hold pulse
43	45	XSH1	O	Select sample and hold pulse
44	46	XSH2	O	Select sample and hold pulse
45	47	XDL1	O	Delay line clock
46	48	XDL2	O	Delay line clock
47	49	BFG	O	Encoder chroma modulator pulse
48	50	CLP1	O	Pulse output pin for clamp
49	51	CLP2	O	
50	52	CLP3	O	
51	53	CLP4	O	
52	54	PBLK	O	Blanking cleaning pulse
53	55	ID	O	Line discrimination pin
54	56	WEN	O	Write enable pin (during low speed shutter only) (Details given later)
55	57	TEST2	I	Test pin "Normally at L"
56	58	V_{DD1}	—	Power supply pin
57	59	CL	O	Output pin of 1/2 frequency divided input clock from CK
58	60	PS	I	Electronic shutter speed data input L : Serial input H : Parallel input (pull-up resistance)
59	61	HD	I	Horizontal sync signal input pin
60	62	VD	I	Vertical sync signal input pin
61	63	HTSG	I	Control XSG1 and 2 L : XSG1 and 2 are stopped H : XSG1 and 2 are generated (Pull-up resistance)
62	64	TEST1	I	Test pin "Normally at L"
63	1	XCK	O	Inverted output pin of input clock from CK
64	2	CK	I	Inverter input pin for duty control (IC main clock input)

Electrical Characteristics

1) DC characteristics

(V_{DD}=5V±5%, V_{SS}=0V, T_{opr}=−20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		4.75	5.0	5.25	V
	V_{EE}		−4.2	−4.0	−3.8	V
I/O voltage	V_I, V_O		V_{SS}		V_{DD}	V
Input voltage	V_{IHC}		0.7V_{DD}			V
	V_{ILC}				0.3V_{DD}	V
*1 Input voltage	V_{IHT}		2.2			V
	V_{ILT}				0.8	V
Output voltage 1	V_{OH1}	I_{OH}=−2mA	V_{DD}−0.5			V
	V_{OL1}	I_{OL}=4mA			0.4	V
*2 Output voltage 2	V_{OH2}	I_{OH}=−4mA	V_{DD}−0.5			V
	V_{OL2}	I_{OL}=8mA			0.4	V
*3 Output voltage 3	V_{OH3}	I_{OH}=−8mA	V_{DD}−0.5			V
	V_{OL3}	I_{OL}=8mA			0.4	V
*4 Output voltage 4	V_{OH4}	I_{OH}=−2mA	V_{DD}−0.5			V
	V_{OL4}	I_{OL}=4mA			V_{EE}+0.4	V

*1. Pins 59 and 60 (HD, VD)
*2. Pins 22, 37, 38, 39 and 57 (RG, MCK, XSHP, XSHD, CL)
*3. Pins 26 and 27 (H1, H2)
*4. Pins 23 (LH1)

1)-a Oscillation I/O Electrical Characteristics

(OSCI, OSCO, CK, XCK)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical threshold value	L V_{TH}			$V_{DD/2}$		V
Input voltage	V_{IH}		0.7V_{DD}			V
	V_{IL}				0.3V_{DD}	V
Feedback resistor	R_{FB}	V_{IN} = V_{SS} or V_{DD}	500K	2M	5M	Ω
Output voltage	V_{OH}	I_{OH}=−1mA	$V_{DD/2}$			V
	V_{OL}	I_{OL}=1mA			$V_{DD/2}$	V

2) I/O Capacity

(V_{DD}=V_I=0V, f_M=1MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacity	C_{IN}				9	pF
Output capacity	C_{OUT}				11	pF

Electronic Shutter

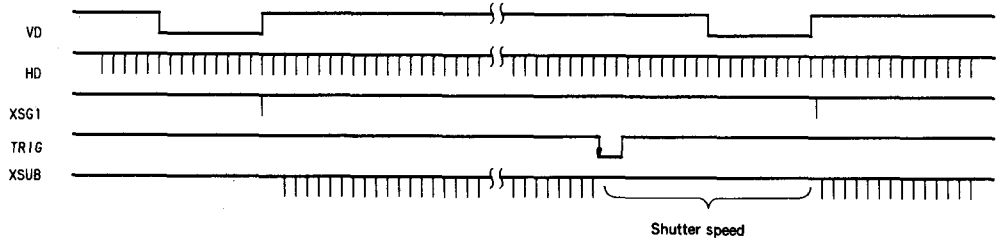
Shutter pins

PS, TRIG, SMD1, SMD2 ·····Mode
XSUB ·····Output
ED0, ED1, ED2 ·····Shutter speed

Order of priority of mode
TRIG› SMD1, 2› PS

Mode Operation

1. TRIG (Pull-up resistance)
   - For normal shutter operation, TRIG pin is either left open or connected to the power supply.
   - For continuous variable shutter operation, input a clock pulse to TRIG pin.



XSUB pulse that occurs during the period between XSG1 and the falling edge of TRIG is extracted. By stopping this XSUB pulse between the falling edge of TRIG and the next XSG1, the shutter speed is determined.

When the shutter speed is controlled using TRIG pin, to enlarge the control range it is necessary to set the shutter speed at 1/10000 by means of ED0, 1 and 2 pins as mentioned here after.

2. ED0, ED1 and ED2 (Shutter speed control pins)
   PS (Parallel input / Serial input select pin)
   SMD1 and 2 (Shutter mode select pins)

2-1. Shutter mode

Mode	Flickerless	High speed shutter	Low speed shutter	Without shutter
SMD1	L	L	H	H
SMD2	L	H	L	H

- Flickerless·····Mode to eliminate flicker resulting from fluorescent frequency
- High speed shutter·····Shutter with a speed faster than 1/60 (NTSC) and 1/50 (PAL)
- Low speed shutter·····Shutter with a speed lower than 1/60 (NTSC) and 1/50 (PAL)
- Without shutter·····There is no shutter operation.

2-2. PS

Either parallel input or serial input is selected as data input to determine the shutter speed.

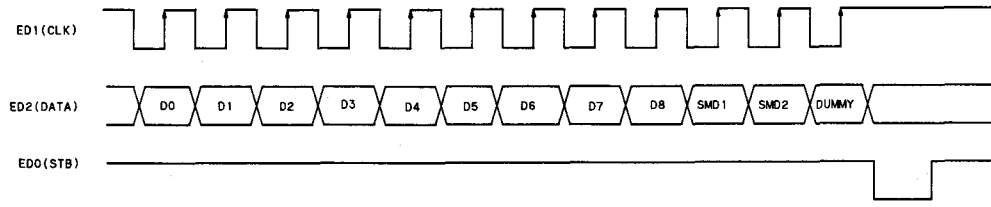
- Parallel input ·····8 shutter speeds are obtained with using the 3 bits; ED0, ED1 and ED2.
- Serial input·····Shutter speed is obtained with the input of ED0 (Strobe), ED1 (CLK) and ED2 (Data) to the respective pins.

2-2-1. [Parallel input]

Shutter Speed Corresponding Chart

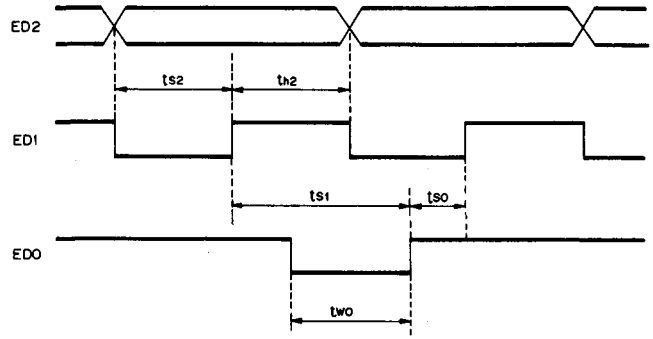
Mode	NTSC/PAL	PS	SMD1	SMD2	ED0	ED1	ED2	Shutter speed
OFF	X	X	H	H	X	X	X	Shutter OFF
Flickerless	NTSC	X	L	L	X	X	X	1/100 (S)
	PAL	X	L	L	X	X	X	1/120 (S)
High speed shutter	NTSC	H	L	H	H	H	H	1/60 (S)
	PAL	H	L	H	H	H	H	1/50 (S)
	X	H	L	H	L	H	H	1/125 (S)
	X	H	L	H	H	L	H	1/250 (S)
	X	H	L	H	L	L	H	1/500 (S)
	X	H	L	H	H	H	L	1/1000 (S)
	X	H	L	H	L	H	L	1/2000 (S)
	X	H	L	H	H	L	L	1/4000 (S)
	X	H	L	H	L	L	L	1/10000 (S)
Low speed shutter	X	H	H	L	H	H	H	2FLD
	X	H	H	L	L	H	H	4FLD
	X	H	H	L	H	L	H	6FLD
	X	H	H	L	L	L	H	8FLD
	X	H	H	L	H	H	L	10FLD
	X	H	H	L	L	H	L	12FLD
	X	H	H	L	H	L	L	14FLD
	X	H	H	L	L	L	L	16FLD

2-2-2. [Serial input]



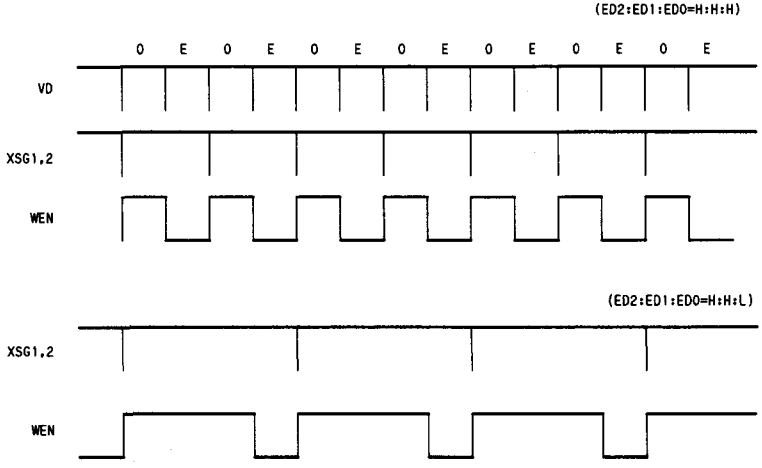
ED2 data is latched in the register with the rising edge of ED1 and loaded inside at the ED0 low period.

AC Characteristics



Symbol		Min.	Max.
t_{s2}	ED2 set up time in relation to ED1 rise	20ns	—
t_{h2}	ED2 hold time in relation to ED1 rise	20ns	—
t_{s1}	ED1 rise set up time in relation to EDO rise	20ns	—
t_{wo}	EDO pulse width	20ns	50μs
t_{so}	EDO rise set up time in relation to ED1 rise	20ns	—

2-2-3. [Low speed shutter timing chart]



2-2-4. [Shutter speed calculating formula]

High speed shutter

- For NTSC

  $T=[262_{10}-(1FF_{16}-L_{16})]\times 63.56+34.78\mu s$

- For PAL

  $T=[312_{10}-(1FF_{16}-L_{16})]\times 64+35.6\mu s$

NTSC			PAL		
Load value	Shutter speed	Calculated value	Load value	Shutter speed	Calculated value
FA_{16}	1/10000	1/10169	$C8_{16}$	1/10000	1/10040
FC_{16}	1/4000	1/4435	CA_{16}	1/4000	1/4394
100_{16}	1/2000	1/2085	CE_{16}	1/2000	1/2068
108_{16}	1/1000	1/1012	$D6_{16}$	1/1000	1/1004
118_{16}	1/500	1/499	$E6_{16}$	1/500	1/495
137_{16}	1/250	1/252	105_{16}	1/250	1/250
176_{16}	1/125	1/125	143_{16}	1/125	1/125
196_{16}	1/100	1/100	149_{16}	1/120	1/120

Low speed shutter

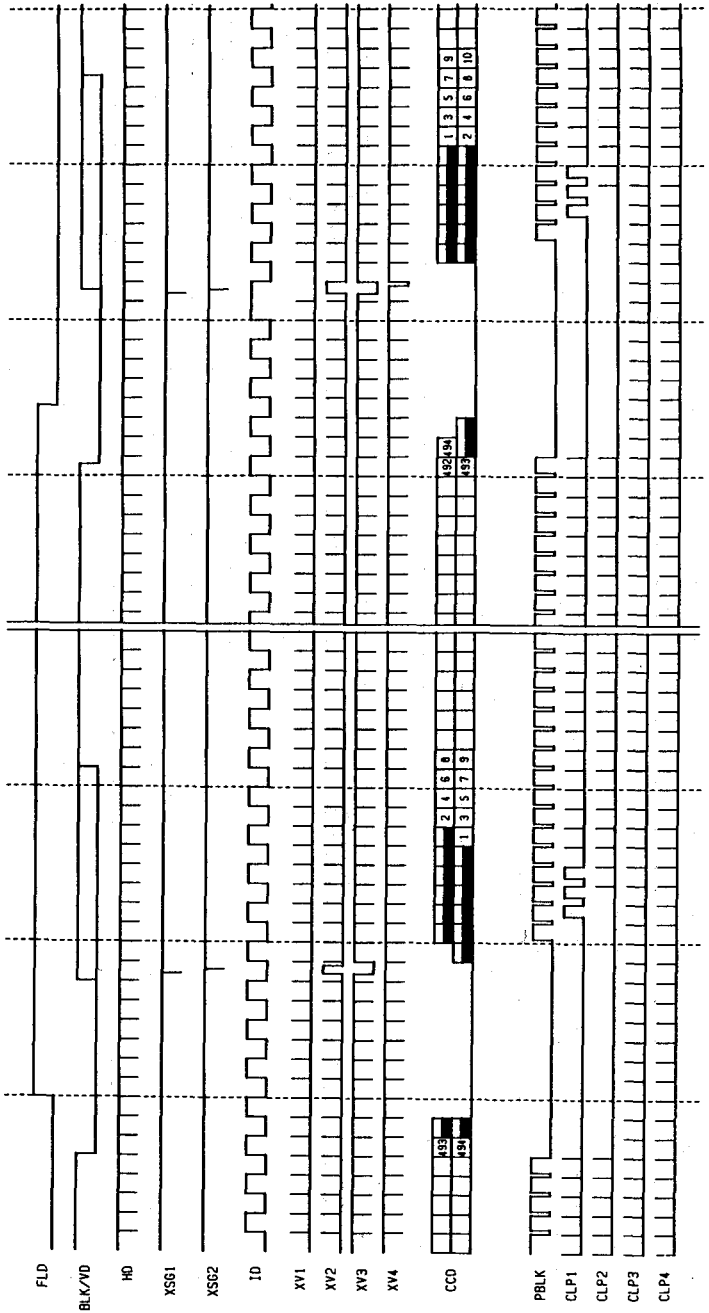
Shutter speed calculating formula

- $N=2\times(FF_{16}-L_{16})$ FLD

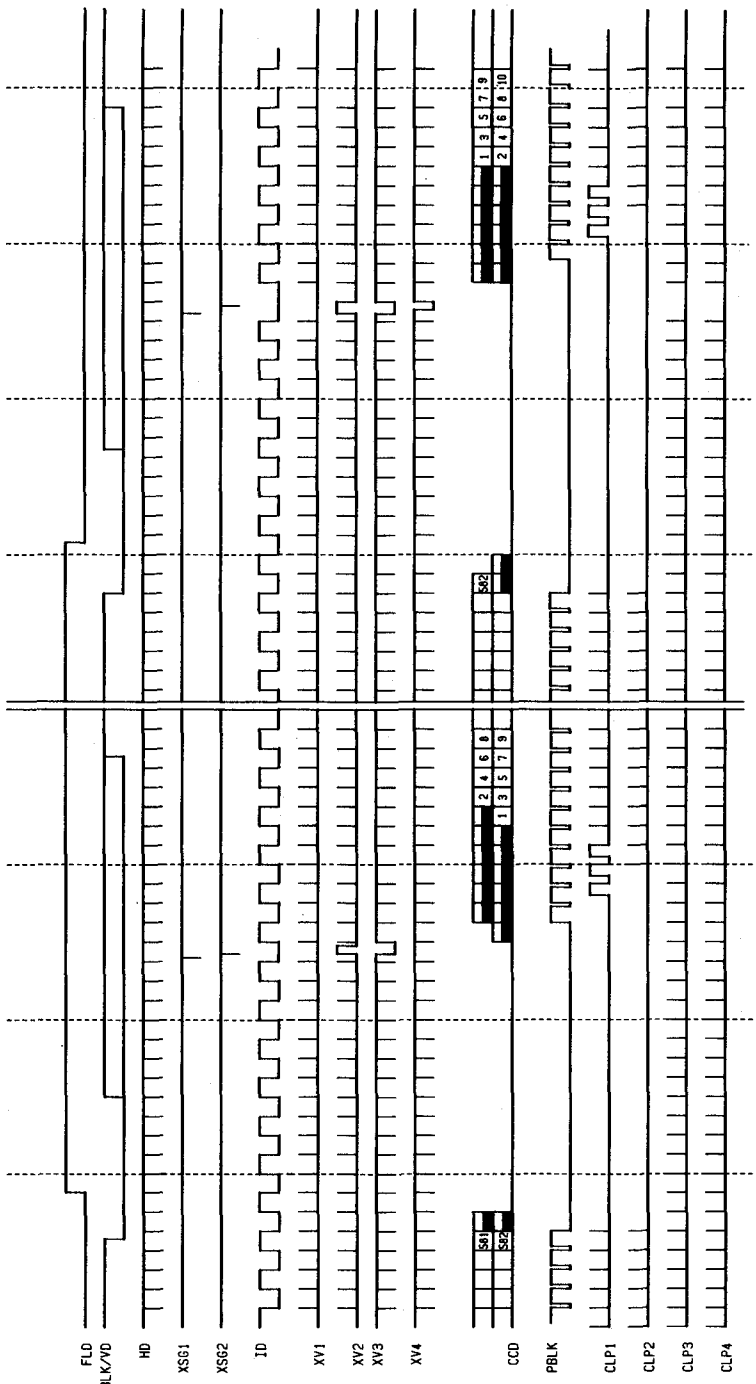
  However FF_{16} cannot be used as a load value.

Load value	Shutter speed (FLD)
FE_{16}	2
FD_{16}	4
⋮	⋮
01_{16}	508
00_{16}	510

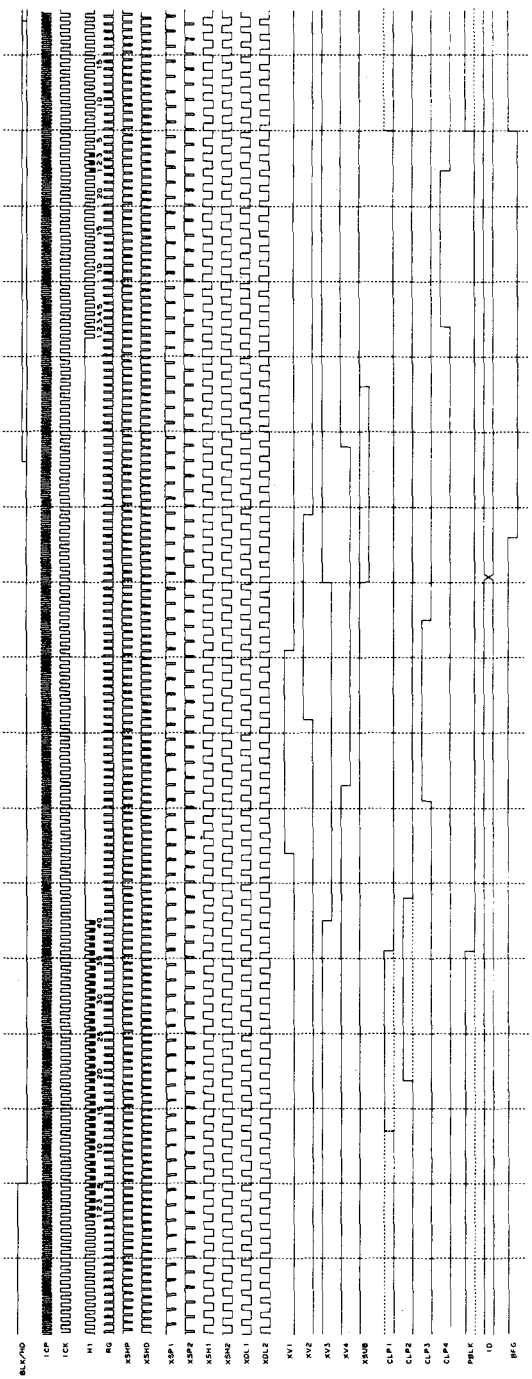
Time Chart (1) 〈NTSC vertical direction〉



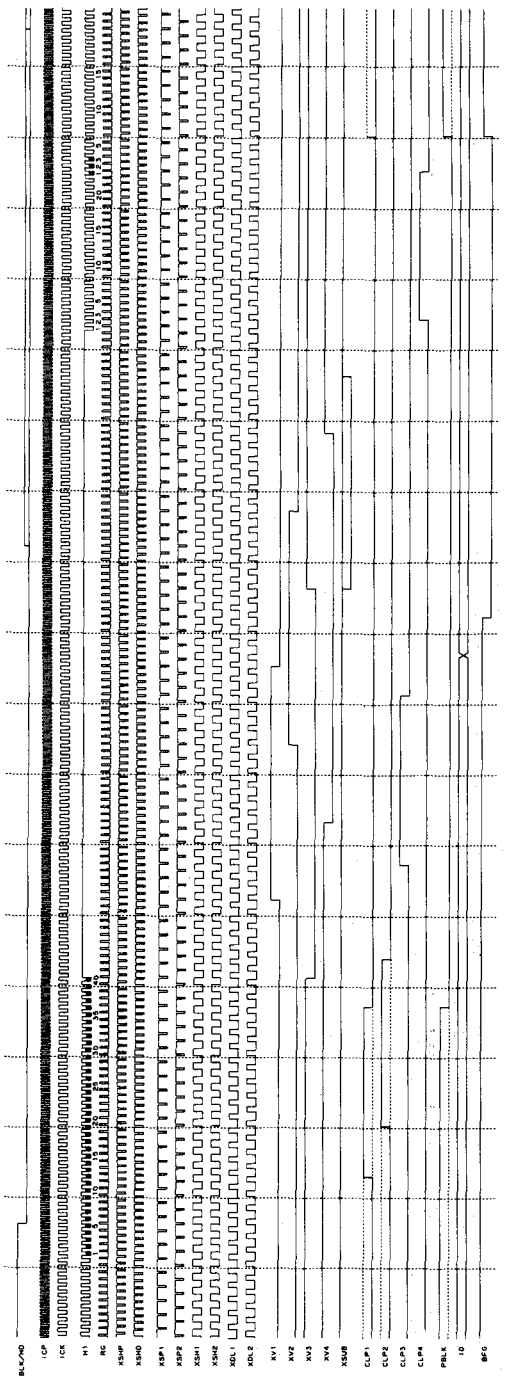
Time Chart (2) ⟨PAL vertical direction⟩



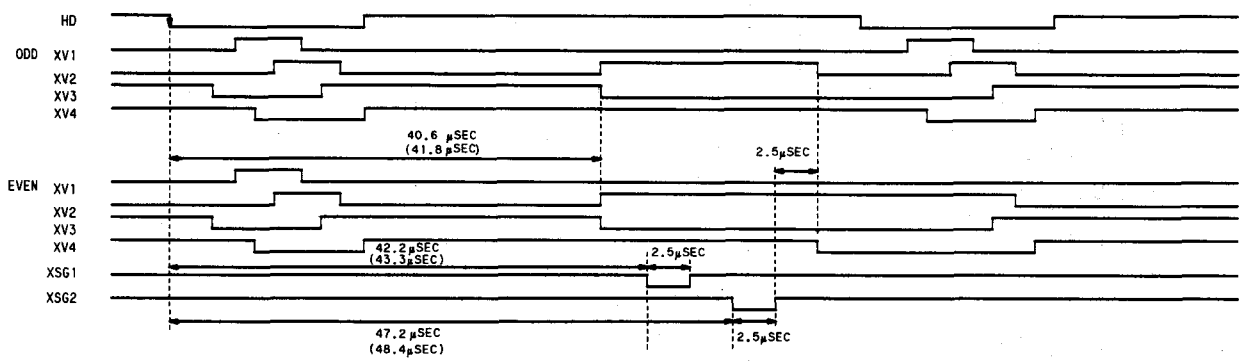
Time Chart (3) 〈NTSC horizontal direction〉



Time Chart (4) 〈PAL horizontal direction〉

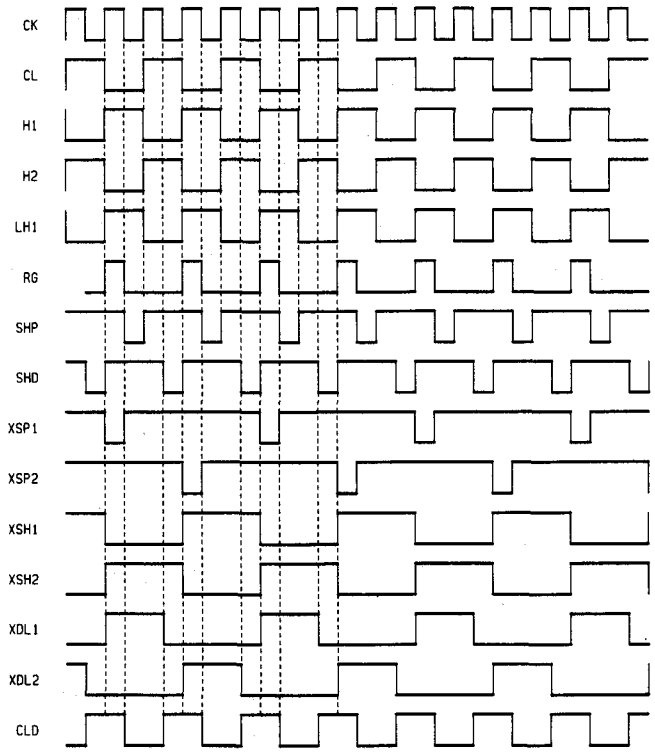


Time Chart (5) 〈XV1 to XV4 modulation〉



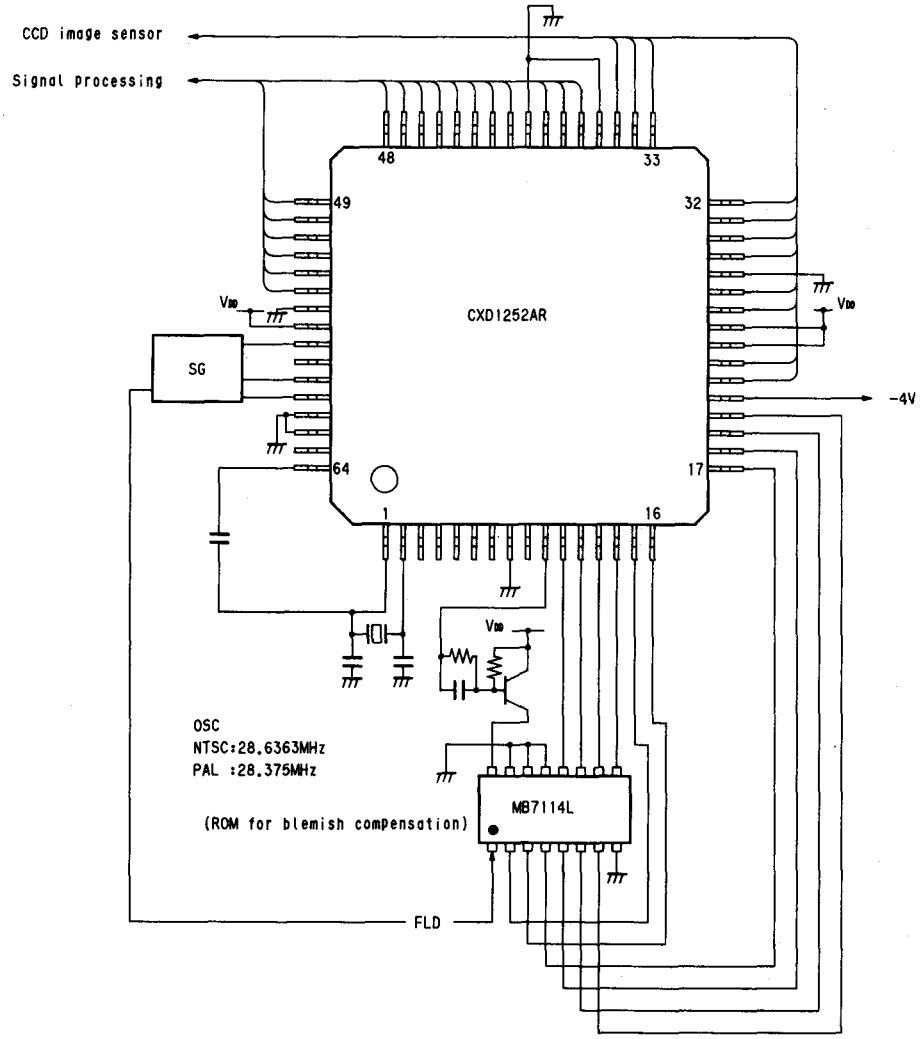
Note) Time at PAL mode is given in parentheses.

Time Chart (6) 〈High speed phase〉



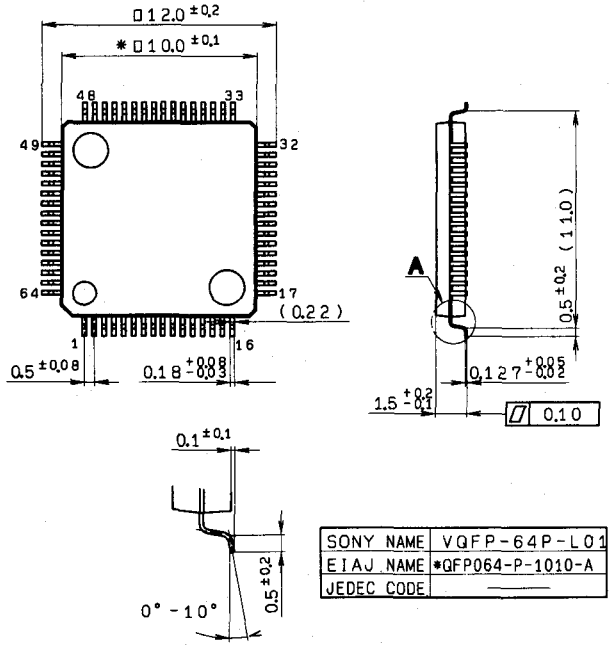
⟨Application Circuit⟩

VQFP Package



Package Outline Unit : mm

CXD1252AR 64pin VQFP (Plastic) 0.3g

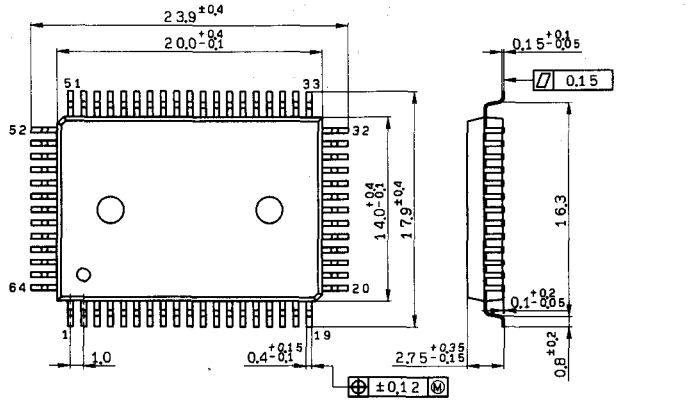


SONY NAME	VQFP-64P-L01
EIAJ NAME	*QFP064-P-1010-A
JEDEC CODE	———

Detailed diagram of A

Dimensions marked with * does not include resin residue

CXD1252AQ 64pin QFP (Plastic) 1.5g



SONY NAME	QFP-64P-L01
EIAJ NAME	*QFP064-P-1420-A
JEDEC CODE	———

Timing Generator IC

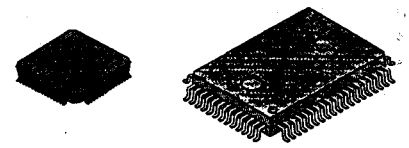
Description

The CXD1253AR/AQ is a timing generator IC which generates the timing pulses necessary for ICX026CK, ICX027CK, ICX044AK and ICX045AK.

Features

- QFP/VQFP package
- NTSC/PAL
- Field accumulation mode
- Built-in electronic shutter
- Built-in blemish compensation circuit
- Built-in 0 to 5V driver (H1, H2)
- Abundant electronic shutter functions,
- Shutter speed control
  (Serial input/Parallel input)
- Corresponds to all shutter speeds (Serial input)
- Compatible with low speed shutter/high speed shutter

64pin VQFP (Plastic) 64pin QFP (Plastic)



- Flickerless compatible
- Compatible with continuously variable shutter

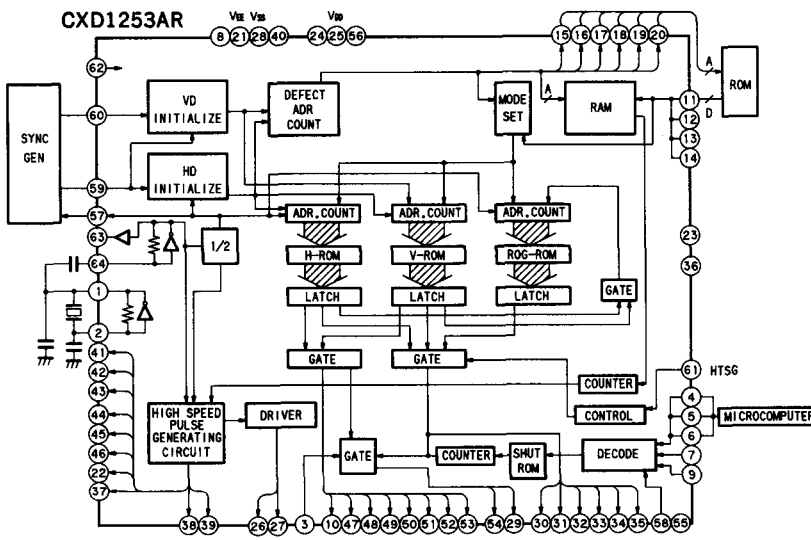
Applications

CCD camera system

Structure

Silicon gate CMOS IC

Block Diagram



E91147-HP

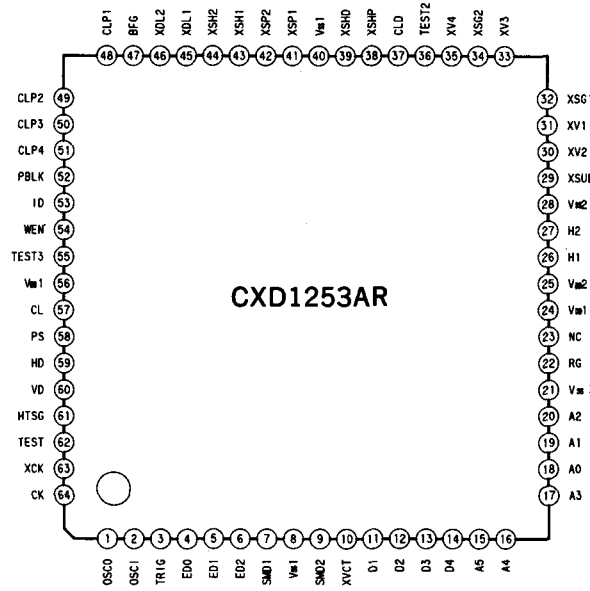
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	V_{SS}−0.5 to +7.0	V
• Input voltage	V_I	V_{SS}−0.5 to V_{DD}+0.5	V
• Output voltage	V_O	V_{SS}−0.5 to V_{DD}+0.5	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−55 to +150	°C
• Supply voltage	V_{EE}	−5 to V_{SS}	V

Recommended Operating Conditions

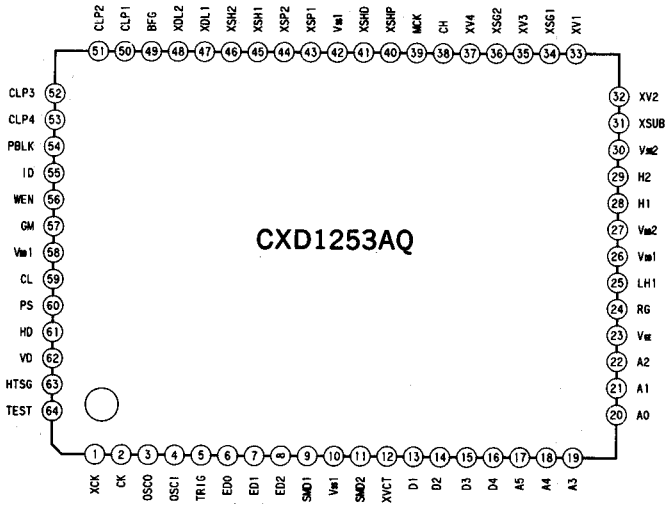
• Supply voltage	V_{DD}	4.75 to 5.25	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Supply voltage	V_{EE}	−4.2 to −3.8	V

Pin Configuration (1)



Mode	Pin	PRESET	L		H	
D1	11	L	ROM OFF		ROM ON	
D2	12	L	Normally Low			
D3	13	L	Normally Low			
D4	14	L	NTSC		PAL	
TEST3	55	L	Normally Low			
PS	58	H	Serial input		Parallel input	
HTSG	61	H	XSG1, 2 OFF		Normal	
ED0	4	H	Shutter Speed			
ED1	5	H				
ED2	6	H				
SMD1	7	H	L	L	H	H
SMD2	9	H	L	H	L	H
MODE			Flickerless	High Speed Shutter	Low Speed Shutter	Shutter OFF

Pin Configuration (2)



Mode	Pin	PRESET	L		H	
D1	13	L	ROM OFF		ROM ON	
D2	14	L	Normally Low			
D3	15	L	Normally Low			
D4	16	L	PAL		NTSC	
TEST3	57	L	Normally Low			
PS	60	H	Serial input		Parallel input	
HTSG	63	H	XSG1, 2 OFF		Normal	
ED0	6	H	Shutter Speed			
ED1	7	H				
ED2	8	H				
SMD1	9	H	L	L	H	H
SMD2	11	H	L	H	L	H
MODE			Flickerless	High Speed Shutter	Low Speed Shutter	Shutter OFF

Pin Description

Pin No. (VQFP)	Pin No. (QFP)	Symbol	I/O	Description
1	3	OSCO	O	Inverter output pin for oscillation
2	4	OSCI	I	Inverter input pin for oscillation
3	5	TRIG	I	Continuously variable shutter control pin (Pull-up resistance)
4	6	ED0	I	Shutter speed control pin (Details given later) (Pull-up resistance)
5	7	ED1	I	
6	8	ED2	I	
7	9	SMD1	I	Shutter mode setting pin (Pull-up resistance) (Details given later)
8	10	V_{SS}	—	GND
9	11	SMD2	I	Shutter mode setting pin (Pull-up resistance) (Details given later)
10	12	XVCT	O	Power supply control pin of external ROM
11	13	D1	I	Data input pin used when external ROM is employed / In case the external ROM is not employed (Pull-down resistance) / "Normally at L"
12	14	D2	I	"Normally at L"
13	15	D3	I	"Normally at L"
14	16	D4	I	L: NTSC / H: PAL
15	17	A5	O	Address output pin to external ROM
16	18	A4	O	
17	19	A3	O	
18	20	A0	O	
19	21	A1	O	
20	22	A2	O	
21	23	V_{SS3}	—	GND
22	24	RG	O	Reset gate pulse output pin
23	25	NC	O	Do not connect anything
24	26	V_{DD1}	—	Power supply pin
25	27	V_{DD2}	—	Power supply pin (For H1 and H2)
26	28	H1	O	Clock pulse output pin for CCD horizontal register drive
27	29	H2	O	Clock pulse output pin for CCD horizontal register drive
28	30	V_{SS2}	—	GND (For H1 and H2)
29	31	XSUB	O	CCD discharge pulse output pin
30	32	XV2	O	Clock pulse output pin for CCD vertical register drive
31	33	XV1	O	Clock pulse output pin for CCD vertical register drive
32	34	XSG1	O	CCD sensor charge read out pulse output pin
33	35	XV3	O	Clock pulse output pin for CCD vertical register drive
34	36	XSG2	O	CCD sensor charge read out pulse output pin
35	37	XV4	O	Clock pulse output pin for CCD vertical register drive
36	38	TEST2	I	Do not connect anything
37	39	CLD	O	Delay clock
38	40	XSHP	O	Precharge level sample and hold pulse
39	41	XSHD	O	Data sample and hold pulse

Pin No. (VQFP)	Pin No. (QFP)	Symbol	I/O	Description
40	42	V_{SS1}	—	GND
41	43	XSP1	O	Color separation sample and hold pulse
42	44	XSP2	O	Color separation sample and hold pulse
43	45	XSH1	O	Select sample and hold pulse
44	46	XSH2	O	Select sample and hold pulse
45	47	XDL1	O	Delay line clock
46	48	XDL2	O	Delay line clock
47	49	BFG	O	Encoder chroma modulator pulse
48	50	CLP1	O	Pulse output pin for clamp
49	51	CLP2	O	
50	52	CLP3	O	
51	53	CLP4	O	
52	54	PBLK	O	Blanking cleaning pulse
53	55	ID	O	Line discrimination pin
54	56	WEN	O	Write enable pin (during low speed shutter only) (Details given later)
55	57	TEST3	I	Test pin "Normally at L"
56	58	V_{DD1}	—	Power supply pin
57	59	CL	O	Output pin of 1/2 frequency divided input clock from CK
58	60	PS	I	Electronic shutter speed data input L : Serial input H : Parallel input (pull-up resistance)
59	61	HD	I	Horizontal sync signal input pin
60	62	VD	I	Vertical sync signal input pin
61	63	HTSG	I	Control XSG1 and 2 L : XSG1 and 2 are stopped H : XSG1 and 2 are generated (Pull-up resistance)
62	64	TEST	I	Test pin "Normal mode at L" "Test mode at H" (Pull-down resistance)
63	1	XCK	O	Inverted output pin of input clock from CK
64	2	CK	I	Inverter input pin for duty control (IC main clock input)

Electrical Characteristics

1) DC characteristics

(V_{DD}=5V±5%, V_{SS}=0V, T_{opr}=−20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		4.75	5.0	5.25	V
I/O voltage	V_I, V_O		V_{SS}		V_{DD}	V
Input voltage	V_{IHC}		0.7V_{DD}			V
	V_{ILC}				0.3V_{DD}	V
*1 Input voltage	V_{IHT}		2.2			V
	V_{ILT}				0.8	V
Output voltage 1	V_{OH1}	I_{OH}=−2mA	V_{DD}−0.5			V
	V_{OL1}	I_{OL}=4mA			0.4	V
*2 Output voltage 2	V_{OH2}	I_{OH}=−4mA	V_{DD}−0.5			V
	V_{OL2}	I_{OL}=8mA			0.4	V
*3 Output voltage 3	V_{OH3}	I_{OH}=−8mA	V_{DD}−0.5			V
	V_{OL3}	I_{OL}=8mA			0.4	V

*1. Pins 59 and 60 (HD, VD)
*2. Pins 22, 37, 38, 39 and 57 (RG, MCK, XSHP, XSHD, CL)
*3. Pins 26 and 27 (H1, H2)

1)-a Oscillation I/O Electrical Characteristics

(OSCI, OSCO, CK, XCK)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical threshold value	L V_{TH}			$V_{DD/2}$		V
Input voltage	V_{IH}		0.7V_{DD}			V
	V_{IL}				0.3V_{DD}	V
Feedback resistor	R_{FB}	V_{IN} = V_{SS} or V_{DD}	500K	2M	5M	Ω
Output voltage	V_{OH}	I_{OH}=−1mA	$V_{DD/2}$			V
	V_{OL}	I_{OL}=1mA			$V_{DD/2}$	V

2) I/O Capacity

(V_{DD}=V_I=0V, f_M=1MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacity	C_{IN}				9	pF
Output capacity	C_{OUT}				11	pF

Electronic Shutter

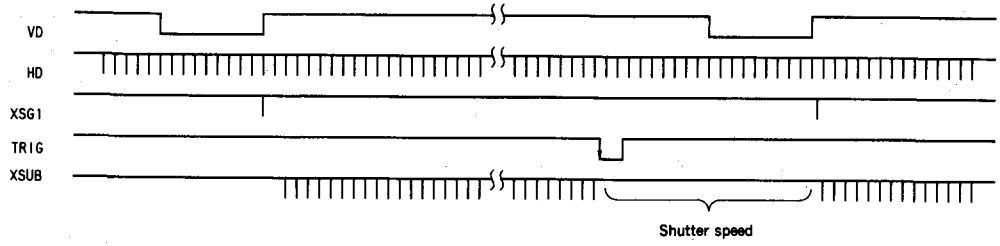
Shutter pins

PS, TRIG, SMD1, SMD2 ·····Mode
XSUB ·····Output
ED0, ED1, ED2 ·····Shutter speed

Order of priority of mode
TRIG> SMD1, 2> PS

Mode Operation

1. TRIG (Pull-up resistance)
   - For normal shutter operation, TRIG pin is either left open or connected to the power supply.
   - For continuous variable shutter operation, input a clock pulse to TRIG pin.



XSUB pulse that occurs during the period between XSG1 and the falling edge of TRIG is extracted. By stopping this XSUB pulse between the falling edge of TRIG and the next XSG1, the shutter speed is determined.

When the shutter speed is controlled using TRIG pin, to enlarge the control range it is necessary to set the shutter speed at 1/10000 by means of ED0, 1 and 2 pins as mentioned here after.

2. ED0, ED1 and ED2 (Shutter speed control pins)
   PS (Parallel input / Serial input select pin)
   SMD1 and 2 (Shutter mode select pins)

2-1. Shutter mode

Mode	Flickerless	High speed shutter	Low speed shutter	Without shutter
SMD1	L	L	H	H
SMD2	L	H	L	H

- Flickerless·····Mode to eliminate flicker resulting from fluorescent frequency
- High speed shutter·····Shutter with a speed faster than 1/60 (NTSC) and 1/50 (PAL)
- Low speed shutter·····Shutter with a speed lower than 1/60 (NTSC) and 1/50 (PAL)
- Without shutter·····There is no shutter operation.

2-2. PS

Either parallel input or serial input is selected as data input to determine the shutter speed.

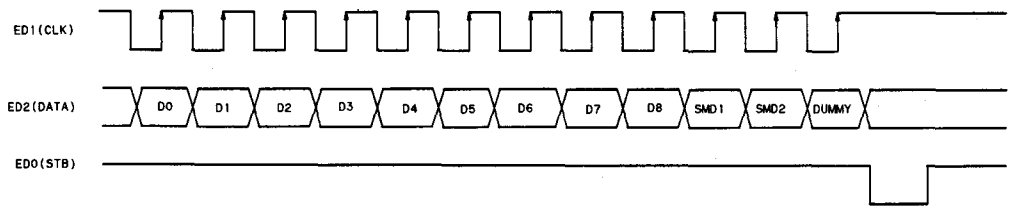
- Parallel input ·····8 shutter speeds are obtained with using the 3 bits; ED0, ED1 and ED2.
- Serial input·····Shutter speed is obtained with the input of ED0 (Strobe), ED1 (CLK) and ED2 (Data) to the respective pins.

2-2-1. [Parallel input]

Shutter Speed Corresponding Chart

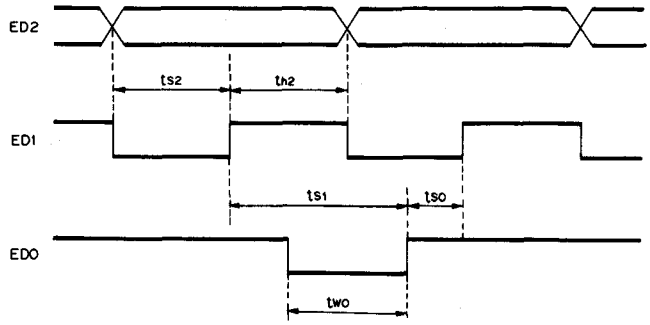
Mode	NTSC/PAL	PS	SMD1	SMD2	ED0	ED1	ED2	Shutter speed
OFF	X	X	H	H	X	X	X	Shutter OFF
Flickerless	NTSC	X	L	L	X	X	X	1/100 (S)
	PAL	X	L	L	X	X	X	1/120 (S)
High speed shutter	NTSC	H	L	H	H	H	H	1/60 (S)
	PAL	H	L	H	H	H	H	1/50 (S)
	X	H	L	H	L	H	H	1/125 (S)
	X	H	L	H	H	L	H	1/250 (S)
	X	H	L	H	L	L	H	1/500 (S)
	X	H	L	H	H	H	L	1/1000 (S)
	X	H	L	H	L	H	L	1/2000 (S)
	X	H	L	H	H	L	L	1/4000 (S)
	X	H	L	H	L	L	L	1/10000 (S)
Low speed shutter	X	H	H	L	H	H	H	2FLD
	X	H	H	L	L	H	H	4FLD
	X	H	H	L	H	L	H	6FLD
	X	H	H	L	L	L	H	8FLD
	X	H	H	L	H	H	L	10FLD
	X	H	H	L	L	H	L	12FLD
	X	H	H	L	H	L	L	14FLD
	X	H	H	L	L	L	L	16FLD

2-2-2. [Serial input]



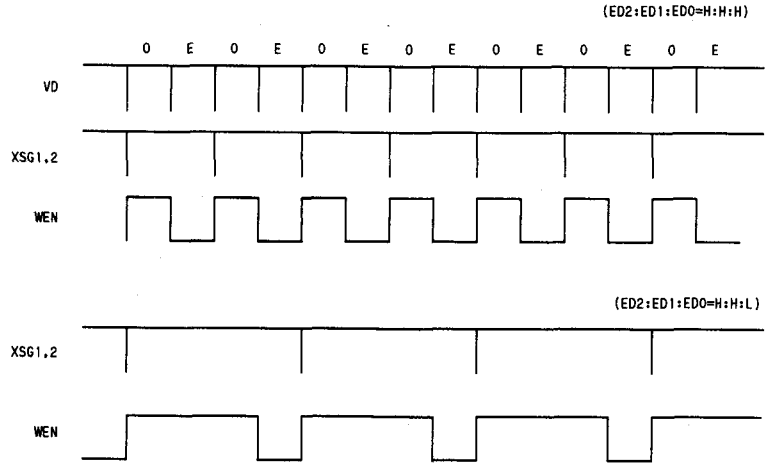
ED2 data is latched in the register with the rising edge of ED1 and loaded inside at the ED0 low period.

AC Characteristics



Symbol		Min.	Max.
t_{s2}	ED2 set up time in relation to ED1 rise	20ns	—
t_{h2}	ED2 hold time in relation to ED1 rise	20ns	—
t_{s1}	ED1 rise set up time in relation to EDO rise	20ns	—
t_{WO}	EDO pulse width	20ns	50μs
t_{SO}	EDO rise set up time in relation to ED1 rise	20ns	—

2-2-3. [Low speed shutter timing chart]



2-2-4. [Shutter speed calculating formula]

High speed shutter

- For NTSC

  $T=[262_{10}-(1FF_{16}-L_{16})]\times 63.56+34.78\mu s$

- For PAL

  $T=[312_{10}-(1FF_{16}-L_{16})]\times 64+35.6\mu s$

NTSC			PAL		
Load value	Shutter speed	Calculated value	Load value	Shutter speed	Calculated value
FA_{16}	1/10000	1/10169	$C8_{16}$	1/1000	1/10040
FC_{16}	1/4000	1/4435	CA_{16}	1/4000	1/4394
100_{16}	1/2000	1/2085	CE_{16}	1/2000	1/2068
108_{16}	1/1000	1/1012	$D6_{16}$	1/1000	1/1004
118_{16}	1/500	1/499	$E6_{16}$	1/500	1/495
137_{16}	1/250	1/252	105_{16}	1/250	1/250
176_{16}	1/125	1/125	143_{16}	1/125	1/125
196_{16}	1/100	1/100	149_{16}	1/120	1/120

Low speed shutter

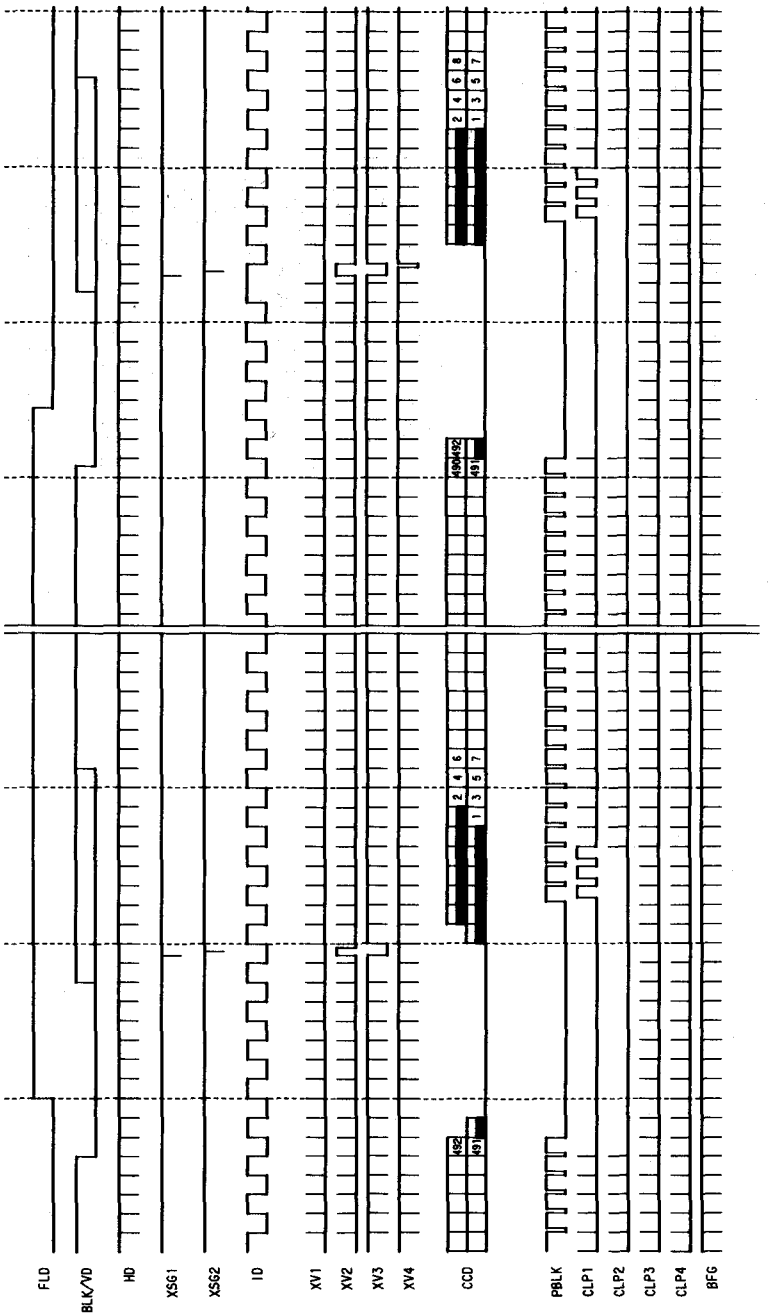
Shutter speed calculating formula

- $N=2\times(FF_{16}-L_{16})$ FLD

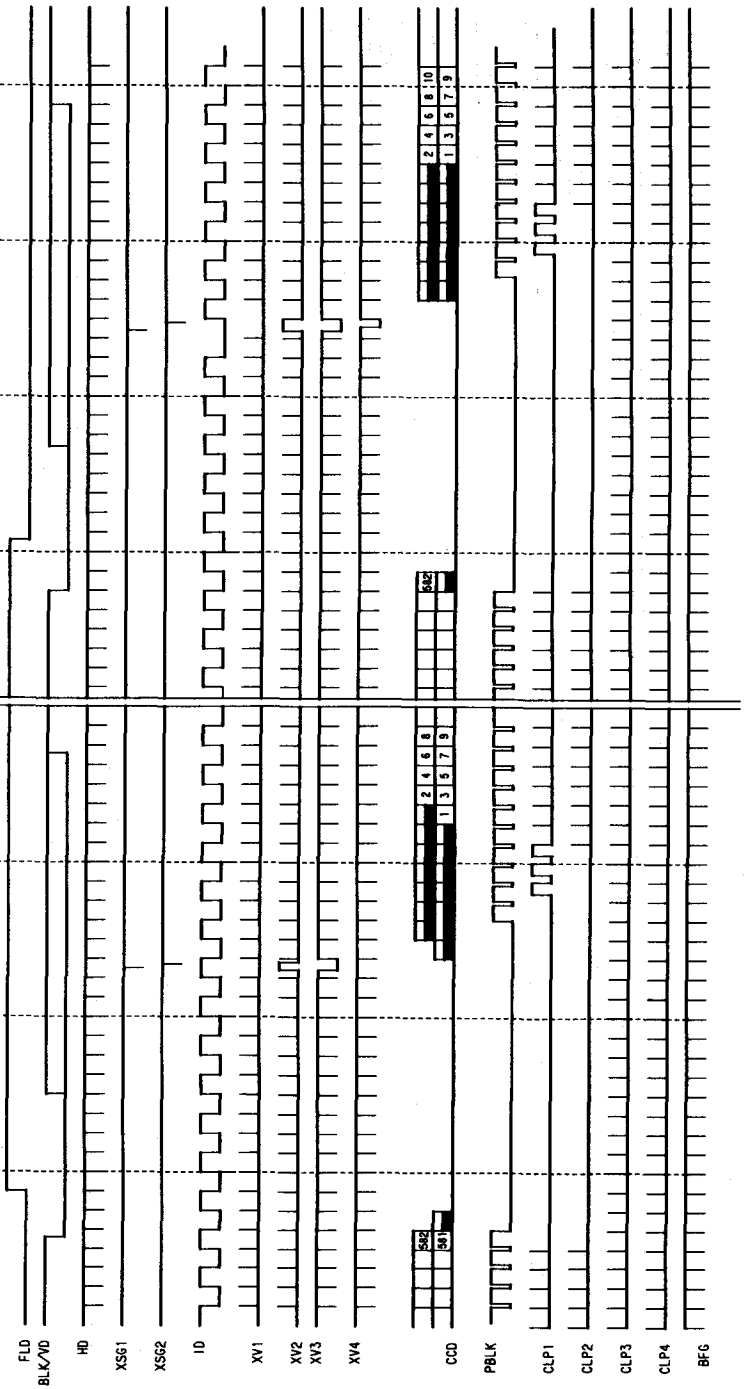
  However FF cannot be used as a load value.

Load value	Shutter speed (FLD)
FE_{16}	2
FD_{16}	4
⋮	⋮
01_{16}	508
00_{16}	510

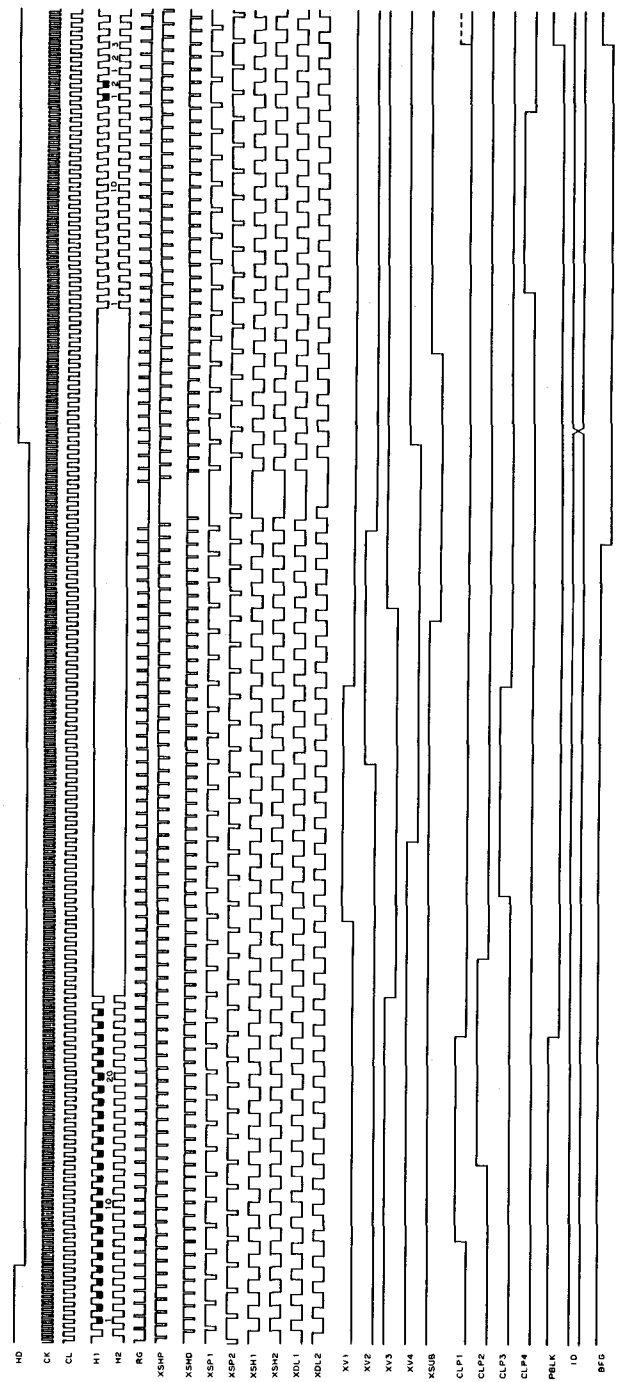
Time Chart (1) ⟨NTSC vertical direction⟩



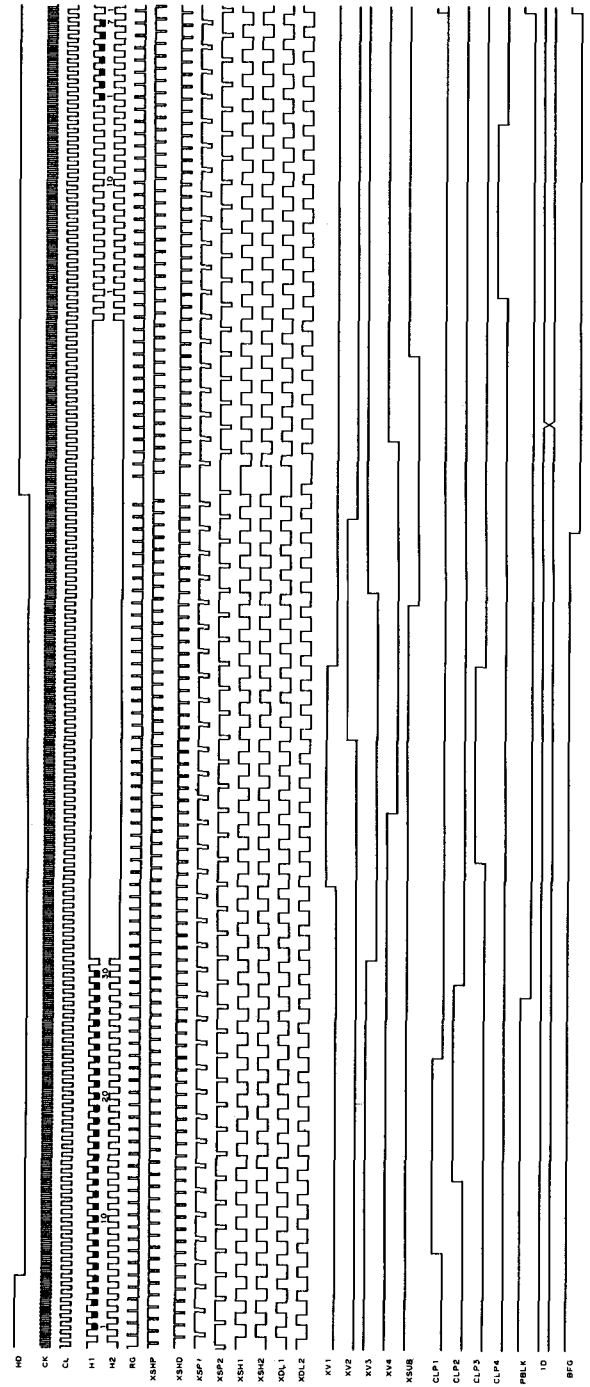
Time Chart (2) 〈PAL vertical direction〉



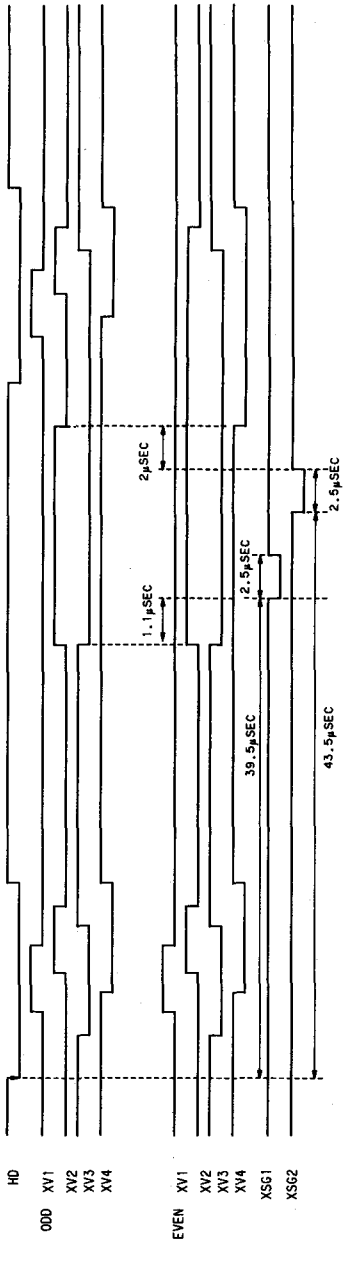
Time Chart (3) 〈NTSC horizontal direction〉



Time Chart (4) 〈PAL horizontal direction〉

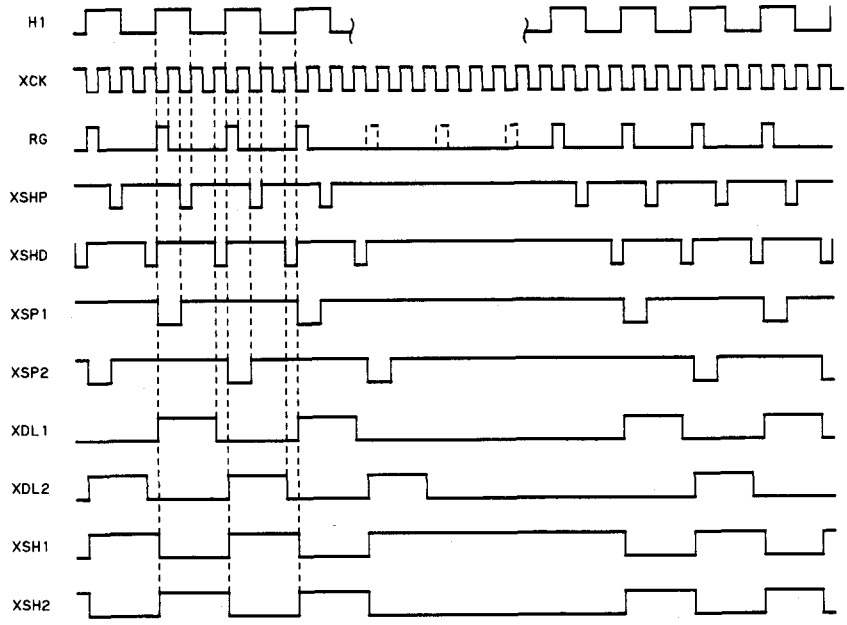


Time Chart (5) 〈XV1 to XV4 modulation〉

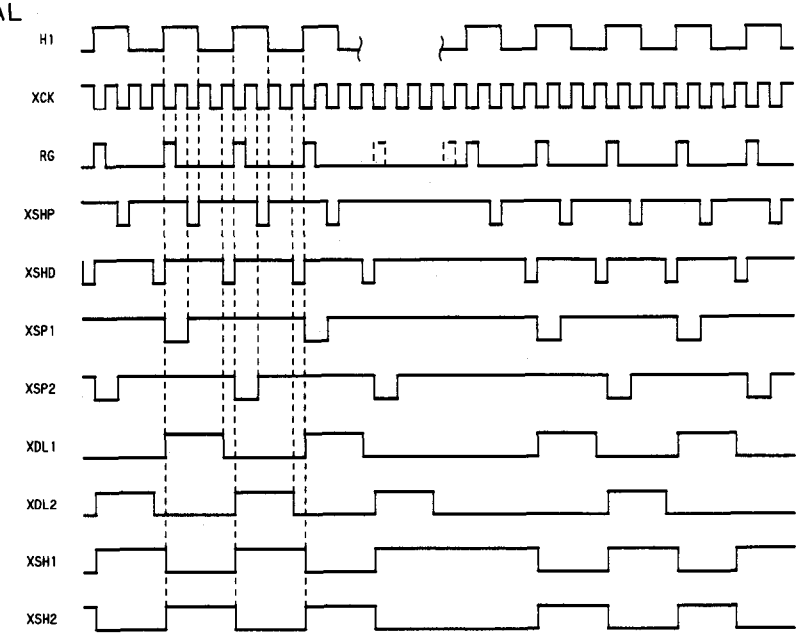


Time Chart (6) 〈High speed timing〉

NTSC

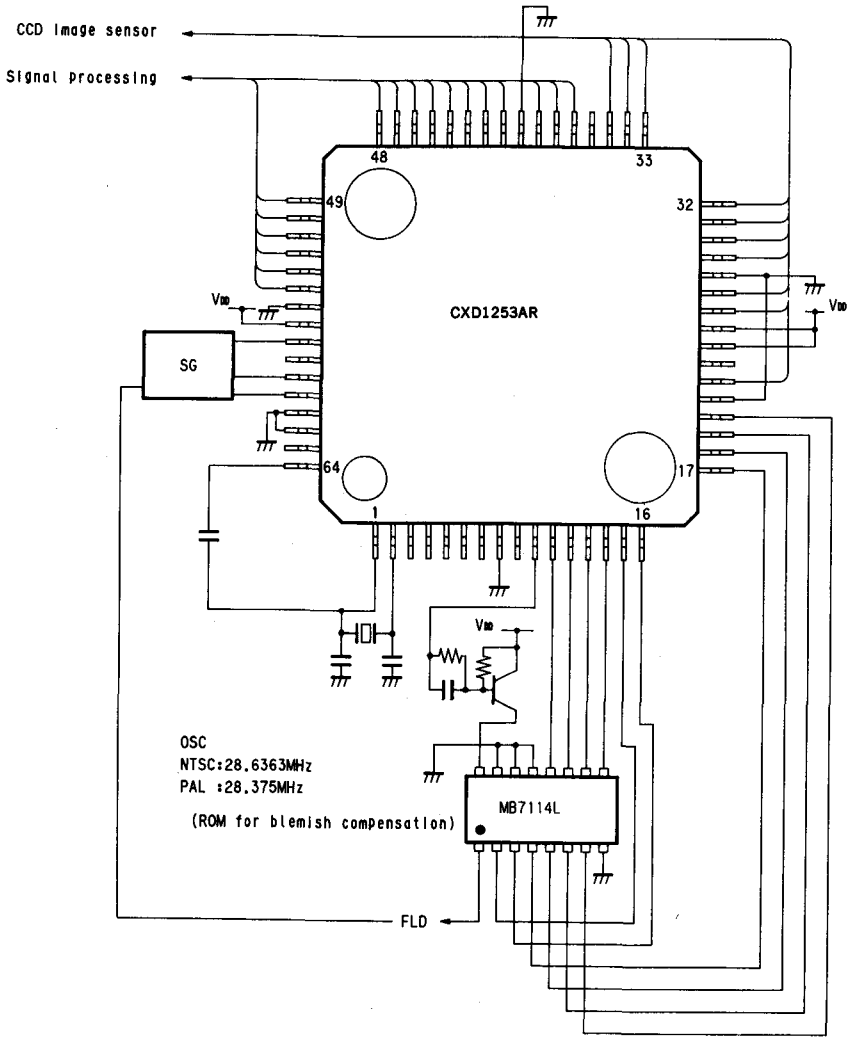


PAL



⟨Application Circuit⟩

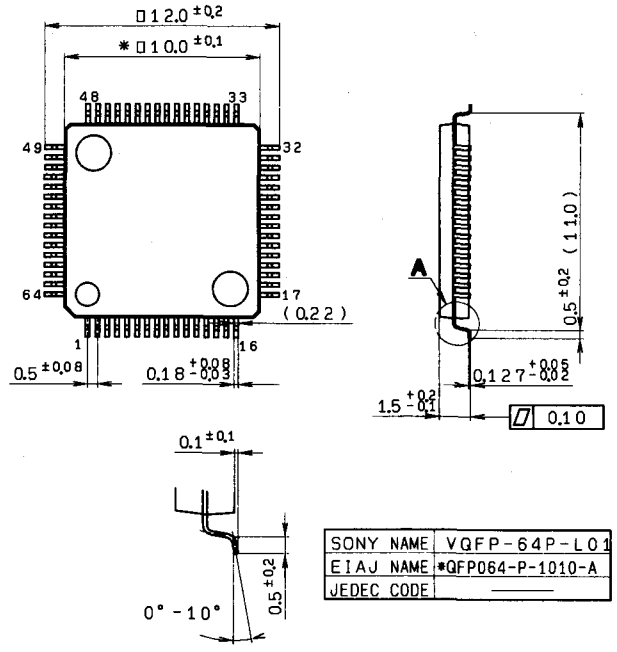
VQFP Package



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

CXD1253AR 64pin VQFP (Plastic) 0.3g

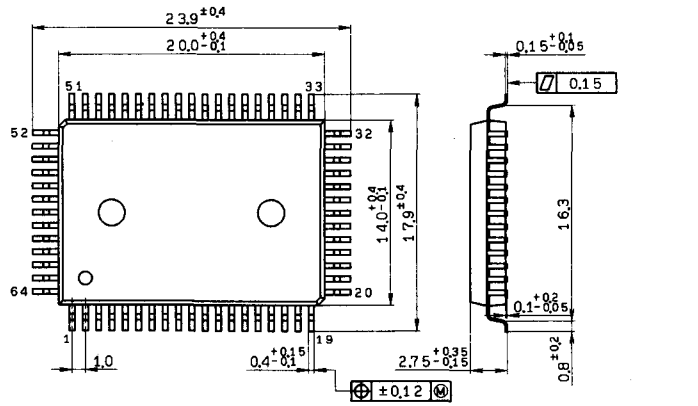


SONY NAME	VQFP-64P-L01
EIAJ NAME	*QFP064-P-1010-A
JEDEC CODE	———

Detailed diagram of A

Dimensions marked with * does not include resin residue.

CXD1253AQ 64pin QFP (Plastic) 1.5g



SONY NAME	QFP-64P-L01
EIAJ NAME	*QFP064-P-1420-A
JEDEC CODE	———

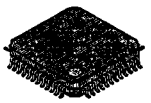
SONY CXD1255Q

Timing Signal Generator of CCD Camera Scanner (for ICX038AK/039AK)

Description

CXD1255Q is a CMOS-type LSI developed for use in the imager scanner for both ICX038AK/AL(NTSC) and ICX039AK/AL (PAL). This IC is used in conjunction with signal generators CXD1030M or CXD1158M.

48pin QFP (Plastic)



Features

- Generates pulses for driving imagers ICX038AK/AL and ICX039AK/AL
- Generates signal processing pulses for chequered coding
- NTSC (EIA)/PAL (CCIR) mode switchover.
- Field/frame accumulation
- Color and B/W mode
- Electronic shutter operation
- Built-in clock oscillation inverter

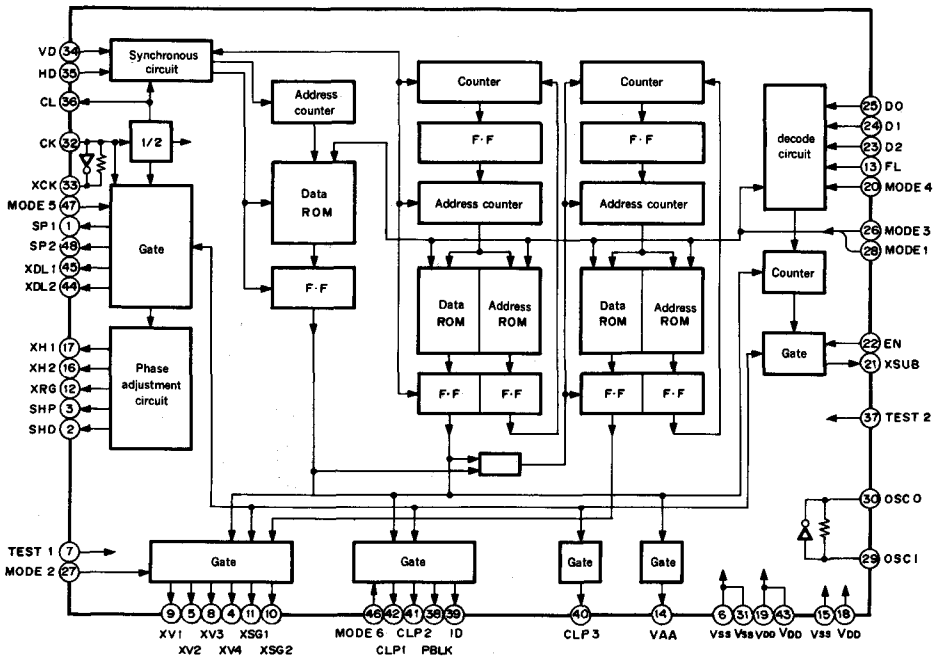
Applications

- CCD camera (NTSC/PAL)

Structure

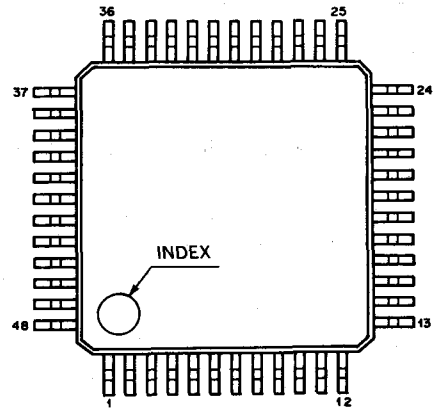
- Silicon gate CMOS

Block Diagram and Pin Configuration



E89219-HP

Pin Configuration (Top View)



Absolute Maximum Ratings (Ta=25°C)V_{SS}=0V

• Storage temperature	T_{stg}	−55 to +150	°C
• Operating temperature	T_{opr}	−20 to +75	°C
• Supply voltage	V_{DD}	V_{SS}−0.5 to +7.0	V
• Input voltage	V_I	V_{SS}−0.5 to V_{DD}+0.5	V
• Output voltage	V_O	V_{SS}−0.5 to V_{DD}+0.5	V

Recommended Operating Conditions

• Supply voltage	V_{DD}	+4.75 to +5.25	V

Pin Description

No.	Symbol	I/O	Description
1	SP1	O	Color separation S/H pulse (Note 1) L
2	SHD	O	CCD data output S/H pulse
3	SHP	O	CCD precharge level S/H pulse
4	XV4	O	Clock pulse for V register
5	XV2	O	Clock pulse for V register
6	V_{SS}	—	GND
7	TEST1	I	OPEN Pull-down resistance
8	XV3	O	Clock pulse for V register
9	XV1	O	Clock pulse for V register
10	XSG2	O	Sensor charge Read out pulse
11	XSG1	O	Sensor charge Read out pulse
12	XRG	O	CCD output reset pulse
13	FL	I	Electronic shutter flickerless, L: Flickerless, H: Normal
14	VAA	O	Vertical blanking cleaning pulse

No.	Symbol	I/O	Description
15	V_{SS}	—	GND
16	XH2	O	Clock pulse for H register
17	XH1	O	Clock pulse for H register
18, 19	V_{DD}	—	Power supply
20	MODE4	I	Input switchover of electronic shutter speed,L: Serial input, H: parallel input
21	XSUB	O	Sensor discharge pulse
22	EN	I	Electronic shutter ON/OFF, L: Shutter OFF, H: Shutter ON
23	D2	I	Electronic shutter speed switchover input
24	D1	I	Electronic shutter speed switchover input
25	D0	I	Electronic shutter speed switchover input
26	MODE3	I	NTSC/PAL switchover, L: NTSC, H: PAL
27	MODE2	I	Field/frame accumulation switchover, L: Field H: Frame
28	MODE1	I	(Note 2)
29	OSCI	I	Oscillation inverter input
30	OSCO	O	Oscillation inverter output
31	V_{SS}	—	GND
32	CK	I	Duty controlling inverter input
33	XCK	O	Duty controlling inverter output
34	VD	I	Vertical sync signal input
35	HD	I	Horizontal sync signal input
36	CL	O	Sync Generator clock output
37	TEST2	I	GND Pull-Down resistance
38	PBLK	O	Pre-blanking pulse
39	ID	O	Line identification pulse (Note 1) L
40	CLP3	O	Clamp pulse
41	CLP2	O	Clamp pulse
42	CLP1	O	Clamp pulse
43	V_{DD}	—	Power Supply
44	XDL2	O	Clock pulse for delay line (Note 1) SHDP
45	XDL1	O	Clock pulse for delay line (Note 1) L
46	MODE6	I	PBLK control pulse, L: Narrow H: Wide (Note 2)
47	MODE5	I	(Note 2)
48	SP2	O	Color separation S/H pulse (Note 1) L

Note 1) B/W mode output

Note 2) See Operation (p.5) for MODE1, 5, and 6 switchover.

Electrical Characteristics

DC characteristics

V_{DD}=5V±5%, V_{SS}=0V, T_{opr}=−20to+75°C

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage	H level	V_{IH}		0.7V_{DD}			V
	L level	V_{IL}				0.3V_{DD}	V
Input voltage (FL,EN,D0 to 2) * Schmitt trigger	H level	V_{T+}		0.8V_{DD}			V
	L level	V_{T-}				0.2V_{DD}	V
	Hysteresis	$V_{T+}-V_{T-}$		0.7	0.9		V
Output voltage	H level	V_{OH}	I_{OH}=−2mA	V_{DD}−0.5			V
	L level	V_{OL}	I_{OL}=4mA			0.4	V
Output voltage (Oscillation cell) (OSCO, XCK)	H level	V_{OH}	I_{OH}=−1mA	V_{DD}/2			V
	L level	V_{OL}	I_{OL}=1mA			V_{DD}/2	V
Input leak current			V_I=0V to V_{DD}	−10		10	μA
Oscillation cell feedback resistance		R_{FB}		500K	2M	5M	Ω

I/O capacity

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			9	pF
output pin	C_{OUT}			11	pF

Test condition: V_{DD}=V_I=0V, f=1MHz

Operation

CXD1255Q is provided with input pins for the setting of various modes. Related input pins are pulled up or pulled down beforehand inside the IC. Should an input pin be left open a certain mode is selected. (The pull up/down resistance value is approx. 100kΩ.)

〈For color usage〉

Pin	No.	Preset	Description	
			Input: "H"	Input: "L"
MODE1	28	L	Normal: "L"	
MODE2	27	L	Normal: "L"	
MODE3	26	L	PAL	NTSC
MODE4	20	H	(Electronic shutter speed setting)	
			Parallel input	Serial input
MODE5	47	L	Normal: "L"	
MODE6	46	L	(PBLK control pulse width switchover)	
			Wide	Narrow
EN	22	H	Electronic shutter ON	OFF
FL	13	H	Electronic shutter Normal	Flickerless
D2	23	H	Electronic shutter speed control (described later in detail)	
D1	24	H		
D0	25	H		

<For black-and-white usage>

Pin	No.	Preset	Description	
			Input: "H"	Input: "L"
MODE1	28	L	Normal: "H"	
MODE2	27	L	Frame accumulation	Field accumulation
MODE3	26	L	PAL	NTSC
MODE4	20	H	(Electronic shutter speed setting)	
			Parallel input	Serial input
MODE5	47	L	Normal "H"	
MODE6	46	L	Normal "H"	
EN	22	H	Electronic shutter ON	OFF
FL	13	H	Electronic shutter Normal	Flickerless
D2	23	H	Electronic shutter speed control (described later in detail)	
D1	24	H		
D0	25	H		

Operating conditions are shown in timing charts:

- NTSC vertical timing chart
- NTSC horizontal timing chart
- PAL vertical timing chart
- PAL horizontal timing chart

Electronic shutter speed control

	External pin							Internal register								Shutter speed XSUB ㉑
	P/S	EN	CRNT	FL	D2	D1	D0			EN	FL2	FL1	D2	D1	D0	
	↑⑳	↑㉒	↓㉖	↑⑬	↑㉓	↑㉔	↑㉕	D7	D6	D5	D4	D3	D2	D1	D0	
Parallel mode P/S=H	H	H		H	L	L	L									1/60 Note)
	H	H		H	L	L	H									1/125
	H	H		H	L	H	L									1/250
	H	H		H	L	H	H									1/500
	H	H		H	H	L	L									1/1000
	H	H		H	H	L	H									1/2000
	H	H		H	H	H	L									1/4000
	H	H		H	H	H	H									1/10000
	H	H	L	L												1/100
	H	H	H	L												1/120
	H	L														H
Serial mode P/S=L FL=H EN=H	L	H		H						H		H	L	L	L	1/60 Note)
	L	H		H						H		H	L	L	H	1/125
	L	H		H						H		H	L	H	L	1/250
	L	H		H						H		H	L	H	H	1/500
	L	H		H						H		H	H	L	L	1/1000
	L	H		H						H		H	H	L	H	1/2000
	L	H		H						H		H	H	H	L	1/4000
	L	H		H						H		H	H	H	H	1/10000
	L	H	H	H						H	H	L				1/100
	L	H	H	H						H	L	L				1/120
	L	H	L	H						H	H	L				1/100
	L	H	L	H						H	L	L				1/120
	L	H		H						L						H
Serial mode parallel CTL P/S=L	L	H	L	L												1/100
	L	H	H	L												1/120
	L	L														H

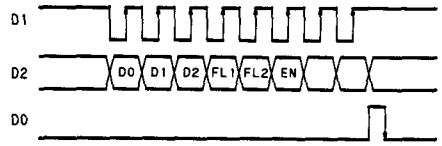
MODE 3 CR/NT
MODE 4 P/S

Abbreviations P : Parallel input S : Serial input
CR : PAL NT : NTSC

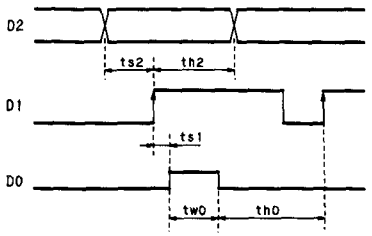
Note) 1/30 at accumulating NTSC frame.

AC Characteristics

In serial input mode (MODE4=L)



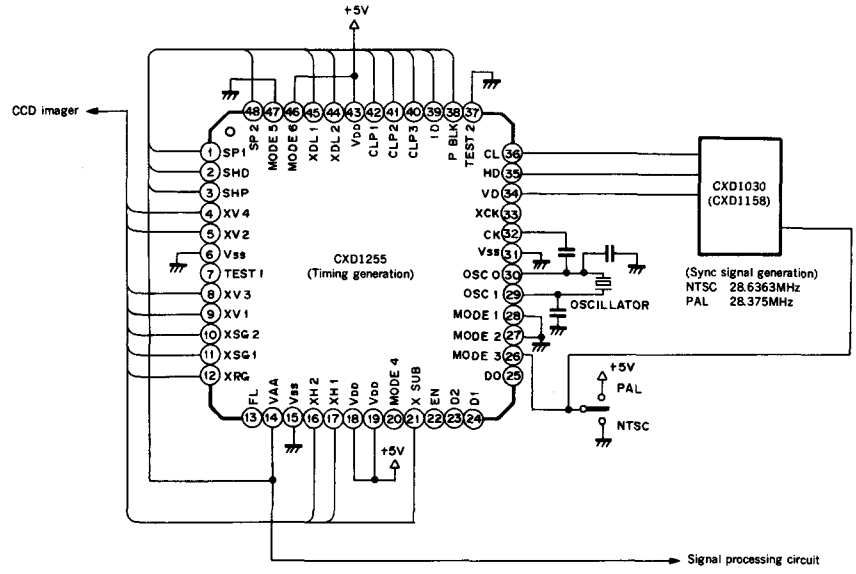
Mode setting in serial input



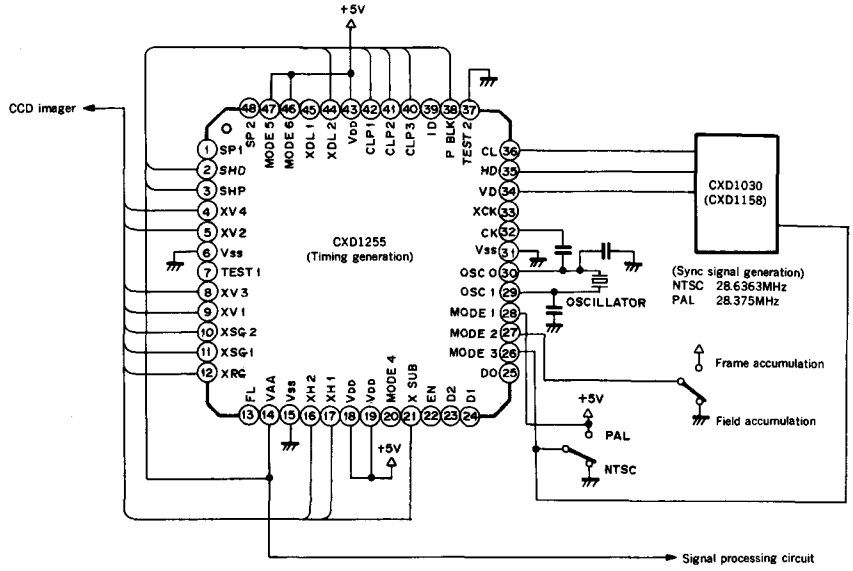
Symbol	Item	MIN
ts2	D2 set up time vs. D1 raising	20ns
th2	D2 hold time vs. D1 raising	20ns
ts1	D1 raising set up time vs. D0 raising	20ns
tw0	D0 pulse width	20ns
th0	D1 raising timing vs. D0 falling	20ns

Applicaiton circuit

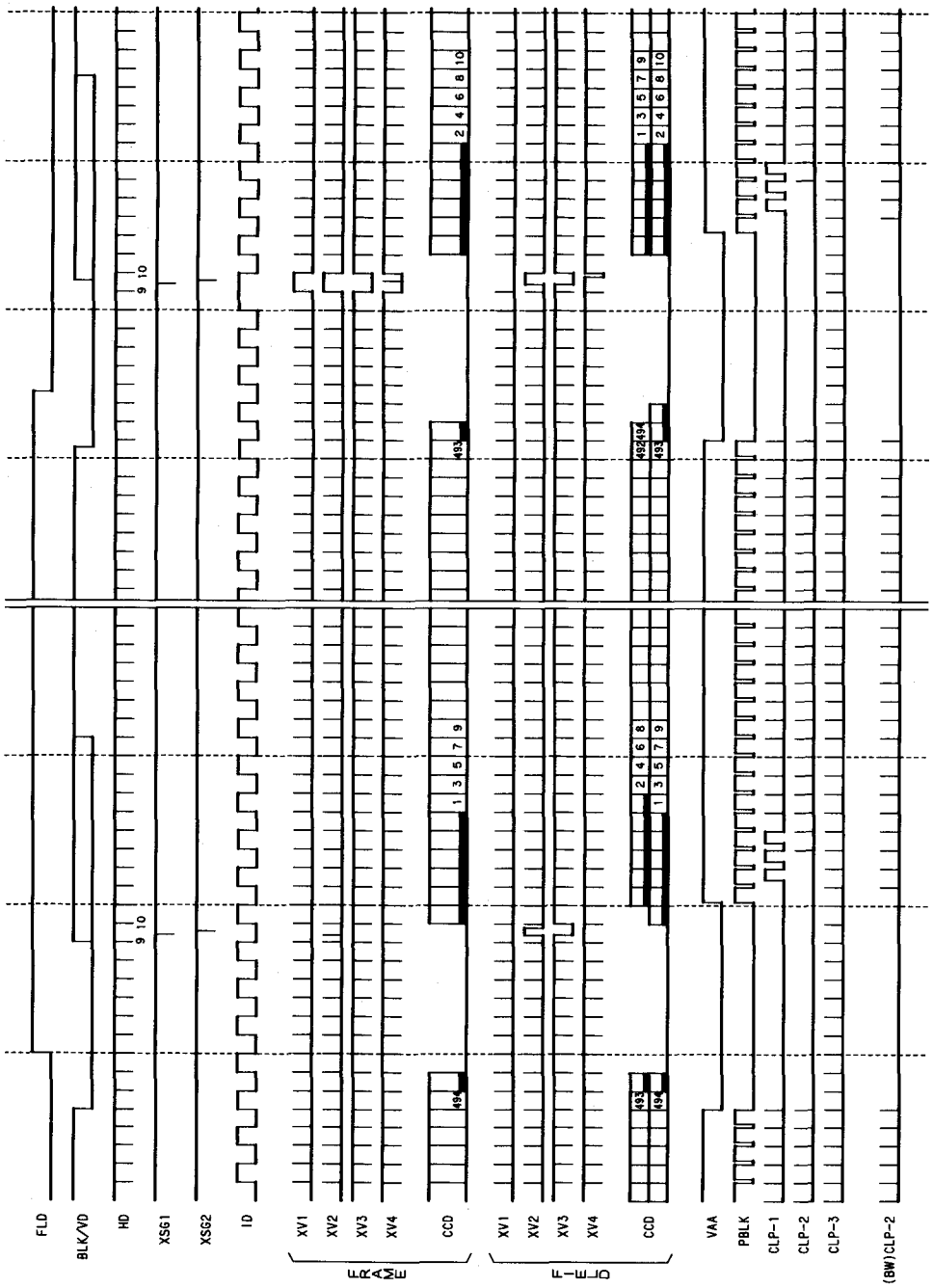
<Color mode>



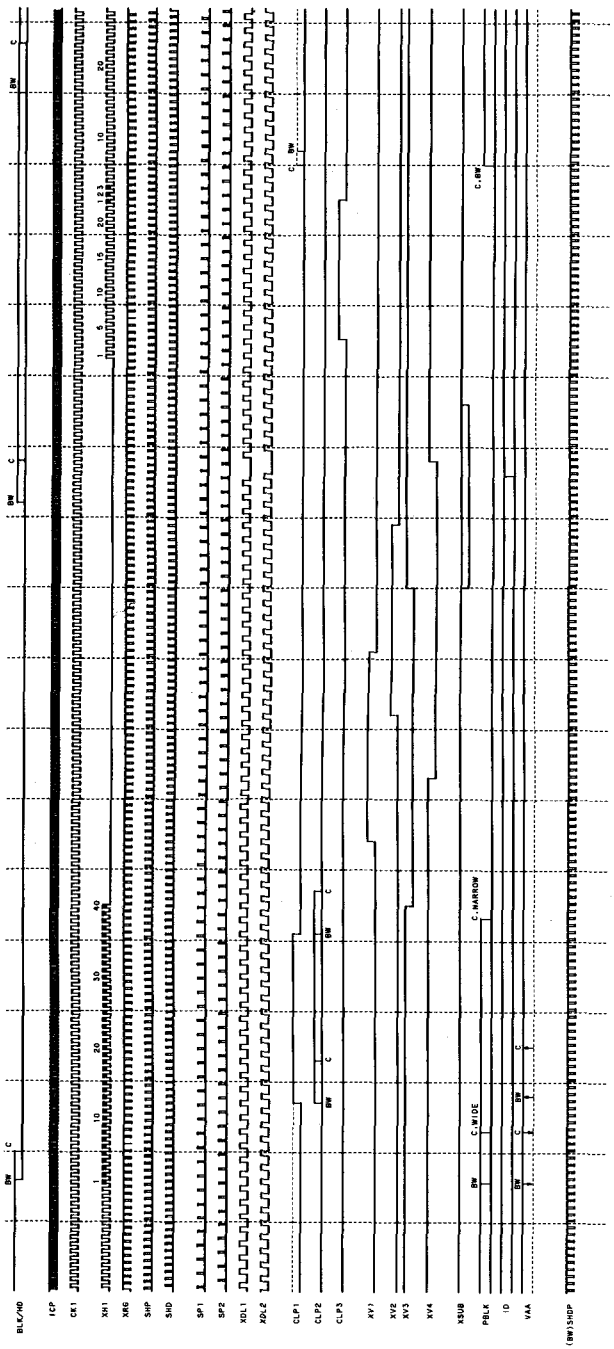
<B/W mode>



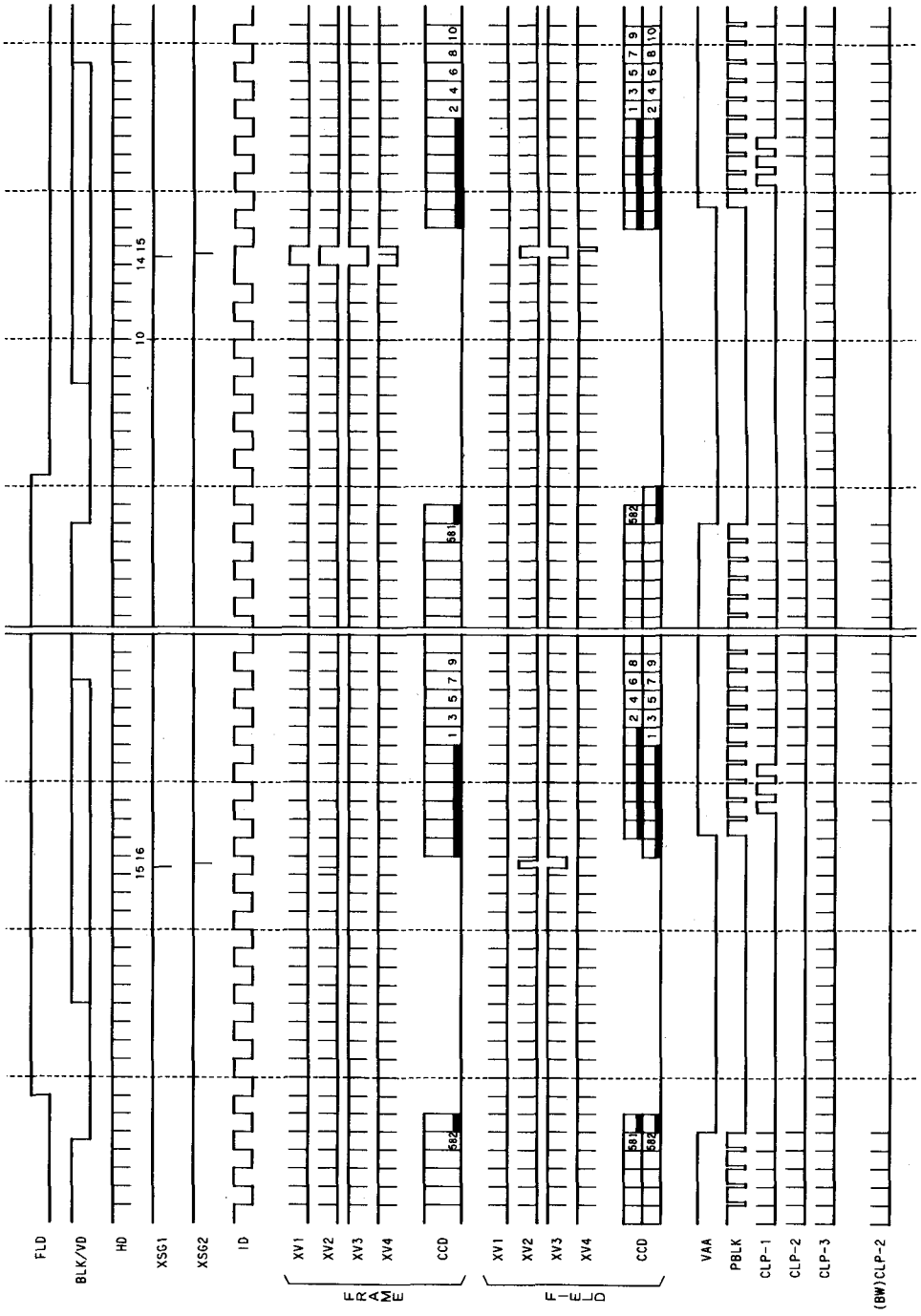
NTSC (EIA) Vertical



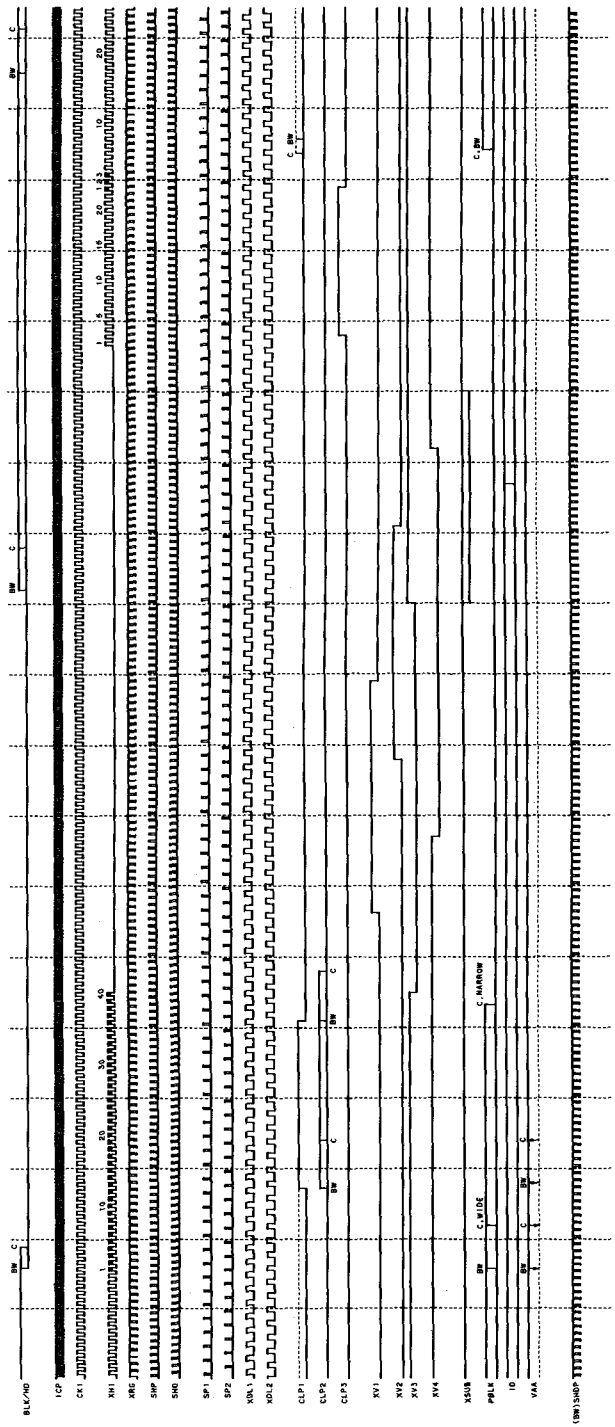
NTSC (EIA) Horizontal



PAL (CCIR) Vertical

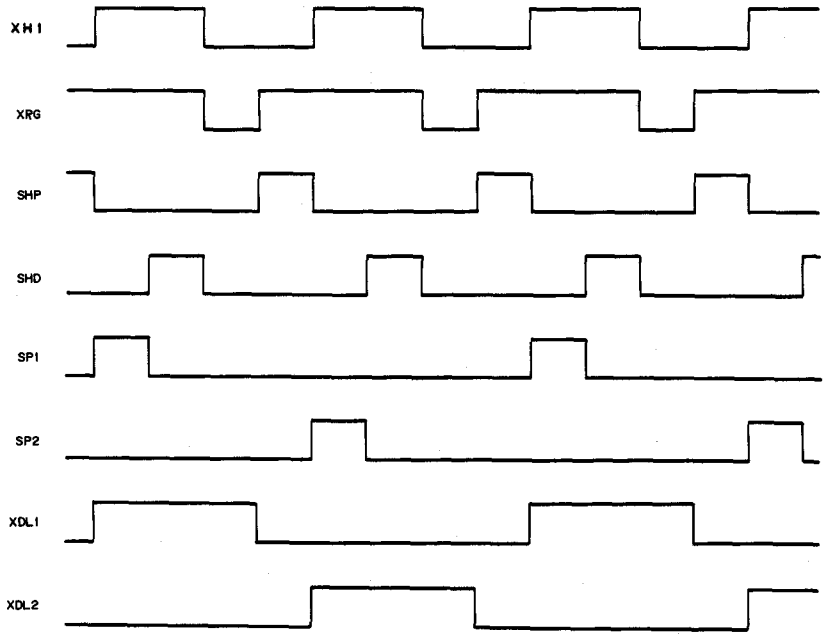


PAL (CCIR) Horizontal

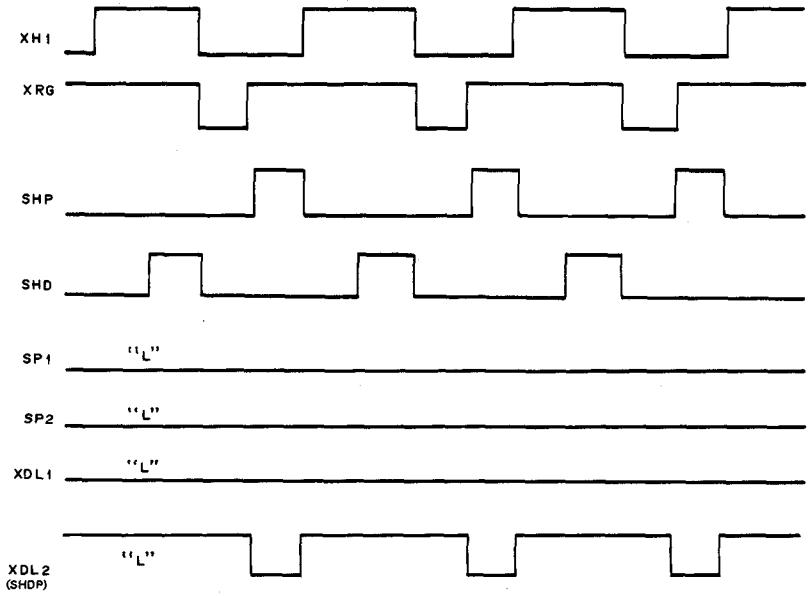


High-speed clock detailed timing

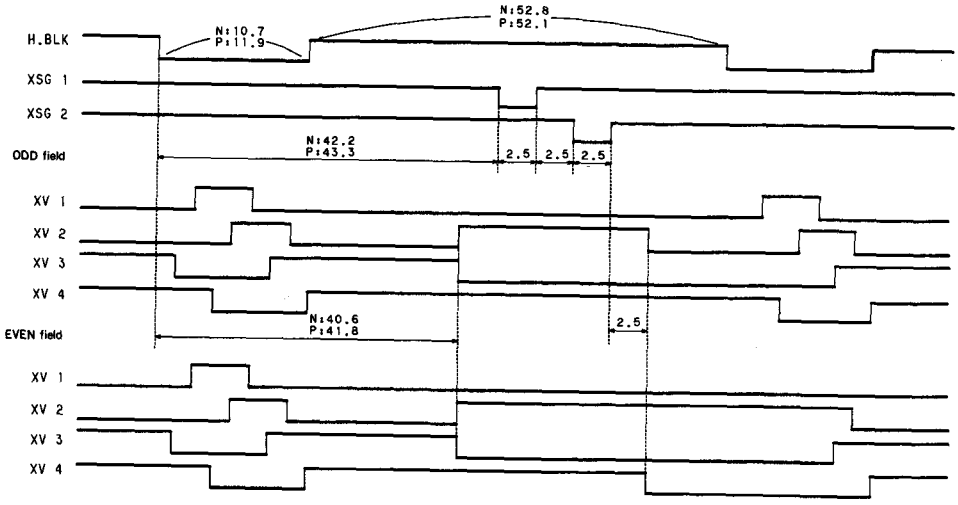
1. Color mode



2. B/W mode



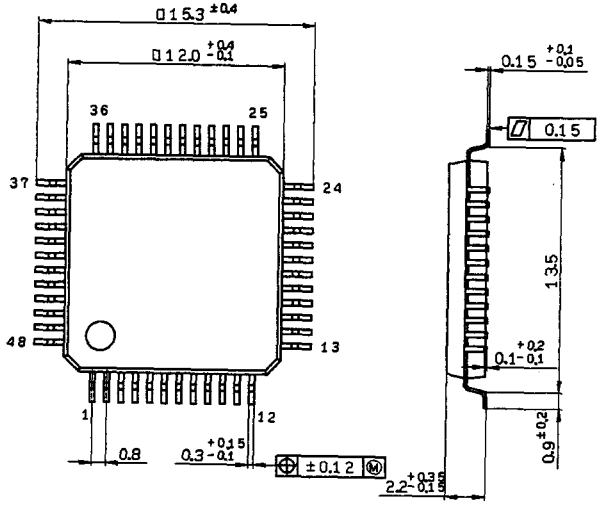
Readout period extension chart



Unit: μS

Package Outline Unit: mm

48pin QFP (Plastic) 0.6g



QFP-48P-L04

Timing setting for Electronic Shutter (CCD imager)

Description

The CXD1141M developed for CCD cameras is an LSI that sets the timing of electronic shutters.

Features

- Compatible with variable shutters (1/60 to 1/10000 sec)
- Compatible with flickerless
- Compatible with NSTC/PAL
- Mode setting compatible with serial/parallel

Function

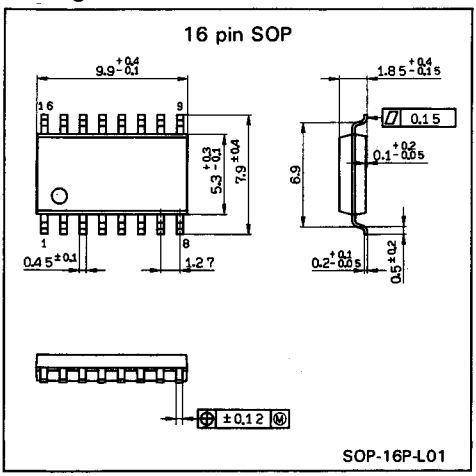
Sets the timing of electronic shutters.

Structure

Silicon gate CMOS

Package Outline

Unit: mm



Absolute Maximum Ratings (Ta = 25°C)

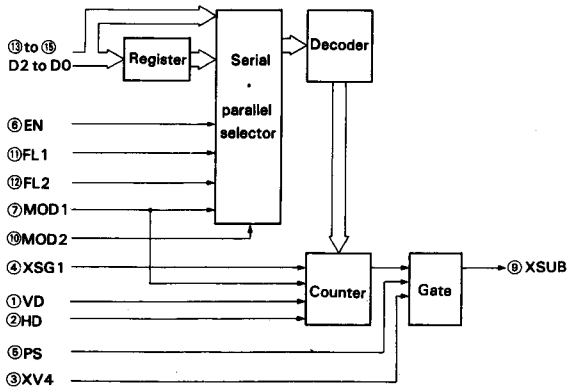
• Supply voltage	V_{DD}	Vss − 0.5* to + 7.0	V
• Input voltage	V_{IN}	Vss − 0.5* to V_{DD} + 0.5	V
• Output voltage	V_O	Vss − 0.5* to V_{DD} + 0.5	V
• Operating temperature	Topr	− 20 to + 75	°C
• Storage temperature	Tstg	− 55 to + 150	°C

* Vss = 0V

Recommended Operating Conditions

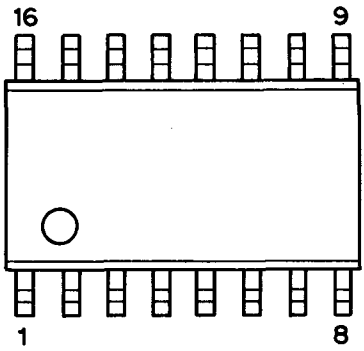
• Supply voltage	V_{DD}	4.5 to 5.5 (5.0V Typ.)	V
• Operating temperature	Topr	− 20 to + 75	°C

Block Diagram



70620-YA

Pin Configuration and Description (Top View)



No.	Symbol	I/O	Description
1	VD	I	Vertical drive pulse
2	HD	I	Horizontal drive pulse
3	XV4	I	Vertical scanning clock
4	XSG1	I	Sensor electric charge lead out pluse
5	PS	I	Power save pulse
6	EN	I	Enable signal L: Normal mode, H: Electronic shutter mode
7	MOD1	I	Mode switching L: PAL, H: NTSC
8	V_{SS}	—	GND
9	XSUB	O	Electric charge sweep out pulse
10	MOD2	I	Mode switching L: serial input H: Parallel input
11	FL1	I	Mode switching L: flickerless H: Normal
12	FL2	I	Mode switching L: 60Hz H: 50Hz
13	D2	I	Shutter speed setting
14	D1	I	Shutter speed setting
15	D0	I	Shutter speed setting
16	V_{DD}	—	+5V

Electrical Characteristics

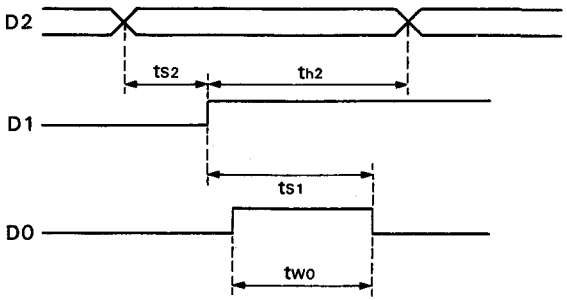
DC characteristics V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, Topr = −20 to +75°C

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply current		I_{DD}				2	mA
		I_{DDS}	Static state*1	0		0.1	mA
Output voltage	H level	V_{OH}	I_{OH} = −1.5mA	V_{DD} − 0.5		V_{DD}	V
	L level	V_{OL}	I_{OL} = 4.0mA	V_{SS}		0.4	V
Input voltage	H level	V_{IH}		0.7V_{DD}			V
	L level	V_{IL}				0.3V_{DD}	V
Input threshold voltage	H level	V_{IH}		0.7V_{DD}	3.0		V
	L level	V_{IL}			2.0	0.3V_{DD}	V
	Hysteresis	Vh		0.5			V
Input leak current		I_{LI}	V_I = 0V *2	−20	−50	−120	μA

Note) *1 V_{DD} is applied to all input pins.
*2 Pull up resistance is provided to all input pins.

AC characteristics

For serial input mode



Item	Symbol	Min.	Typ.	Max.	Unit
D2 set up time with regards to D1 rising edge.	ts2	20			ns
D2 hold time with regards to D1 rising edge.	th2	20			ns
D1 rising edge set up time with regards to D0 Falling edge.	ts1	20			ns
D0 pulse width	two	20			ns

Input/Output Capacitance

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			8	pF
Output pin	C_{OUT}			8	pF

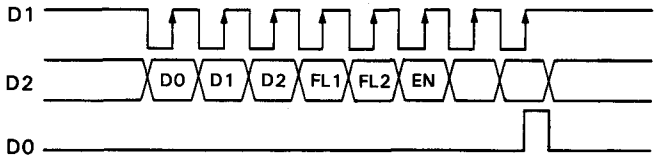
Testing conditions V_{DD} = V_I = 0V, fM = 1MHz

Mode setting

1) Parallel input mode (MOD2 = H)

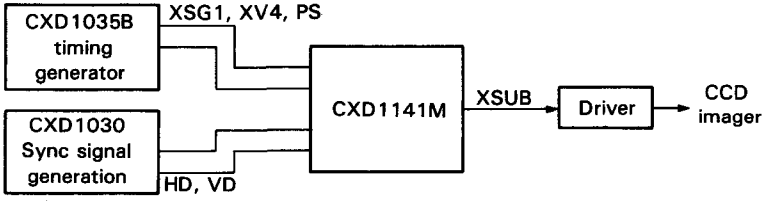
EN	MOD1	MOD2	FL1	FL2	D2	D1	D0	Shutter speed	Theoretical value
H	H	H	H		L	L	L	1/60	1/60
H	H	H	H		L	L	H	1/125	1/125
H	H	H	H		L	H	L	1/250	1/252
H	H	H	H		L	H	H	1/500	1/499
H	H	H	H		H	L	L	1/1000	1/1013
H	H	H	H		H	L	H	1/2000	1/2088
H	H	H	H		H	H	L	1/4000	1/4450
H	H	H	H		H	H	H	1/10000	1/10256
H	L	H	H		L	L	L	1/60	1/60
H	L	H	H		L	L	H	1/125	1/125
H	L	H	H		L	H	L	1/250	1/250
H	L	H	H		L	H	H	1/500	1/495
H	L	H	H		H	L	L	1/1000	1/1005
H	L	H	H		H	L	H	1/2000	1/2070
H	L	H	H		H	H	L	1/4000	1/4403
H	L	H	H		H	H	H	1/10000	1/10090
H	H		L	H				1/100	1/100
H	H		L	L				1/120	1/120
H	L		L	H				1/100	1/100
H	L		L	L				1/120	1/120
L								NORMAL	

2) Serial input mode (MOD2 = L)



D2 data is latched at register with the rising edge of D1 and shifted inside with the D0.

Application Circuit



SONY

CXD1251Q

Timing Generator for Blemish Compensation

Description

CXD1251Q is a CMOS LSI IC used for blemish compensation in CCD imagers such as ICX026AK/AL, ICX022AK (NTSC), ICX027AK/AL, ICX024AK (PAL), CCD blemishes can be compensated at a rate of up to 10 per field.

Features

- Generation of blemish compensation pulses.
- When used for blemish compensation in ICX 026AK/AL and ICX027AK/AL it is combined with scanning IC's CXD1156R (Q).
- For the blemish compensation in ICX022AK or 024AK it is combined with scanning IC CXD1149R.

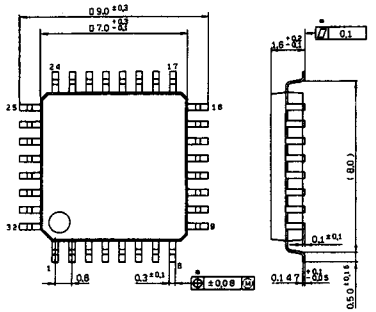
Structure

CMOS LSI

Package Outline

Unit : mm

32 pin QFP (Plastic)



QFP-32P-L01

Application

- Blemish compensation in CCD imagers

Absolute Maximum Ratings (Ta = 25°C)

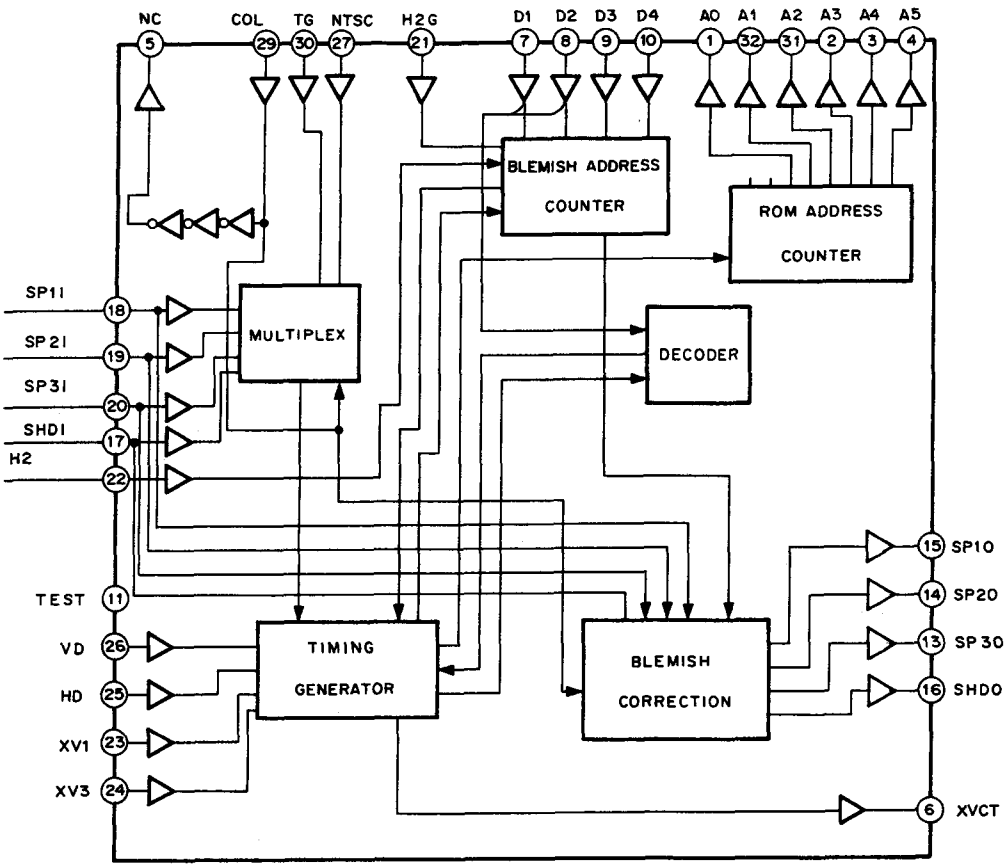
• Supply voltage	V_{CC}	V_{SS} − 0.5 to + 7.0	V
• Input voltage	V_I	V_{SS} − 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} − 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	− 20 to + 75	°C
• Storage temperature	Tstg	− 55 to + 150	°C

Recommended Operating Conditions

• Supply voltage	V_{CC}	4.75 to 5.25	V
• Operating temperature	Topr	− 20 to + 75	°C

80642 – ST

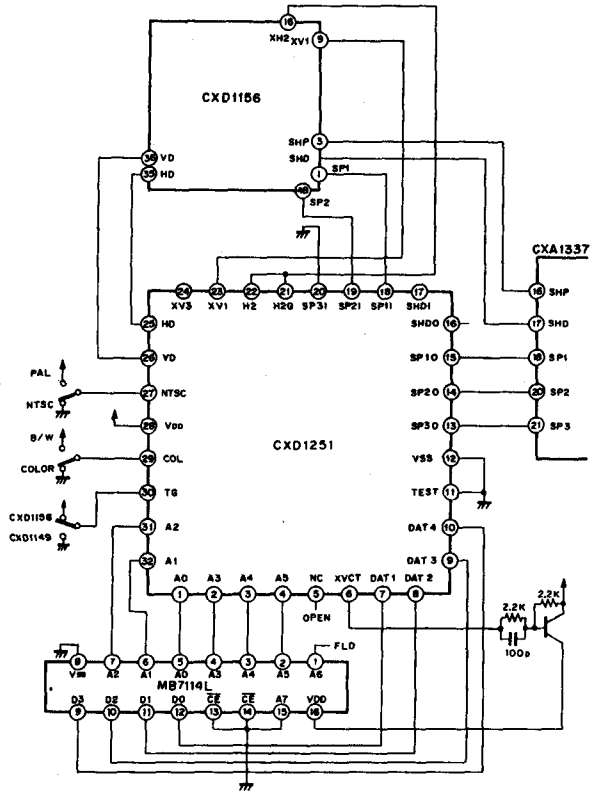
Block Diagram



Pin Description

No.	Symbol	I/O	Description
1	A0	O	Address output pin for external ROM
2	A3	O	Address output pin for external ROM
3	A4	O	Address output pin for external ROM
4	A5	O	Address output pin for external ROM
5	NC	—	
6	XVCT	O	Control output pin for external ROM supply
7	DAT1	I	Data input pin from external ROM
8	DAT2	I	Data input pin from external ROM
9	DAT3	I	Data input pin from external ROM
10	DAT4	I	Data input pin from external ROM
11	TEST	I	Test pin. Normally GND
12	V_{SS}	—	
13	SP3O	O	S/H pulse output pin for blemish compensation
14	SP2O	O	S/H pulse output pin for blemish compensation
15	SP1O	O	S/H pulse output pin for blemish compensation
16	SHDO	O	S/H pulse output pin for blemish compensation
17	SHDI	I	S/H pulse input pin for blemish compensation
18	SP1I	I	S/H pulse input pin for blemish compensation
19	SP2I	I	S/H pulse input pin for blemish compensation
20	SP3I	I	S/H pulse input pin for blemish compensation
21	H2G	I	CCD horizontal scanning clock input pin
22	H2	I	CCD horizontal scanning clock input pin
23	XV1	I	CCD vertical scanning clock input pin
24	XV3	I	CCD vertical scanning clock input pin
25	HD	I	Horizontal drive pulse input pin from sync generator IC
26	VD	I	Vertical drive pulse input pin from sync generator IC
27	NTSC	I	NTSC/PAL Mode select pin H : PAL L : NTSC
28	V_{DD}	I	Supply
29	COL	I	Color/B/W mode select pin H : B/W L : Color
30	TG	I	TG mode select pin H : 1149R L : 1156R
31	A2	O	Address output pin for external ROM
32	A1	O	Address output pin for external ROM

Peripheral Circuit (CXD1156 checkers in use)



Electrical Characteristics

DC characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage	V_{IHC}		$0.7V_{DD}$			V
	V_{ILC}				$0.3V_{DD}$	V
Input voltage	V_{IH}	SP1I, SP2I, SP3I, SHDI	2.8			V
	V_{IL}				0.6	V
Output voltage	V_{OH}	$I_{OH} = -2mA$	$V_{DD} - 0.5$			V
	V_{OL}	$I_{OL} = 4mA$			0.4	V

I/O capacity

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input pin	C_{IN}				9	pF
Output pin	C_{OUT}				11	pF

Connection Diagram for Respective Modes

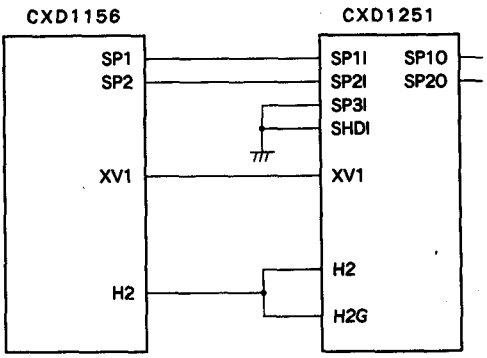


Fig. 1. With CXD1156 checkers in use

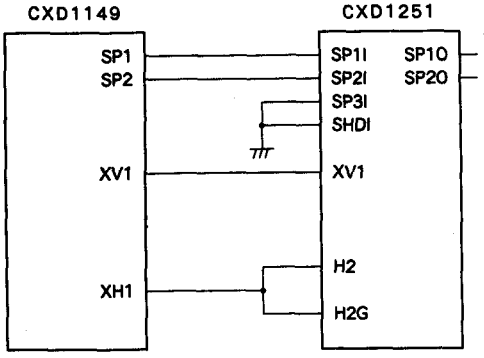


Fig. 2. With CXD1149 checkers in use

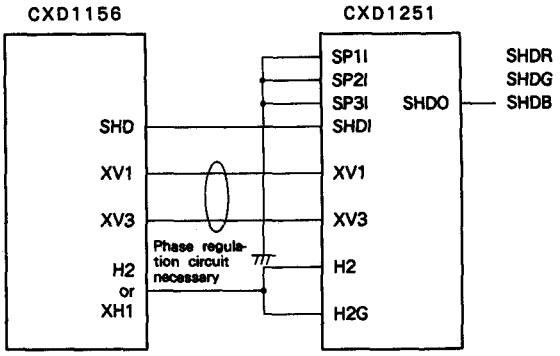


Fig. 3. CXD1156 : BW in use

SONY

CXB0026AM

CCD Driver

Description

CXB0026AM is a special version of CXB0026M with the following improvements:

1) High frequency operation ability.
2) Improved output voltage amplitude (voltage usage ratio).

Other specifications match those of CXB0026M.

Features

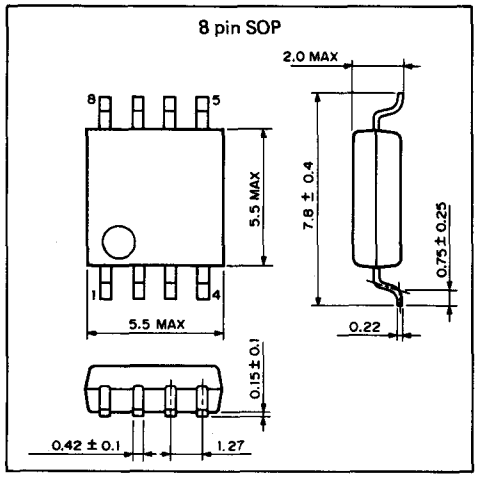
- High frequency operation ability.
- Improved output voltage amplitude.
- TTL compatible input.
- High output current drive.
- 2.0 mW low consumption when input at low level.

Structure

Bipolar silicon monolithic IC

Package Outline

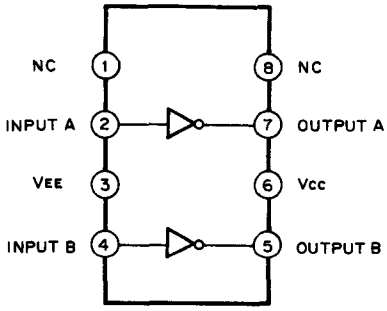
Unit: mm



Absolute Maximum Ratings (Ta=25°C)

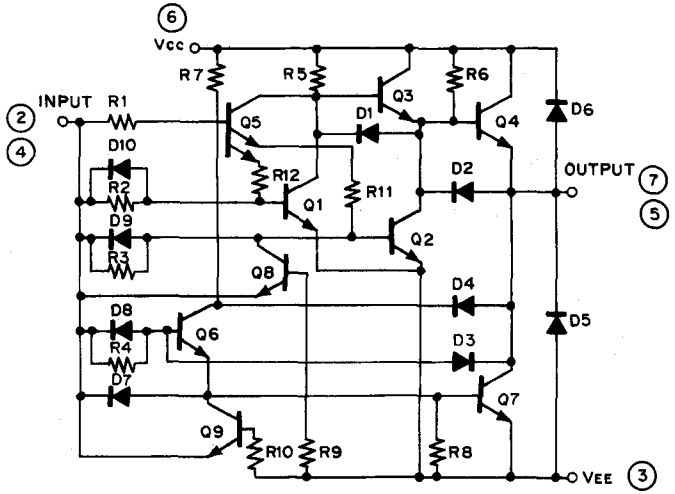
• Supply voltage	V_{CC-EE}	22	V
• Input current	I_I	100	mA
• Input voltage	V_I	V_{EE}+5.5	V
• Instant output current	Iopk	±1.5	A
• Junction temperature	T_J	+150	°C
• Operating temperature	Ta	0 to 70	°C
• Storage temperature	Tstg	−65 to 150	°C
• Allowable power dissipation (Ta=70°C, PC Board Mount)	P_D	400	mW

Pin Configuration



70847A-ST

Equivalent Circuit



Electrical Characteristics

Ta=0 to 70°C, $V_{CC}-V_{EE}$=10 to 20V, C_L=1000 pF, Ta=25°C (Typ.)

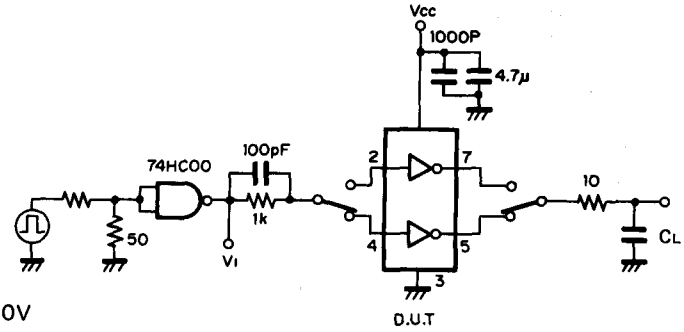
Item	Symbol	Min.	Typ.	Max.	Unit
H level input voltage $V_O=V_{EE}+1.0$ Vdc	V_{IH}	$V_{EE}+2.0$	$V_{EE}+1.5$	–	V
H level input current $V_I-V_{EE}=2.4$ Vdc, $V_O=V_{EE}+1.0$ Vdc	I_{IH}	–	10	15	mA
L level input $V_O=V_{CC}-1.0$ Vdc	V_{IL}	–	$V_{EE}+0.6$	$V_{EE}+0.4$	V
L level input current $V_I-V_{EE}=0$ Vdc, $V_O=V_{CC}-1.0$ Vdc	I_{IL}	–	−0.005	−10	mA
Output voltage at L level input $V_I-V_{EE}=0.4$ Vdc	V_{OH}	$V_{CC}-1.0$	$V_{CC}-0.7$	–	V
Output voltage at H level input $V_I-V_{EE}=2.4$ Vdc	V_{OL}	–	$V_{EE}+0.5$	$V_{EE}+1.0$	V
Supply current at ON (1 circuit) $V_{CC}-V_{EE}=20$ Vdc, $V_I-V_{EE}=2.4$ Vdc	I_{CCL}	–	30	40	mA
Supply current at OFF (1 circuit) $V_{CC}-V_{EE}=20$ Vdc, $V_I-V_{EE}=0$ Vdc	I_{CCH}	–	10	100	μA

Switching Characteristics

V_{CC}=7V, V_{EE}=0V, Ta=25°C, C_L=270P

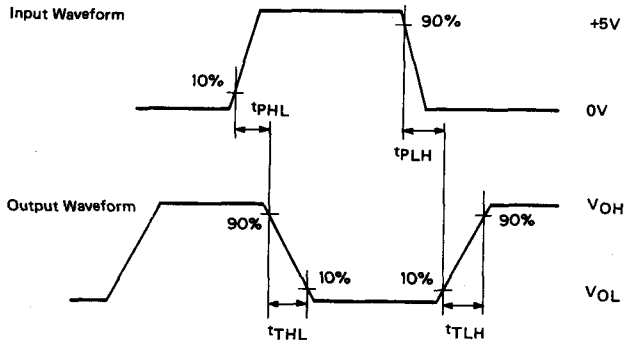
Item	Symbol	Min.	Typ.	Max.	Unit
Clock level	V_{OH}–V_{OL}	V_{CC}–0.5	–	V_{CC}	V
Propagation time (H→L)	t_{PHL}	4.75	–	6.75	ns
Propagation time (L→H)	t_{PLH}	–	–	14	ns
Transition time (H→L)	t_{THL}	–	–	11	ns
Transition time (L→H)	t_{TLH}	–	–	17	ns

Characteristics Test Circuit



* V_I=5.0V
f=14 MHz
t_{TLH}=t_{THL}≦8ns
Duty 50%

I/O Waveforms



Vertical clock driver for CCD imagers

Description

The CXA1065M is a bipolar IC developed to drive the vertical shift register of CCD imagers (ICX022 etc.).

It is composed of seven drivers that can drive large capacitors with wide voltage amplitude. A suppressing function of coupling between phases reduces blooming and smear to make this IC ideal for vertical clock driving of CCD imaging devices.

Features

- Almost all functions required for vertical clock driving of CCD imager are provided.
- Negative voltage source is not needed.
- Suppressing function of coupling between phases.
- Wide output amplitude — Output voltage amplitude is almost equal to supply voltage.
- Wide operating voltage range −5.5 to +25 V
- Low power consumption with the built-in power-saving circuit — 116 mW Typ. when the ICX022 equivalent circuit load is driven.

Structure

Silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C)

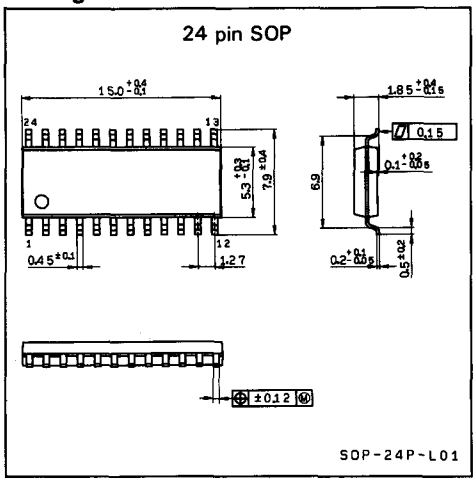
• Supply voltage	$V_{CC}1$	6	V
	$V_{CC}2$-1	27	V
	$V_{CC}2$-2	27	V
	$V_{CC}2$-3	27	V
	$V_{CC}2$-4	27	V
	$V_{CC}3$	27	V
	$V_{CC}4$	27	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−55 to +150	°C
• Allowable power dissipation	P_D	560	mW

Recommended Operating Conditions

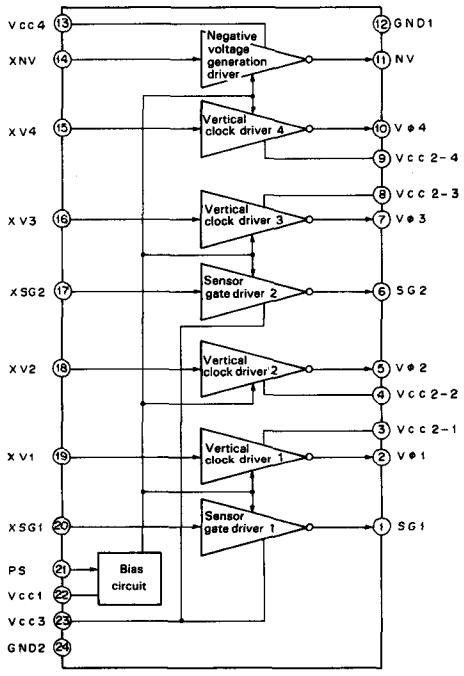
$V_{CC}1$	4.5 to 5.5	V
$V_{CC}2$-1	5.5 to 25	V
$V_{CC}2$-2	5.5 to 25	V
$V_{CC}2$-3	5.5 to 25	V
$V_{CC}2$-4	5.5 to 25	V
$V_{CC}3$	5.5 to 25	V
$V_{CC}4$	5.5 to 25	V

Package Outline

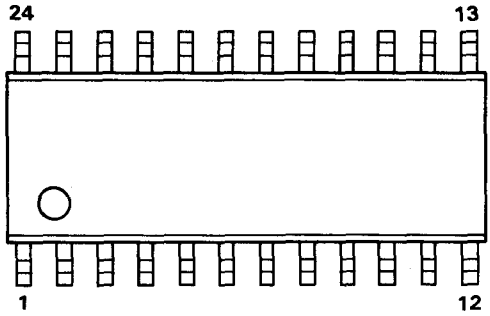
Unit: mm



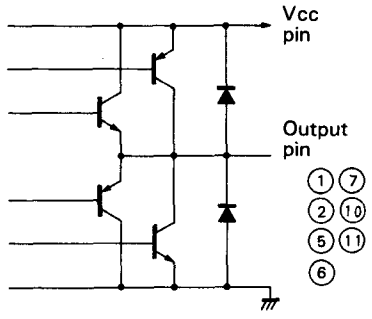
Block Diagram

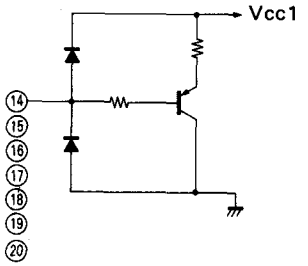
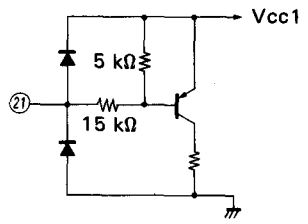


Pin Configuration (Top View) and Description



No.	Symbol	Description	Equivalent circuit
		Function of each driver is inverter. Truth table: Input L → Output H; Input H → Output L	
1	SG1	Sensor gate driver 1	Output pins
2	Vφ1	Vertical clock driver 1	
5	Vφ2	Vertical clock drivr 2	
6	SG2	Sensor gate driver 2	
7	Vφ3	Vertical clock driver 3	
10	Vφ4	Vertical clock driver 4	
11	NV	Negative voltage generation driver	
3	Vcc2-1	Vertical clock driver 1	Vcc pins
4	Vcc2-2	Vertical clock driver 2	
8	Vcc2-3	Vertical clock driver 3	
9	Vcc2-4	Vertical clock driver 4	
13	Vcc4	Negative voltage generation driver	
23	Vcc3	Sensor gate driver 1, 2	
12	GND1	GND	
24	GND2		



No.	Symbol	Description		Equivalent circuit
14	XNV	Negative voltage generation driver	Input *pin*	
15	XV4	Vertical clock driver 4		
16	XV3	Vertical clock driver 3		
17	XSG2	Sensor gate driver 2		
18	XV2	Vertical clock driver 2		
19	XV1	Vertical clock driver 1		
20	XSG1	Sensor gate driver 1		
21	PS	Input pin for the power-saving signal (For the power-saving function, refer to the Description of Functions.)		
22	Vcc1	Power supply of the bias circuit.		

Electrical Characteristics

DC characteristics

Ta = 25°C

V_{CC1} = 5V, $V_{CC2\text{-}1}$ = 12V, $V_{CC2\text{-}2}$ = 12V, $V_{CC2\text{-}3}$ = 12V, $V_{CC2\text{-}4}$ = 12V, V_{CC3} = 12V, V_{CC4} = 12V

With outputs open

Parameter			Symbol	Input condition (Blank 0V, H 5V)								Min.	Typ.	Max.	Unit
				PS	XV1	XV2	XV3	XV4	XSG1	XSG2	XNV				
Input current into PS pin		Input current low level	I_{ILPS}									−500	−270		μA
		Input current high level	I_{IHPS}	H									0.03	15	μA
Input current into 7 drivers	Input current low level	XV1	I_{ILXV1}									−15	−2.5		μA
		XV2	I_{ILXV2}												
		XV3	I_{ILXV3}	H											
		XV4	I_{ILXV4}	H											
		XSG1	I_{ILXSG1}	H											
		XSG2	I_{ILXSG2}	H											
		XNV	I_{ILXNV}												
	Input current high level	XV1	I_{IHXV1}		H								0.03	15	μA
		XV2	I_{IHXV2}			H									
		XV3	I_{IHXV3}				H								
		XV4	I_{IHXV4}					H							
		XSG1	I_{IHXSG1}						H						
		XSG2	I_{IHXSG2}							H					
		XNV	I_{IHXNV}								H				
Input voltage	Low level		V_{IL}											0.05	V
	High level		V_{IH}									4.95			V

Parameter		Symbol	Input condition (Blank 0V, H 5V)								Min.	Typ.	Max.	Unit
			PS	XV1	XV2	XV3	XV4	XSG1	XSG2	XNV				
DC supply cuttent of bias circuit at V_{CC1}	PS: L All inputs: L	$I_{CC1\ LL}$									1.5	3.5	5.5	mA
	PS: L All inputs: H	$I_{CC1\ LH}$		H	H	H	H	H	H	H	0.5	1.7	3.0	mA
	PS: H All inputs: L	$I_{CC1\ HL}$	H								1.5	3.2	5.0	mA
	PS: H All inputs: H	$I_{CC1\ HH}$	H	H	H	H	H	H	H	H	0.5	1.3	2.5	mA
DC supply current of vertical clock driver 1 at $V_{CC2\text{-}1}$	PS: L XV1: L	$I_{CC2\text{-}1\ LL}$									0.5	2.0	3.0	mA
	PS: L XV1: H	$I_{CC2\text{-}1\ LH}$		H										
	PS: H XV1: L	$I_{CC2\text{-}1\ HL}$	H								0.1	0.5	1.0	mA
	PS: H XV1: H	$I_{CC2\text{-}1\ HH}$	H	H							1.5	3.2	5.0	mA
DC supply current of vertical clock driver 2 at $V_{CC2\text{-}2}$	PS: L XV2: L	$I_{CC2\text{-}2\ LL}$									0.5	2.0	3.0	mA
	PS: L XV2: H	$I_{CC2\text{-}2\ LH}$			H									
	PS: H XV2: L	$I_{CC2\text{-}2\ HL}$	H								0.1	0.5	1.0	mA
	PS: H XV2: H	$I_{CC2\text{-}2\ HH}$	H		H						1.5	3.2	5.0	mA
DC supply current of vertical clock driver 3 at $V_{CC2\text{-}3}$	PS: L XV3: L	$I_{CC2\text{-}3\ LL}$									0.5	2.0	3.0	mA
	PS: L XV3: H	$I_{CC2\text{-}3\ LH}$				H								
	PS: H XV3: L	$I_{CC2\text{-}3\ HL}$	H								1.5	3.2	5.0	mA
	PS: H XV3: H	$I_{CC2\text{-}3\ HH}$	H			H					0.1	0.5	1.0	mA
DC supply current of vertical clock driver 4 at $V_{CC2\text{-}4}$	PS: L XV4: L	$I_{CC2\text{-}4\ LL}$									0.5	2.0	3.0	mA
	PS: L XV4: H	$I_{CC2\text{-}4\ LH}$					H							
	PS: H XV4: L	$I_{CC2\text{-}4\ HL}$	H								1.5	3.2	5.0	mA
	PS: H XV4: H	$I_{CC2\text{-}4\ HH}$	H				H				0.1	0.5	1.0	mA
DC supply current of sensor gate drivers 1, 2 at V_{CC3}	PS: L XSG1, 2: L	$I_{CC3\ LL}$									1.0	4.0	6.0	mA
	PS: L XSG1, 2: H	$I_{CC3\ LH}$						H	H					
	PS: H XSG1, 2: L	$I_{CC3\ HL}$	H								3.0	6.4	10.0	mA
	PS: H XSG1, 2: H	$I_{CC3\ HH}$	H					H	H		0.1	0.7	1.4	mA
DC supply current of negative voltage generation driver at V_{CC4}	XNV: L	$I_{CC4\ L}$									0.5	2.0	3.0	mA
	XNV: H	$I_{CC4\ H}$								H				

Characteristics when CXA1065M drives the equivalent circuit of CCD imager, ICX022

Supply current

Ta = 25°C, V_{CC1} = 5V, V_{CC2} = 10.6V, V_{CC3} = 13.4V, V_{CC4} = 10.6V
The CXD1035B (timing generator) is used as the input signal source.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current at V_{CC1}	I_{CC1}		0.5	1.9	3.0	mA
Supply current at V_{CC2}	I_{CC2}		3.0	7.1	8.5	mA
Supply current at V_{CC3}	I_{CC3}		0.2	0.8	1.5	mA
Supply current at V_{CC4}	I_{CC4}		0.5	2.0	3.0	mA

Output waveform of each driver

Ta = 25°C, V_{CC1} = 5V, V_{CC2} = 10V, V_{CC3} = 13.4V, V_{CC4} = 10.6V
The CXD1035B (timing generator) is used as the input signal source.

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Output waveform of negative voltage generation driver	Falling edge voltage	V_{NVL}	Voltage at NV at 350ns after XNV rising edge	0.05	0.71	1.15	V
	Rising edge voltage	V_{NVH}	Voltage at NV at 350ns after XNV falling edge	9.45	10.13	10.55	V
	L level voltage	V_{NVLL}	Voltage at NV at 2100ns after rising edge of XNV	−0.08	−0.02	0.04	V
	H level voltage	V_{NVHH}	Voltage at NV at 2100ns after at XNV falling edge	10.52	10.58	10.64	V

Parameter			Symbol	Condition	Min.	Typ.	Max.	Unit
Output waveforms of vertical clock drivers 1, 2, 3, 4	L level voltage	Vφ1	$V_{\phi 1L}$	Voltage at Vφ1 at 490ns after XV1 rising edge	0.06	0.32	0.80	V
		Vφ2	$V_{\phi 2L}$	Voltage at Vφ2 at 490ns after XV2 rising edge		0.35		
		Vφ3	$V_{\phi 3L}$	Voltage at Vφ3 at 490ns after XV3 rising edge		0.45		
		Vφ4	$V_{\phi 4L}$	Voltage at Vφ4 at 490ns after XV4 rising edge		0.47		
	H level voltage	Vφ1	$V_{\phi 1H}$	Voltage at Vφ1 at 1050ns after XV1 falling edge	9.91	9.98	10.06	V
		Vφ2	$V_{\phi 2H}$	Voltage at Vφ2 at 1050ns after XV2 falling edge				
		Vφ3	$V_{\phi 3H}$	Voltage at Vφ3 at 1050ns after XV3 falling edge				
		Vφ4	$V_{\phi 4H}$	Voltage at Vφ4 at 1050ns after XV4 falling edge				
	L coupling voltage	Vφ1	$V_{\phi 1LL}$	Voltage at Vφ1 at 280ns after XV2 rising edge	−0.58	−0.29	0.01	V
		Vφ2	$V_{\phi 2LL}$	Voltage at Vφ2 at 280ns after XV3 rising dege	−0.55	−0.34	−0.12	V
		Vφ3	$V_{\phi 3LL}$	Voltage at Vφ3 at 280ns after XV4 rising dege	−0.60	−0.37	−0.13	V
		Vφ4	$V_{\phi 4LL}$	Voltage at Vφ4 at 280ns after XV1 rising dege	−0.60	−0.42	−0.23	V
	H coupling voltage	Vφ1	$V_{\phi 1HH}$	Voltage at Vφ1 at 280ns after XV2 falling edge	10.16	10.46	10.62	V
		Vφ2	$V_{\phi 2HH}$	Voltage at Vφ2 at 280ns after XV3 falling edge		10.45		
		Vφ3	$V_{\phi 3HH}$	Voltage at Vφ3 at 280ns after XV4 falling edge		10.37		
		Vφ4	$V_{\phi 4HH}$	Voltage at Vφ4 at 280ns after XV1 falling edge		10.44		
	L coupling amplitude	Vφ1	$V_{\phi 1L\text{-}LL}$	$V_{\phi 1L} - V_{\phi 1LL}$	0.14	0.61	1.07	V
		Vφ2	$V_{\phi 2L\text{-}LL}$	$V_{\phi 2L} - V_{\phi 2LL}$	0.25	0.68	1.10	V
		Vφ3	$V_{\phi 3L\text{-}LL}$	$V_{\phi 3L} - V_{\phi 3LL}$	0.36	0.81	1.26	V
		Vφ4	$V_{\phi 4L\text{-}LL}$	$V_{\phi 4L} - V_{\phi 4LL}$	0.44	0.88	1.32	V
Output waveforms of sensor gate drivers 1, 2	Falling edge voltage	SG1	V_{SG1L}	Voltage at SG1 at 350ns after XSG1 rising edge	0.14	0.84	1.46	V
		SG2	V_{SG2L}	Voltage at SG2 at 350ns after XSG2 rising edge		0.88		
	Rising edge voltage	SG1	V_{SG1H}	Voltage at SG1 at 350ns after XSG1 falling edge	11.94	12.74	13.26	V
		SG2	V_{SG2H}	Voltage at SG2 at 350ns after XSG2 falling edge		12.59		
	L level voltage	SG1	V_{SG1LL}	Voltage at SG1 at 1330ns after XSG1 rising edge	−0.11	0.00	0.11	V
		SG2	V_{SG2LL}	Voltage at SG2 at 1330ns after XSG2 rising edge				
	H level voltage	SG1	V_{SG1HH}	Voltage at SG1 at 1330ns after XSG1 falling edge	13.25	13.36	13.47	V
		SG2	V_{SG2HH}	Voltage at SG2 at 1130ns after XSG2 falling edge				

Electrical Characteristics Test Circuit 1

DC characteristics testing

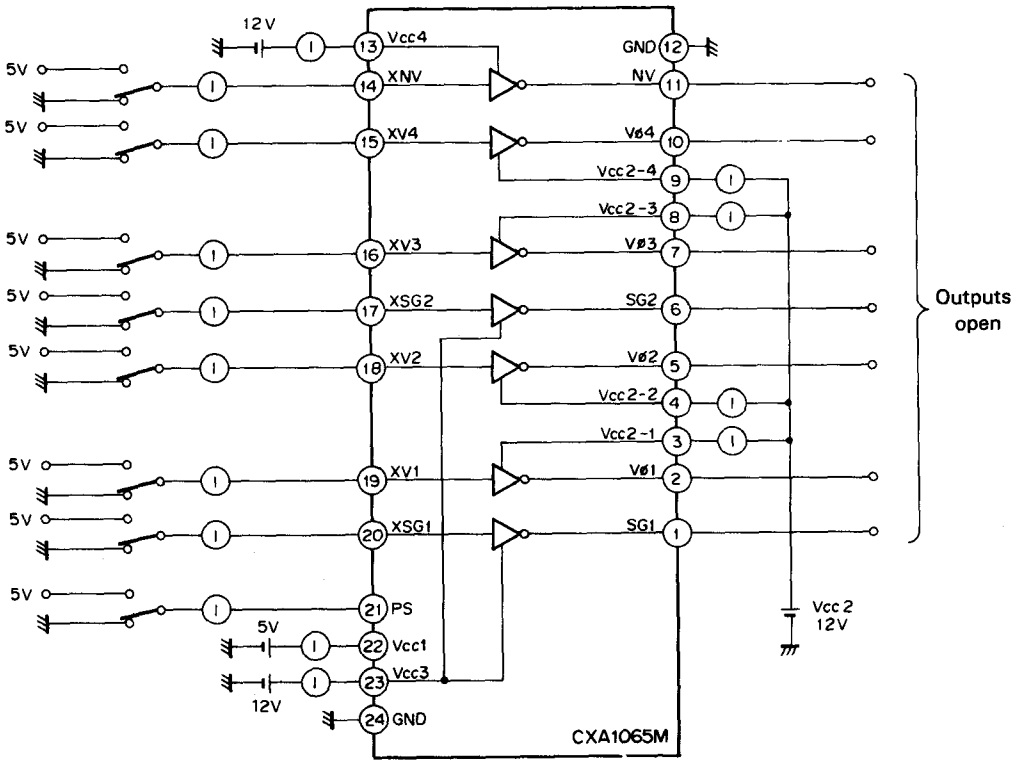


Fig. 1

Electrical Characteristics Test Circuit 2

Supply current testing when CXA1065M drives the equivalent circuit of CCD Imager, ICX022.

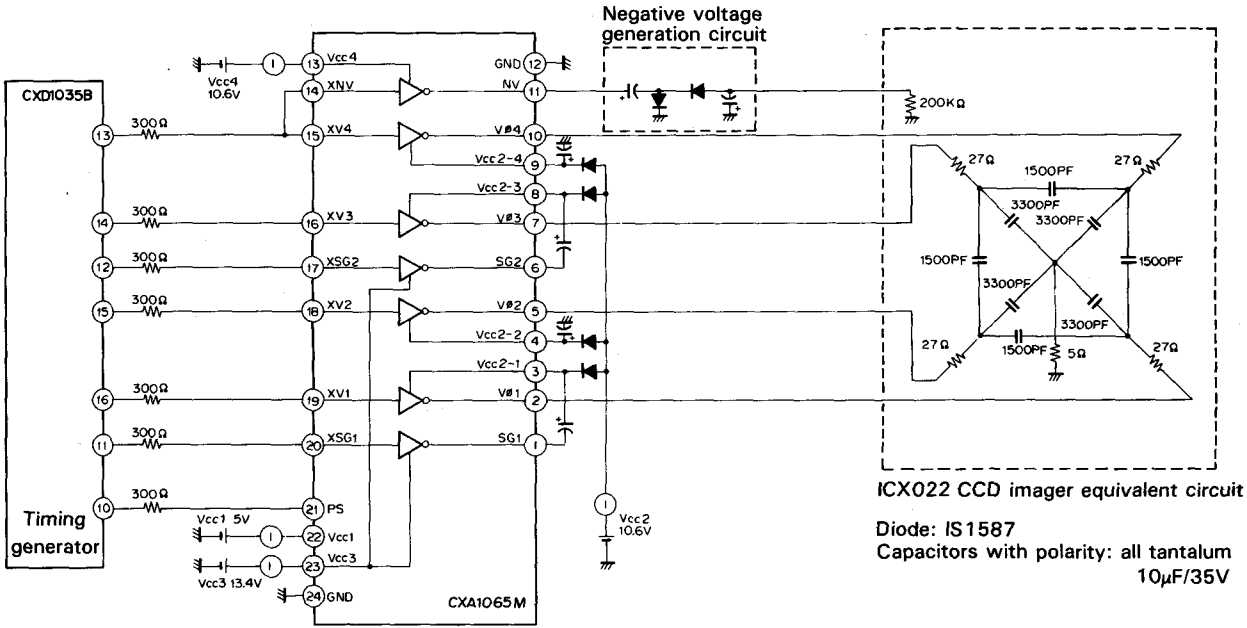


Fig. 2

Electrical Characteristics Test Circuit 3

Waveforms Testing

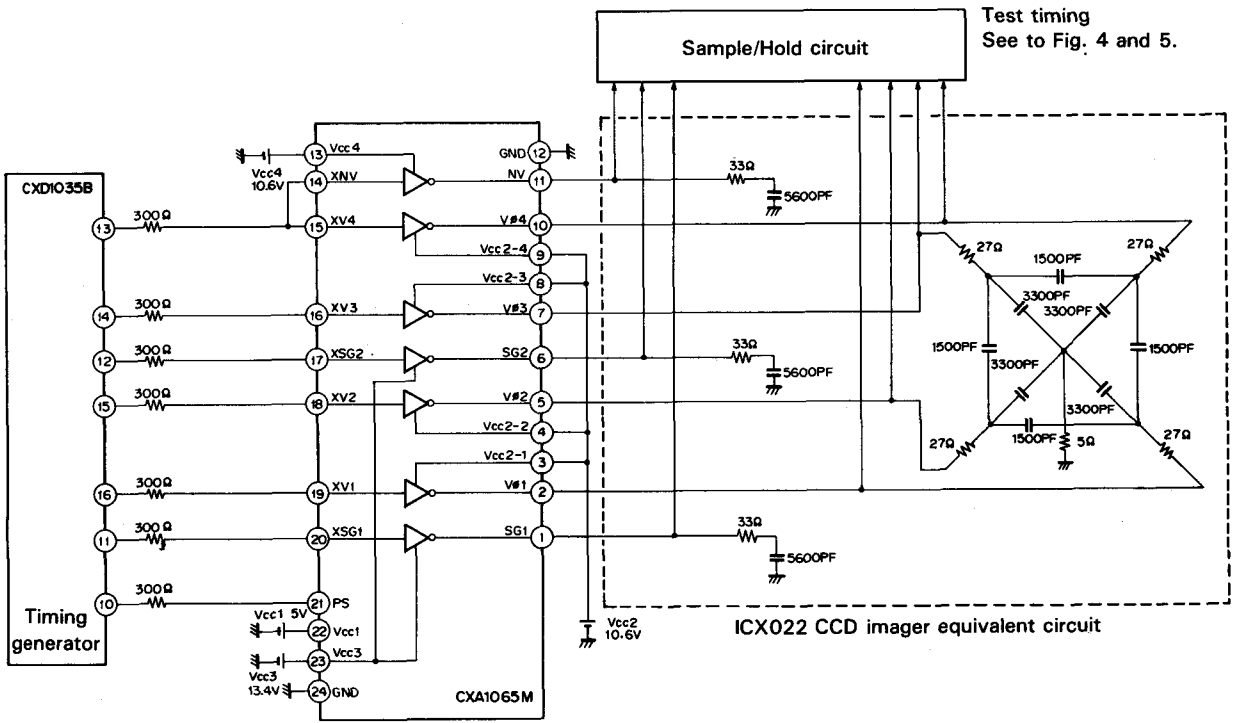


Fig. 3

Timing Chart

Waveform testing of 4-phase vertical clock drivers

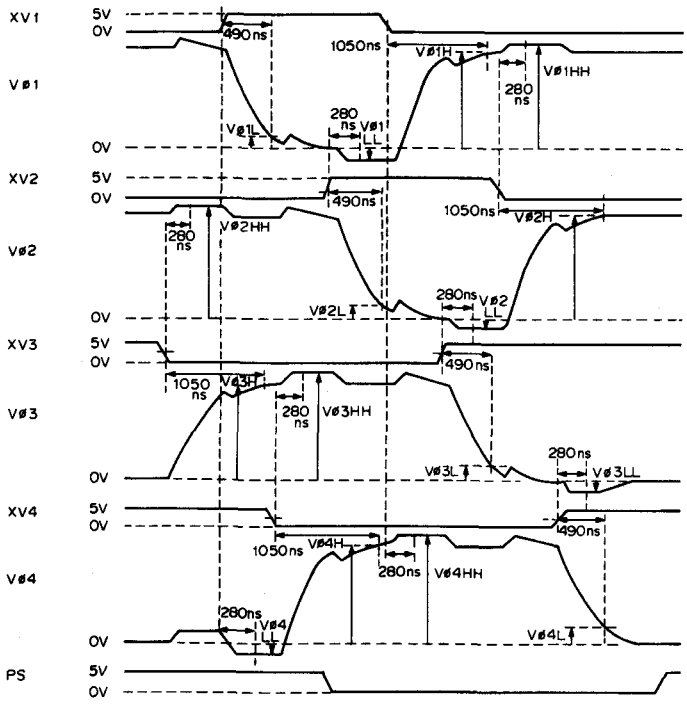


Fig. 4

Waveform testing of sensor gate drivers and negative voltage generation drivers

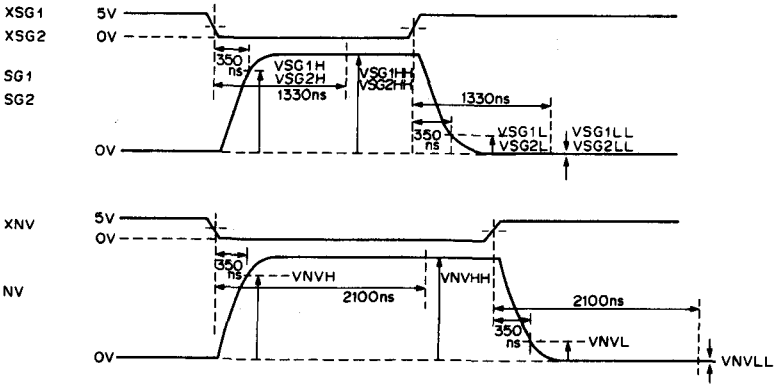


Fig. 5

Description of Operation

Description of functions and operation of the CXA1065M internal circuits

The CXA1065M is composed of a bias circuit and seven drivers.

Apply a voltage of 5 V to the Vcc1 terminal of the bias circuit. This circuit not only determines the DC bias for the seven drivers, but also has a power-saving function which reduces the power consumptions of four vertical clock drivers and two sensor gate drivers.

Directly connect the output of a CMOS IC to the input pins of the seven drivers. (Signal level, H: 5V, L: 0V) The output signal of each driver is inverted with low output impedance and wide amplitude. The output H level voltage of each driver is almost equal to the bias voltage of output stage and the L level output voltage is almost equal to the ground level. (See Fig. 6.)

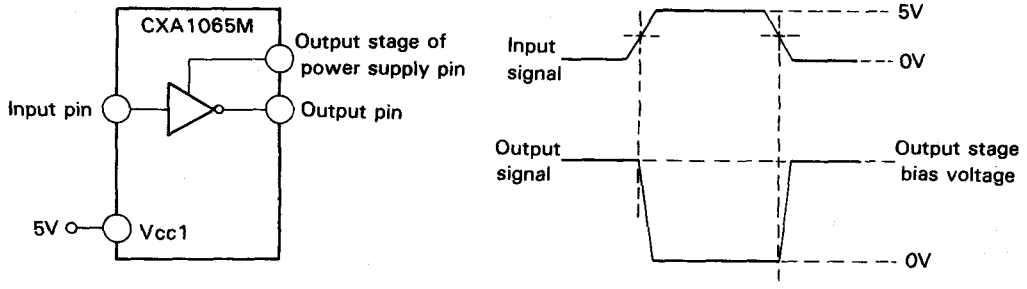


Fig. 6

The 4-phase clock drivers have a suppressing function of the coupling between phases when a CCD imager is driven. This function is suppress coupling voltage from other phases through the imager junction capacitances.

*Power-saving function

The CCD imaging device is equivalently, capacitive load.

Then a large driving ability is required only in the transient period of the output, and there is no need for such a large ability in other periods. The DC bias of the 4-phase clock drivers and 2 sensor gate drivers is changed by the input signal at the PS pin with appropriate timing, to reduce bias current when a large driving ability is not needed and achieve low power consumption.

Reference data: Typical values of supply current when the ICX022 equivalent circuit is driven (See Fig. 2)

	Using power-saving function	Not using power-saving function (PS pin fixed at 0V)
Supply current at Vcc1	1.9 mA	2.3 mA
Supply current at Vcc2	7.1 mA	12.7 mA
Supply current at Vcc3	0.8 mA	3.3 mA
Supply current at Vcc4	2.0 mA	2.0 mA

Description of Operation (CCD imager (ICX022) vertical clock driving system)

(For further information on the driving system of the CCD imager, refer to the specifications.)

Connect the output pin of the CXD1035B (CMOS IC) which is the CCD camera scanning timing generator, to the respective pins (Pin 14 through 21) of CXA1065M.

Clamp the output signal of the 4-phase vertical clock driver to the low level and input it to the vertical shift register transfer clock pin of the CCD imager.

Rectify the output signal of the negative voltage generation driver to obtain two reference voltage (negative voltages) for the low-level clamp. These two voltages are provided to compensate the clamping loss which may occur from the difference in duty between the 4-phase vertical clock drive signals. (When stable low-level clamp reference voltage supply is available with in the equipment, the rectifying circuit for the negative voltage is no more required.)

With the system shown in Fig. 8, the H level voltage of V clock level of the 4-phase vertical clock drive signals after the low-level clamp, is kept at 0 V even if Vcc4 is varied. This is because the circuit is designed to keep the low-level clamp reference voltage equal to the output voltage amplitude of the vertical clock drivers.

To obtain one of the readout clock pulse signals: The output signal of sensor gate driver 1 is used to modulate the output bias voltage of vertical clock driver 1.

To obtain the other signal: The output signal of sensor gate driver 2 used to modulate the output bias voltage of vertical clock driver 3.

If no source of high DC voltage is available in the equipment, the output signal for negative voltage generation driver can be utilized to generate the CCD imager substrate voltage. (See Fig. 7.)

Substrate voltage generation circuit

When maximum DC power supply in the equipment is +15V

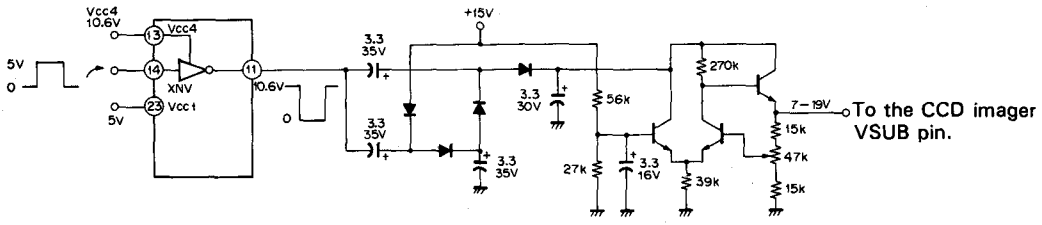
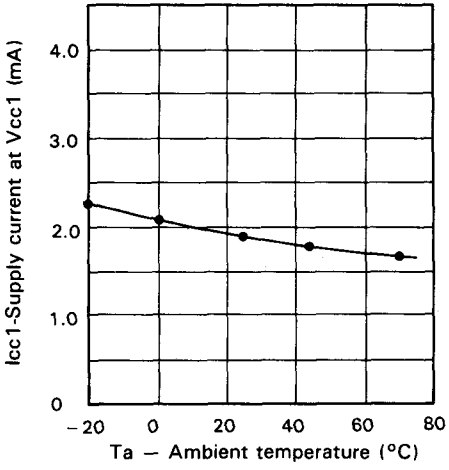


Fig. 7

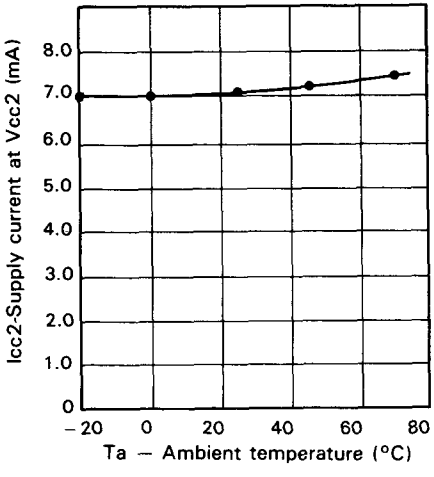
Performance Curves

Supply current when the ICX022 equivalent circuit is driven (Refer to the Test Circuit in Fig. 2).

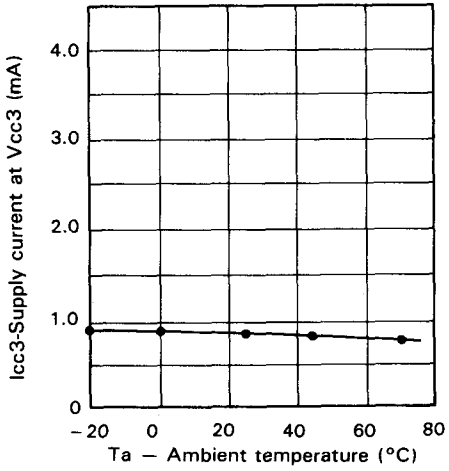
Supply current at Vcc1 vs. Ambient temperature



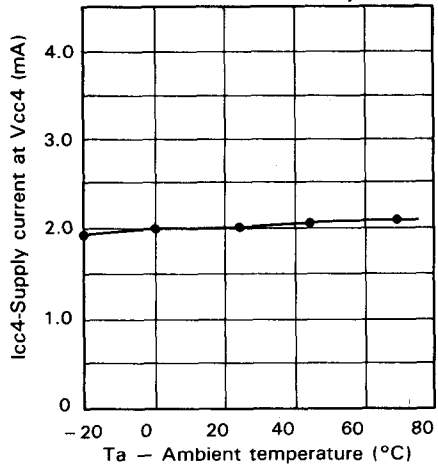
Supply current at Vcc2 vs. Ambient temperature



Supply current at Vcc3 vs. Ambient temperature



Supply current at Vcc4 vs. Ambient temperature



Notes on Application

- A large current flow through the power supply pin or the GND pin during the transient period of the output signal. Therefore, the GND pin must be grounded at a point within 1 cm from the pin. In addition, set the by-pass capacitor of the power supply pin within 1 cm from the pin.
- A conventional CMOS IC suffices as the input signal source of this IC (with an input current of Max. 500μA). To obtain the sharp CCD imager driving signal, minimize the length of the signal line.
- With an elongated signal line between the output pin of this IC and the input pin of the CCD imager, the inductance of the line may cause linking. To avoid this, shorten the line or insert a resistance in series to dump the linking.
- If the signal line between the output pin of this CMOS IC and input pin of this IC is too long, stray capacitance is large. In this case input signal of this IC is dull then sharp CCD imager driving signal is not obtained.

Vertical Clock Driver of CCD Imager

Description

CXD1250M is a clock driver developed for the vertical register drive of ICX026/027.

Features

- 4-channel vertical clock driver and 1 channel substrate driver are built-in.

Structure

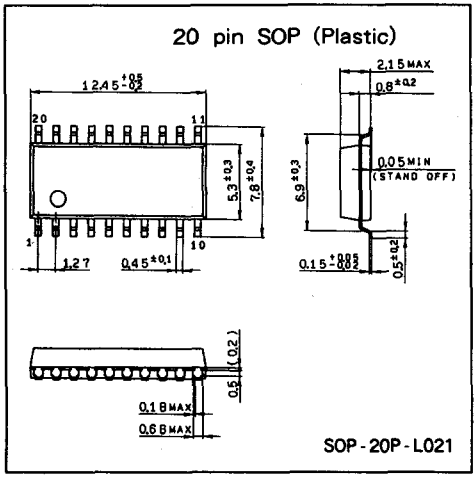
CMOS

Application

- CCD camera

Package Outline

Unit : mm



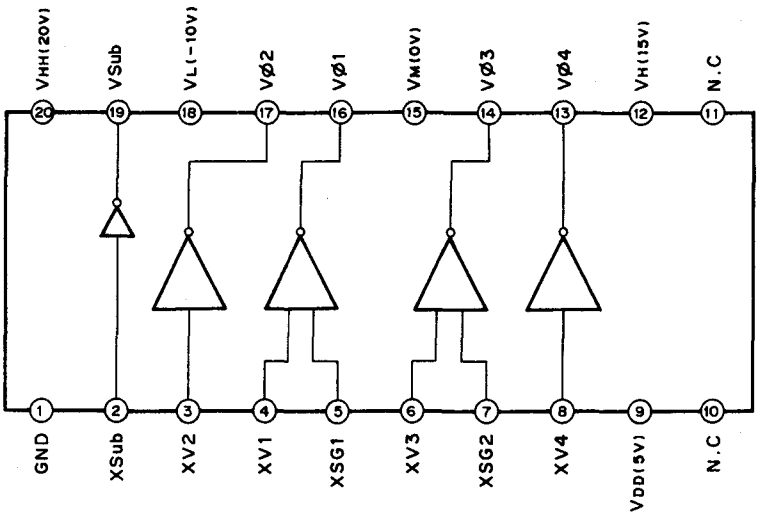
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	$V_L - 0.3$ to $V_L + 35.0$	V
	V_M	$V_L - 0.3$ to $V_L + 35.0$	V
	V_H	$V_L - 0.3$ to $V_L + 35.0$	V
	V_{HH}	$V_L - 0.3$ to $V_L + 35.0$	V
• Input voltage	V_I	$V_L - 0.3$ to $V_{DD} + 0.3$	V
• Output voltage	MV φ (pins 11, 13)	$V_L - 0.3$ to $V_M + 0.3$	V
• Output voltage	HV φ (pins 14, 16)	$V_L - 0.3$ to $V_H + 0.3$	V
• Output voltage	HHV φ (pin 19)	$V_L - 0.3$ to $V_{HH} + 0.3$	V
• Operating temperature	Topr	−25 to +85	°C
• Storage temperature	Tstg	−40 to +125	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	$V_L + 15.0$	V
	V_M	$V_L + 10.0$	V
	V_H	$V_L + 25.0$	V
	V_{HH}	$V_L + 30.0$	V
• Operating temperature	Topr	−20 to +75	°C

Block Diagram and Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	GND	—	GND
2	XSub	I	Output control (VSub)
3	XV2	I	Output control ($V_{\phi 2}$)
4	XV1	I	Output control ($V_{\phi 1}$)
5	XSG1	I	Output control ($V_{\phi 1}$)
6	XV3	I	Output control ($V_{\phi 3}$)
7	XSG2	I	Output control ($V_{\phi 2}$)
8	XV4	I	Output control ($V_{\phi 4}$)
9	V_{DD}	—	Power supply (5V)
10	NC	—	
11	NC	—	
12	V_H	—	Power supply (15V)
13	$V_{\phi 4}$	O	Output (2 level : V_M, V_L)
14	$V_{\phi 3}$	O	Output (3 level : V_H, V_M, V_L)
15	V_M	—	Power supply (0V)
16	$V_{\phi 1}$	O	Output (3 level : V_H, V_M, V_L)
17	$V_{\phi 2}$	O	Output (2 level : V_M, V_L)
18	V_L	—	Power supply (− 10V)
19	VSub	O	Output (2 level : V_{HH}, V_L)
20	V_{HH}	—	Power supply (20V)

Truth Table

Input				Output		
XV1 • 3	XSG1 • 2	XV2 • 4	XSub	V φ 1 • 3	V φ 2 • 4	VSub
L	H	X	X	V_M	X	X
H	H	X	X	V_L	X	X
X	X	L	X	X	V_M	X
X	X	H	X	X	V_L	X
X	X	X	L	X	X	V_{HH}
X	X	X	H	X	X	V_L
L	L	H	X	V_H	V_L	X
H	L	X	X	Z	X	X

X : Don't Care
Z : High Impedance

DC Characteristics (Ta = 25°C)

Item	Symbol	Test condition	Power supply	Min.	Typ.	Max.	Unit
"H" level input voltage	V_{IH}		$V_{DD} = 5$ $V_L = -10$ $V_M = 0$ $V_H = 15$ $V_{HH} = 20$	3.5	—	—	V
"L" level input voltage	V_{IL}			—	—	1.5	V
"L" level output voltage	$V_{\phi L}$	$I_{\phi L} = 20\ \mu A$		—	−10	−9.9	V
"M" level output voltage	$V_{\phi M}$	$I_{\phi M} = -20\ \mu A$		—	0.0	0.1	V
"M" level output voltage	$V_{\phi M}$	$I_{\phi M} = 20\ \mu A$		−0.1	0.0	—	V
"H" level output voltage	$V_{\phi H}$	$I_{\phi H} = -20\ \mu A$		14.9	15	—	V
"HH" level output voltage	$V_{\phi HH}$	$I_{\phi HH} = -20\ \mu A$		19.9	20	—	V
Input current	Ii			—	1.0	—	μA
Power supply current*	I_M			—	4.5	5.0	mA
Power supply current*	I_{DD}			—	0.3	0.5	mA
Power supply current*	I_H			—	0.1	0.2	mA
Power supply current*	I_{HH}			—	0.05	0.1	mA

*Supply current at operation (See the Test Circuit)

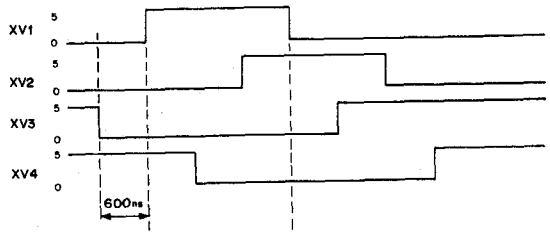
Switching Characteristics

(See the Test Circuit Ta = 25℃, V_{HH} = 20V, V_H = 15V, V_M = 0V, V_L = − 10V, V_{DD} = 5V)

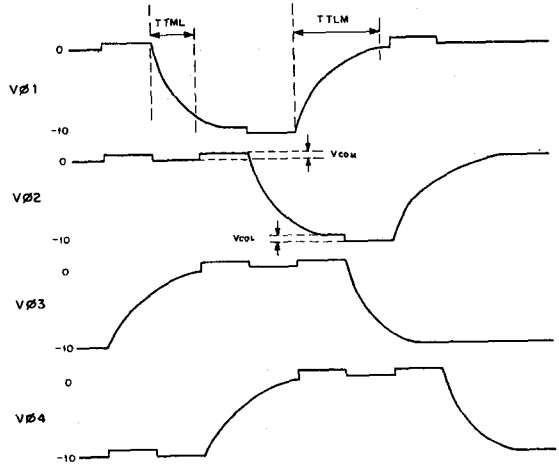
Item	Symbol	Conditions	Max.	Min.	Unit
Output current	I_L	V φ 1 to 4 = − 9.5V	− 25		mA
Output current	I_{M1}	V φ 1 to 4 = − 0.5V		10	mA
Output current	I_{M2}	V φ 1, 3 = 0.5V	− 9		mA
Output current	I_H	V φ 1, 3 = 14.5V		12	mA
Output current	I_{SL}	VSub = − 9.5V	− 12		mA
Output current	I_{SH}	VSub = − 19.5V		7	mA
Rise time $V_L \rightarrow V_M$	T_{TLM}	V φ 1 to 4 = − 0.5V After input transient	1000		ns
Fall time $V_M \rightarrow V_L$	T_{TML}	V φ 1, 3 = − 9.5V After input transient	500		ns
Rise time $V_M \rightarrow V_H$	T_{TMH}	V φ 1, 3 = 14V After input transient	1000		ns
Fall time $V_H \rightarrow V_M$	T_{THM}	V φ 1, 3 = 1V After input transient	1000		ns
Rise time $V_L \rightarrow V_{HH}$	T_{TLHH}	VSub = 17V After input transient	200		ns
Fall time $V_{HH} \rightarrow V_L$	T_{THHL}	VSub = − 7V After input transient	200		ns
Coupling amplitude (middle level)	V_{COM}	V φ 1 to 4	0.5		V
Coupling amplitude (low level)	V_{COL}	V φ 1 to 4	0.5		V

Input Waveform

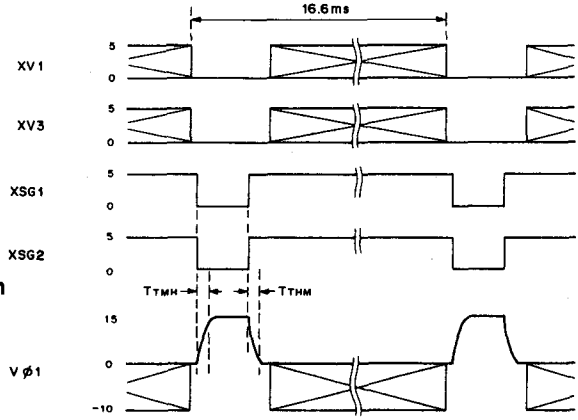
(Repeat Cycle 15.7kHz)



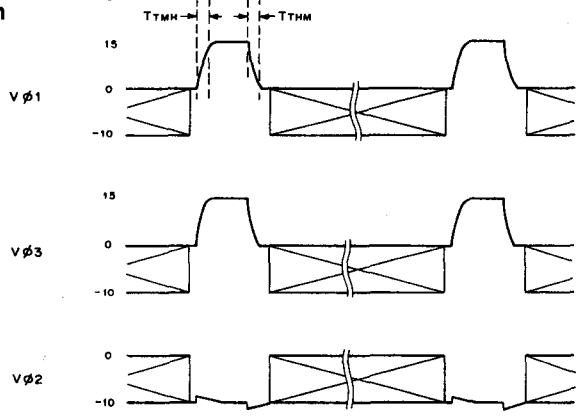
Output Waveform

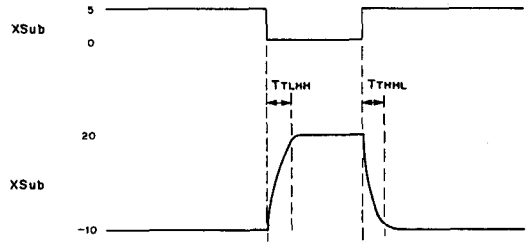


Input waveform

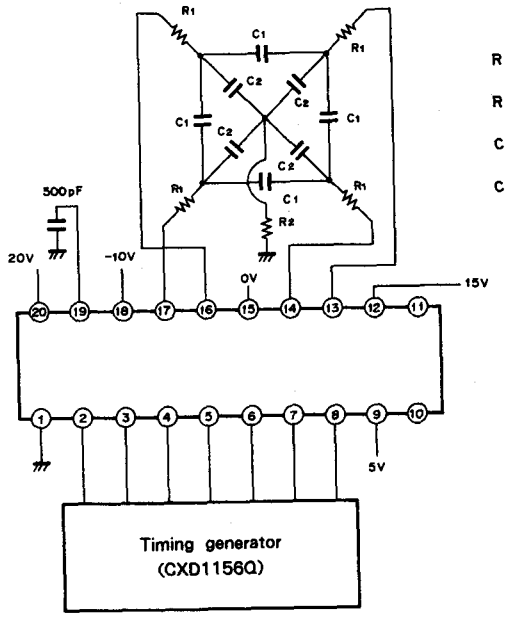


Output waveform





Test Circuit



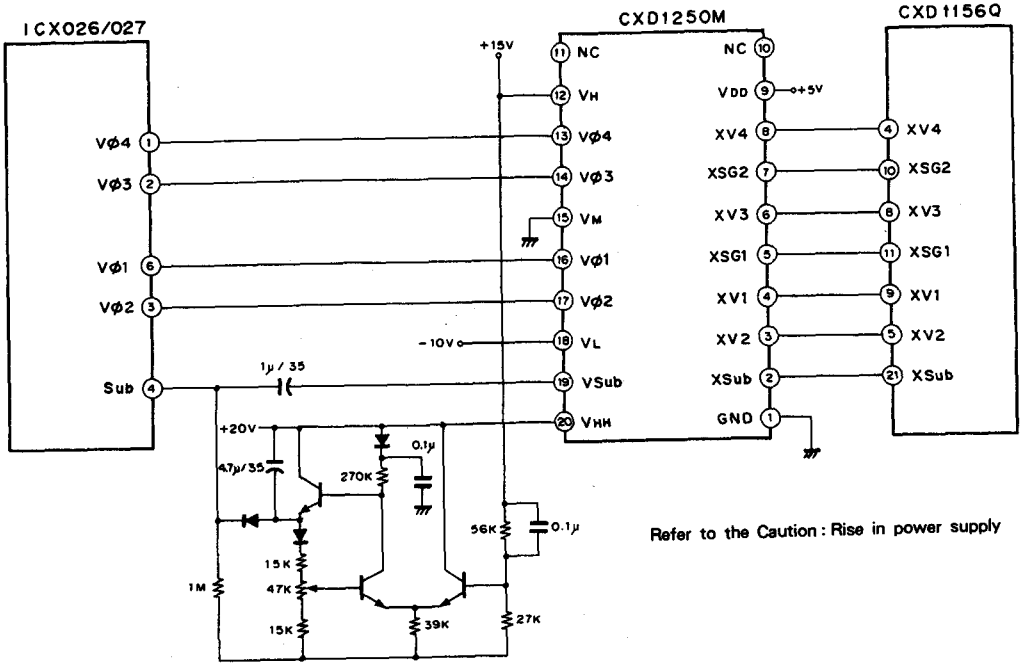
R1 ; 27Ω

R2 ; 5Ω

C1 ; 1500pF

C2 ; 3300pF

Application Circuit

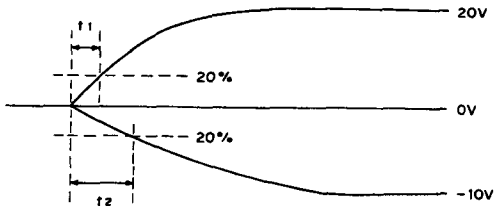


Refer to the Caution : Rise in power supply

Caution : Rise in Power Supply

When the substrate driver is in use, be careful not to let the CCD imager (ICX026/027) Sub (pin 4) turn into negative voltage.

To this end, raise the −10V and +20V supplies at the application circuit under the following conditions.



$t_2 > t_1 \geqq 10ms$

Signal Processing IC for Video Camera

5) Signal Processing IC for Video Camera

Type	Applications	Functions	Page
CX20095A CX20186	Video output	6dB amplifier, Video driver, Bidirectional video driver	479
CXA1516M/Q	Auto Focus detector for camcoder	Built-in 3-channel Built-in gain control (6 to 33dB)	486
CXA1270N	Vertical aperture correction	Vertical aperture correction signal generation	496
CXA1310AQ	CCD B/W camera processing	Signal processing, Built-in AGC loop operationnal amplifier	504
CXA1337Q-Z/R	CCD color camera sample and hold, color separation	CDS, AGC, color separation S/H, Chroma suppression	518
CXA1390AQ/AR		CDS, AGC,color separation	537
CXA1338Q-Z/R	CCD color camera matrix	From color complementary (Mg, G, Cy, Ye) mosaic coding, R, G, B, synthetic and Y signal processing	554
CXA1391Q/R	CCD color camera processing	Original color separation, White balance, γ correction, Sharpness control	575
CXA1339Q-Z/R		Matrix, White balance, γ correction, Negative/positive inversion	608
CXA1072Q-Z/R	CCD color camera encoder	Aperture, Auto-carrier balance, Negative-positive inversion, Fader, Chroma suppression, BLK cleaning	627
CXA1392Q/R		Aperture correction, Y/C separation output	651
CXA1592Q/R	CCD color camera processing	Aperture correction, Y/C separation output Chang version of CXA1392 (ratio and level)	674
CXA1393AN/AM	Title addition	Title insertion for video camera	697
CXA1439M	For CCD camera, CDS	CDS, 6dB amplifier, 9.5dB amplifier	713
CXL1503M CXL1505M	Chroma signal 1H delay line	In-phase for color signal delay (1H×4) CMOS-CCD delay line	721
CXL1517M CXL1518M	Chroma signal 1H delay line	1H×3 CMOS-CCD delay line	729
CXL1517N CXL1518N	Chroma signal 1H delay line	1H×3 CMOS-CCD delay line	736
CXL1504M	Luminance signal 1H delay line	NTSC 1H CMOS-CCD delay line	743
CXL5504M/P			751

SONY CX20095A/CX20186

Video Output

Description

The CX20095A/CX20186 is a bipolar IC designed as a driver of 75Ω line (transmission and receiving line) used in the video signal system. It is comprised of a 75Ω line drive, receiving amplifier and 6dB amplifier for multi-purpose applications.

Features

- Low power supply voltage operation, Vcc = 5V (Standard).
- Transmission/Receiving amplifier has a built-in sync chip clamp.
- Bilateral communication configuration is possible with one line.
- Driver amp and 6dB amp are provided with power-saving function.
- Simple superimpose is possible with the trans amp.

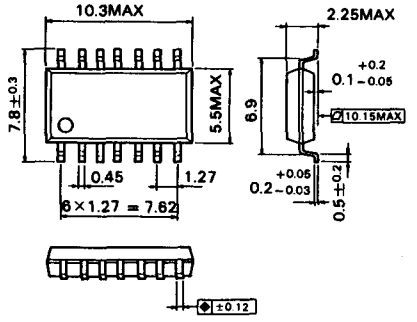
Structure

Bipolar silicon monolithic IC

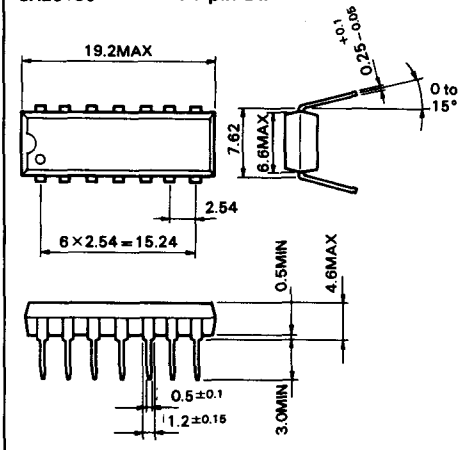
Package Outline

Unit: mm

CX20095A 14 pin SOP



CX20186 14 pin DIP



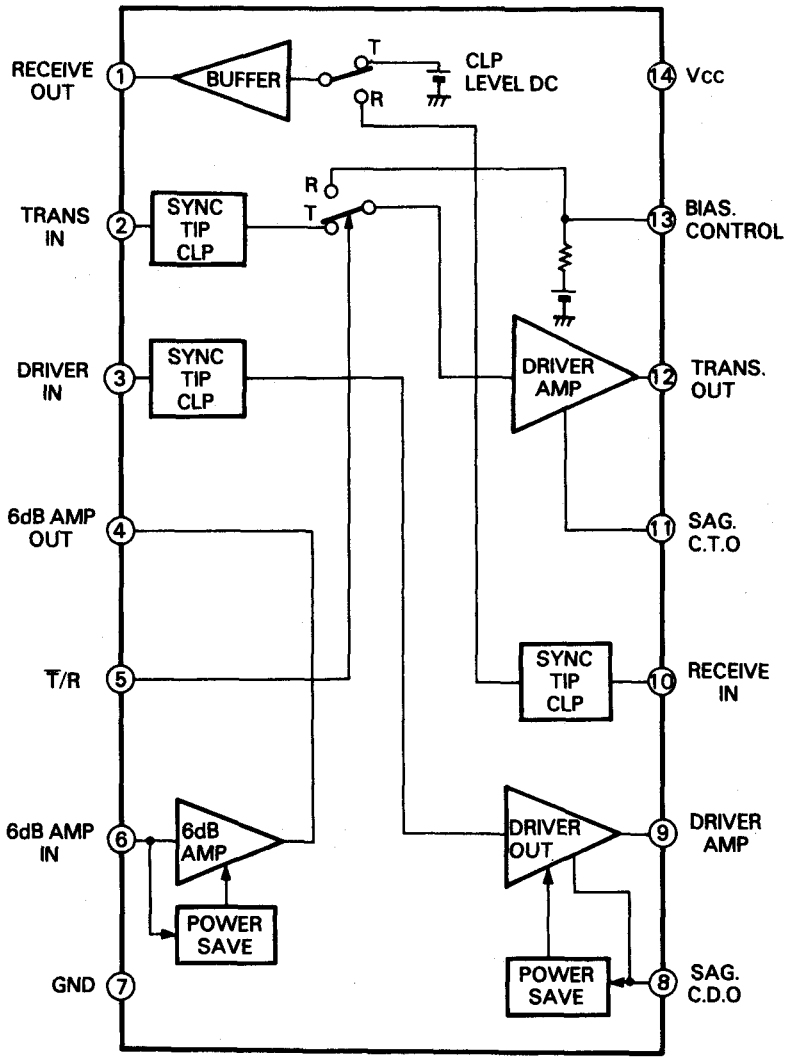
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc		17	V
• Operating temperature	Topr		−10 to +65	°C
• Storage temperature	Tstg		−55 to +150	°C
• Allowable power dissipation	PD	CX20095A	500	mW
		CX20186	650	mW

Recommended Operating Condition

• Supply voltage	Vcc	4.8 to 5.2	V

Block Diagram and Pin Configuration (Top view)



Pin Description

Standard terminal voltage (DC voltage when no signal is input, Ta = 25°C. See Electrical Characteristics Measuring Circuit Diagram) Unit: V

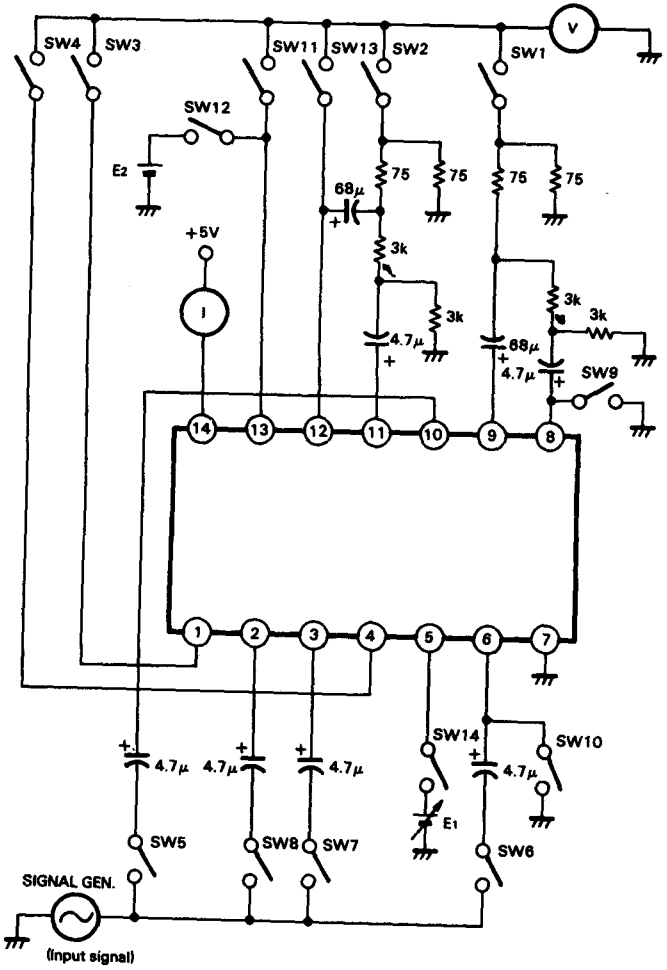
No.	Name	Voltage (V) standard value	Description
1	RECEIVE OUT	1.65	When Pin 5 is at "H", the signal input from Pin 10 is output with gain 0 dB. DC is output when Pin 5 is at "L".
2	TRANS IN	1.28	Trans amp input: As sync chip clamp may result, a low impedance input is required.
3	DRIVER IN	1.28	Drive amp input: As sync chip clamp may result, a low impedance input is required.
4	6 dB AMP OUT	2.35	The signal input from Pin 6 is output with gain 6 dB.
5	T/R	0	Mode switching terminal Trans/Receive: Receive mode at "H" (over 4V) and Trans mode at "L" (less than 1V).
6	6 dB AMP IN	2.45	6 dB amp input: Input impedance more than approx. 10 kΩ, DC 2.4V
7	GND	0	
8	SAG.C.D.O.	1.29	The Pin 9 sag is corrected by adding the sag component in the Pin 9 output. Refer to Electrical Characteristics Measuring Circuit Diagram.
9	DRIVER OUT	1.08	Driver amp output: 75 Ω line drive is output. The signal input from Pin 3 is output with gain 6 dB.
10	RECEIVE IN	1.74	Receiving amp input: As sync chip clamp may result, a low impedance input is required.
11	SAG.C.T.O.	1.30	The Pin 12 sag is corrected by adding the sag component in the Pin 12 output. Refer to Electrical Characteristics Measuring Circuit Diagram.
12	TRANS. OUT	1.10	Trans amp output: The signal input from Pin 2 when Pin 5 is at "L" is output to the 75 Ω line with a gain of 6 dB. A DC voltage determined at Pin 13 is output when Pin 5 is at "H".
13	BIAS. CONTROL	2.13	When Pin 5 is at "H", its voltage is varied to vary the Pin 12 output (DC) in turn. By linking with Pin 5, simple superimpose can be possible in the Pin 12 output. (In this case, the Pin 1 output is affected).
14	Vcc	5.0	+5.0V.

Electrical Characteristics

(Ta = 25°C, Vcc = 5.0V, See Electrical Characteristic Measuring Circuit Diagram)

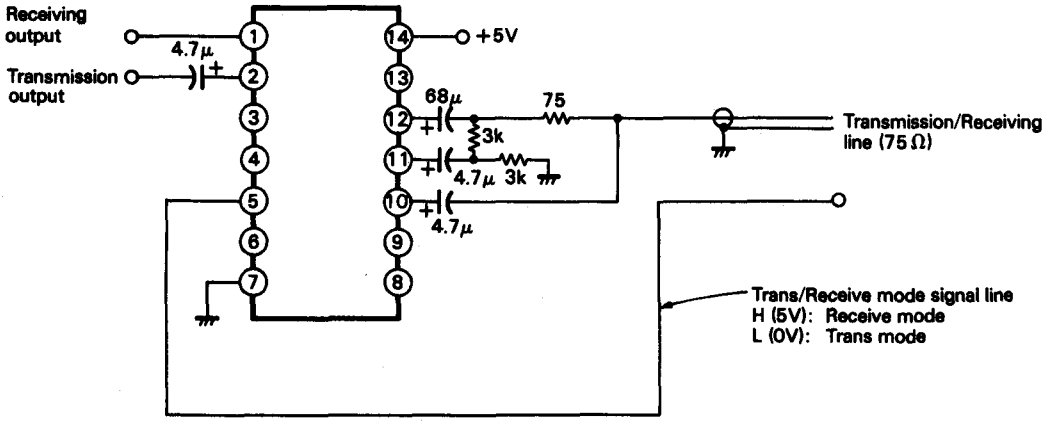
Test No.	Measuring item	Measuring point	Input condition	Measuring condition 1	2	3	4	5	6	7	8	9	10	11	12	13	14	Remark	Measuring symbol	Standard Min.	Typ.	Max.	Unit
1	Consumption current	I																	I_D	7.5	10.5	14	mA
2	Power saving	I										ON	ON						I_{DPS}	4.5	6.5	8.5	mA
3	Trans amp gain	V	500kHz, 1Vp-p		ON						ON						ON	E_1: Less than 1V (for 1Vp-p input)	G_T	−0.5	0	−0.5	dB
4	Trans dynamic range	V	16kHz, Square wave		ON						ON						ON	E_1: Less than 1V (input equivalent)	D_T	1.4			Vp-p
5-a	Trans bias control	V												ON			ON	E_1: Measured value over 4V = A	V_{13}	2.0	2.1	2.2	V
5-b	Trans bias control	V														ON	ON	E_1: Measured value over 4V = B	V_{12}	2.65	2.75	2.85	V
5-c	Trans bias control	V	E_2 = 2.3V												ON	ON	ON	$20 \log \frac{\text{(Measuring value)} - B}{E_2 - A}$ (E_2 = 2.3V)	G_{BC}	5.3	5.8	6.3	dB
6	Receiver amp gain	V	500kHz, 1Vp-p			ON		ON									ON	E_1: Over 4V (for 1Vp-p input)	G_R	−0.5	0	−0.5	dB
7	Receiver dynamic range	V	16kHz, Square wave			ON		ON									ON	E_1: Over 4V (input equivalent)	D_R	1.7			Vp-p
8	Driver amp gain	V	500kHz, 1Vp-p	ON						ON								For input 1Vp-p	G_D	−0.5	0	−0.5	dB
9	Driver dynamic range	V	16kHz, Square wave	ON						ON								Input equivalent	D_D	1.4			Vp-p
10	6dB amp gain	V	500kHz, 1Vp-p				ON		ON									For input 1Vp-p	G_A	5.5	6.0	6.5	dB
11	6dB dynamic range	V	16kHz, 1.4Vp-p Square wave				ON		ON									1.4Vp-p	D_A	2.6	2.8	3.0	Vp-p
12	Trans receiving leakage	V	4MHz 0.7Vp-p			ON					ON						ON	E_1: Over 4V (for 0.7Vp-p) (4MHz component)	L_{TR}			−40	dB

Electrical Characteristics Test Circuit

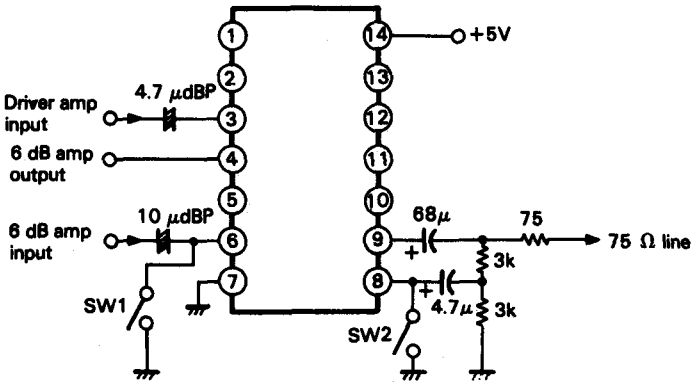


Application Circuit

Transmission and receiving reference circuit diagram (Trans amp, Receive amp)

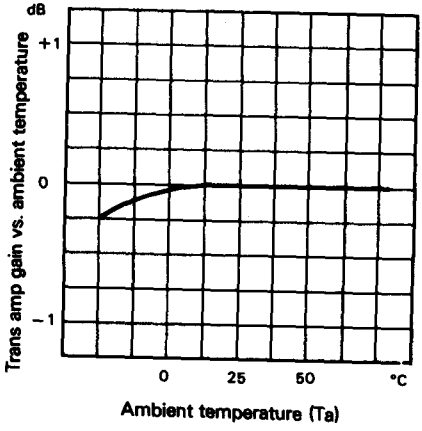


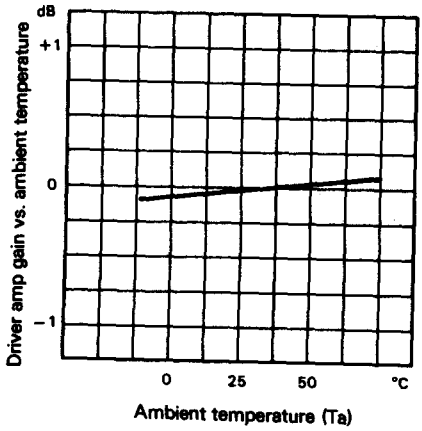
Driver amp, 6 dB amp external reference circuit diagram

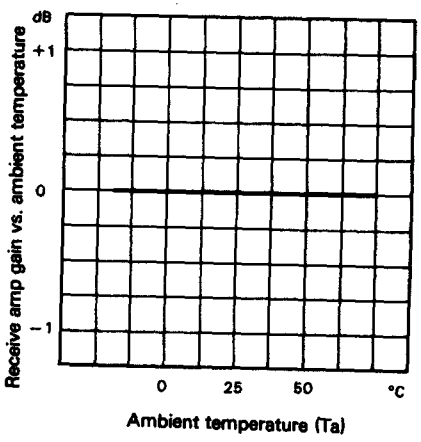


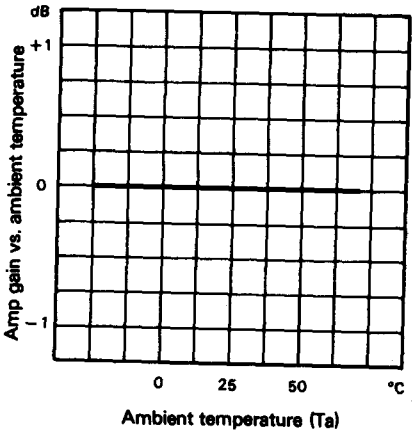
SW1: 6 dB amp power saving mode when switched on.
SW2: Driver amp power saving mode when switched on.

Temperature Characteristics









*Note) Gain at 25°C is assumed to be 0 dB.

AF Detector for Camcorder

Description

The CXA1516M/Q is a bipolar IC designed for the auto focus of CCD cameras.

It is composed of gain control amplifiers, double-side wave detectors and peak holds.

Features

- Built-in 3 channels
- Gain control with wide variable width (6 to 33dB Typ.)
- Gain setting possible for each channel independently
- Corresponds to 2 types of window pulses

Structure

Bipolar silicon monolithic IC

Application

CCD cameras

CXA1516M
28pin SOP (Plastic)

CXA1516Q
32pin QFP (Plastic)

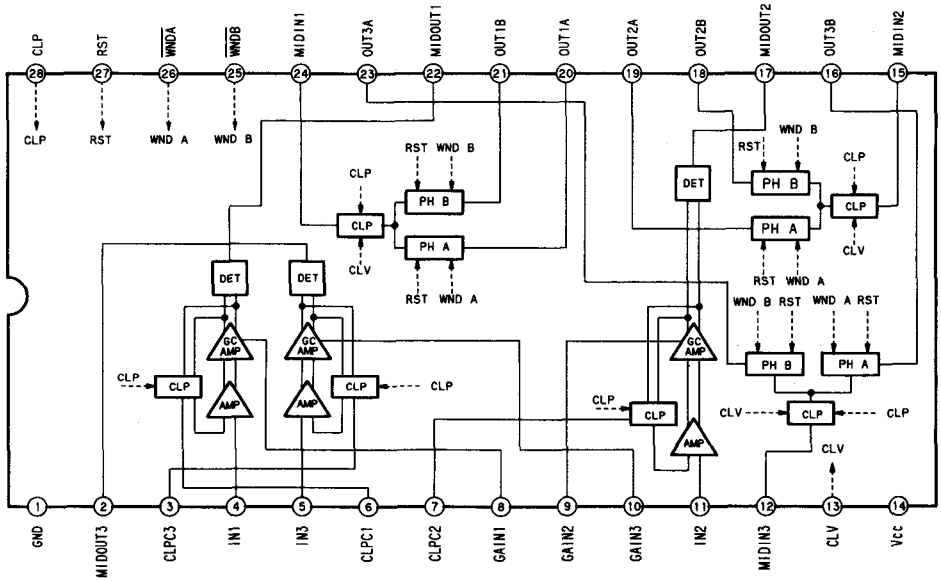
Absolute Maximum Ratings

• Supply voltage	V_{CC}		12	V
• Operating temperature	T_{opr}		−20 to +75	°C
• Storage temperature	T_{stg}		−65 to +150	°C
• Allowable power dissipation	P_D	CXA1516M	850	mW
		CXA1516Q	500	mW

Recommended Operating Conditions

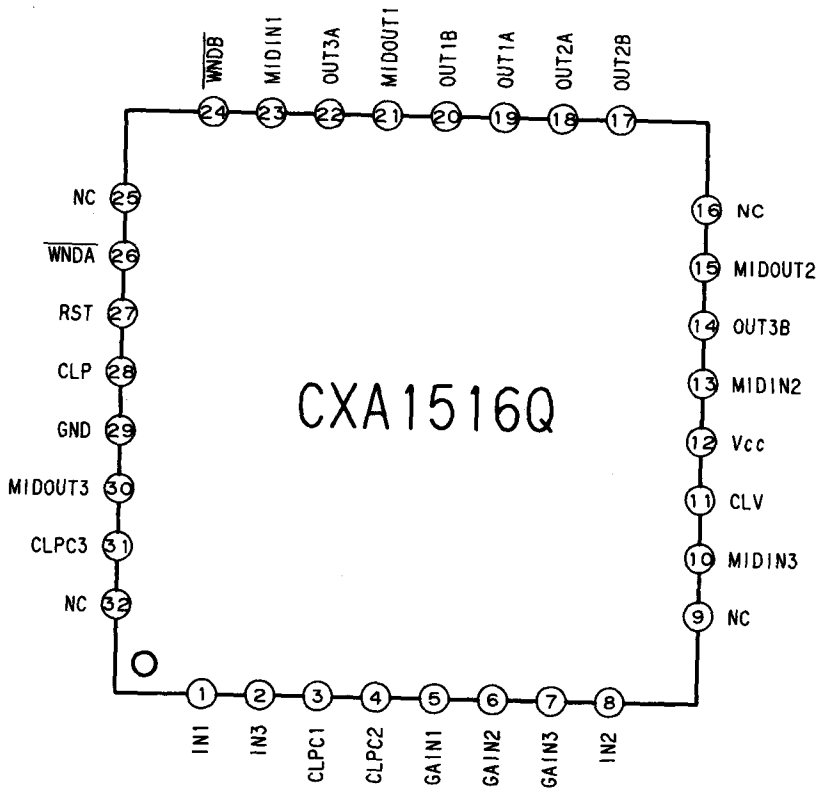
Supply voltage	V_{CC}	4.75 to 5.25	V

Block Diagram and Pin Configuration (CXA1516M)



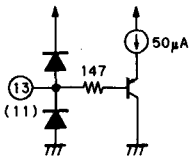
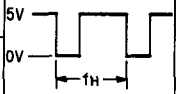
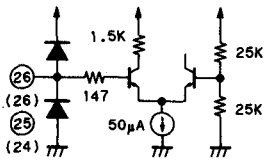
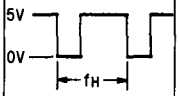
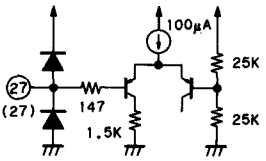
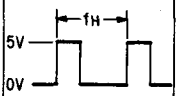
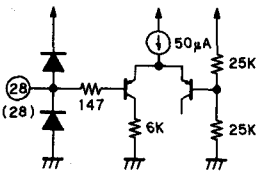
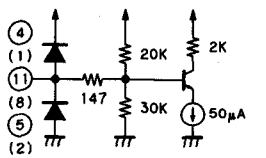
E90934-HP

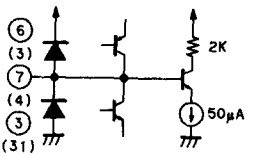
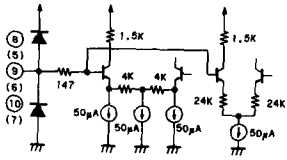
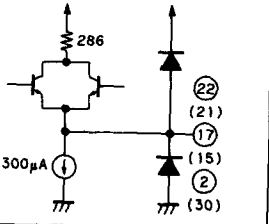
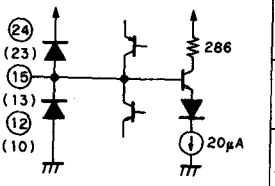
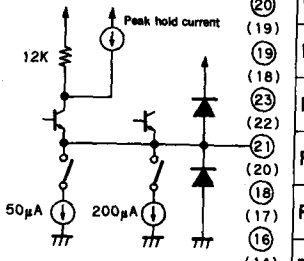
Pin Configuration (CXA1516Q)



Pin Description and Equivalent Circuit

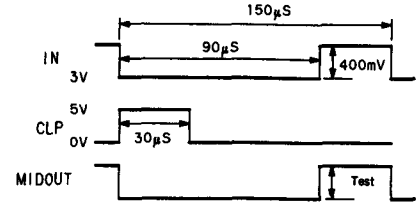
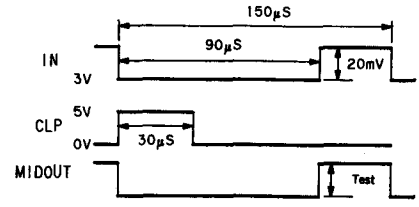
Brackets ( ) at the Equivalent Circuit indicate CXA1516Q Pin No.

Pin No. SOP	Pin No. QFP	Symbol	I/O	Voltage (Typ.)	Equivalent circuit	Description
1	29	GND	—	0V		
14	12	V_{CC}	—	5V		
13	11	CLV	I	1V		Peak hold reference voltage input pin. Input 1V.
26	26	$\overline{WNDA}$	I			WINDOW pulse input pin A (active at L) V_{TH}=2.5V
25	24	$\overline{WNDB}$	I			WINDOW pulse input pin B (active at L) V_{TH}=2.5V
27	27	RST	I			Reset pulse input pin (active at H) V_{TH}=2.5V
28	28	CLP	I			Clamp pulse input pin (active at H) V_{TH}=2.5V
4	1	IN1	I	3V		DET Amp input pin (ch 1). Input through capacitor. Biased internally at 3V.
11	8	IN2	I			DET Amp input pin (ch 2). Input through capacitor. Biased internally at 3V.
5	2	IN3	I			DET Amp input pin (ch 3). Input through capacitor. Biased internally at 3V.

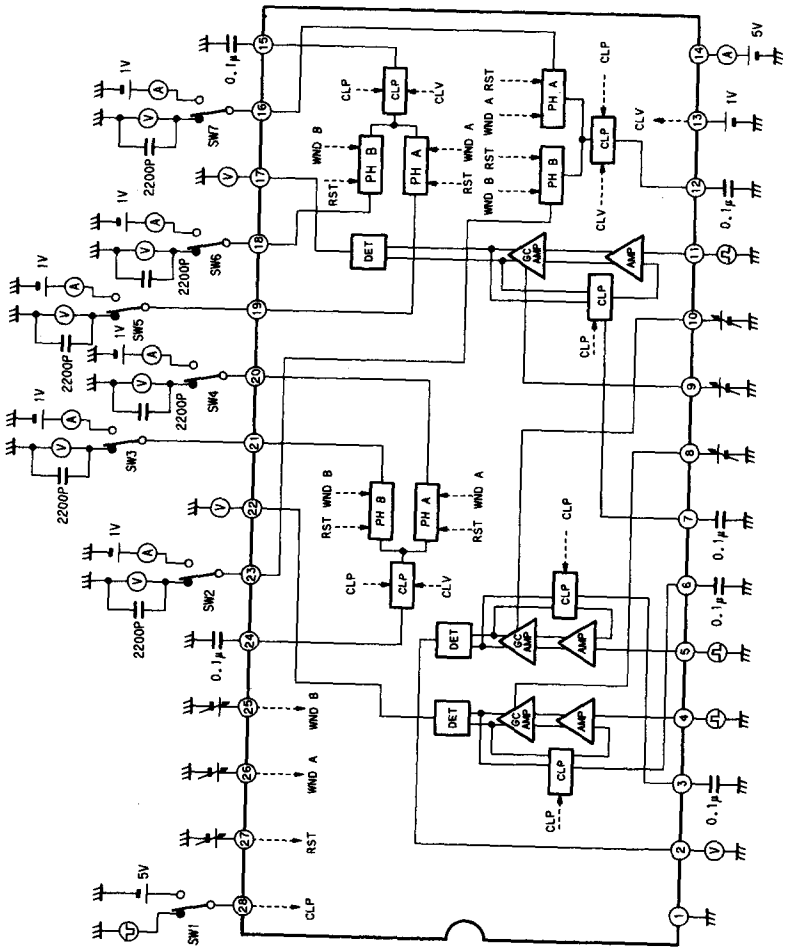
Pin No. SOP	Pin No. QFP	Symbol	I/O	Voltage (Typ.)	Equivalent circuit	Description
6	3	CLPC1	—	—		Capacitor connecting pin for MIDOUT1 output clamp
7	4	CLPC2				Capacitor connecting pin for MIDOUT2 output clamp
3	31	CLPC3				Capacitor connecting pin for MIDOUT3 output clamp
8	5	GAIN1	I	0V to 5V		Gain adjustment pin of MIDOUT1 output
9	6	GAIN2				Gain adjustment pin of MIDOUT2 output
10	7	GAIN3				Gain adjustment pin of MIDOUT3 output
22	21	MIDOUT1	O	2.2V (Black level)		DET Amp output pin 1
17	15	MIDOUT2				DET Amp output pin 2
2	30	MIDOUT3				DET Amp output pin 3
24	23	MIDIN1	I	2.4V (Black level)		Peak hold input pin 1. Input through clamp capacitor.
15	13	MIDIN2				Peak hold input pin 2. Input through clamp capacitor.
12	10	MIDIN3				Peak hold input pin 3. Input through clamp capacitor.
20	19	OUT1A	O	1V (Black level)		Peak hold output pin 1A
19	18	OUT2A	O			Peak hold output pin 2A
23	22	OUT3A	O			Peak hold output pin 3A
21	20	OUT1B	O			Peak hold output pin 1B
18	17	OUT2B	O			Peak hold output pin 2B
16	14	OUT3B	O			Peak hold output pin 3B
—	9, 16, 25, 32	NC	—			

Electrical Characteristics

(Ta=25°C, V_{CC}=5.0V)

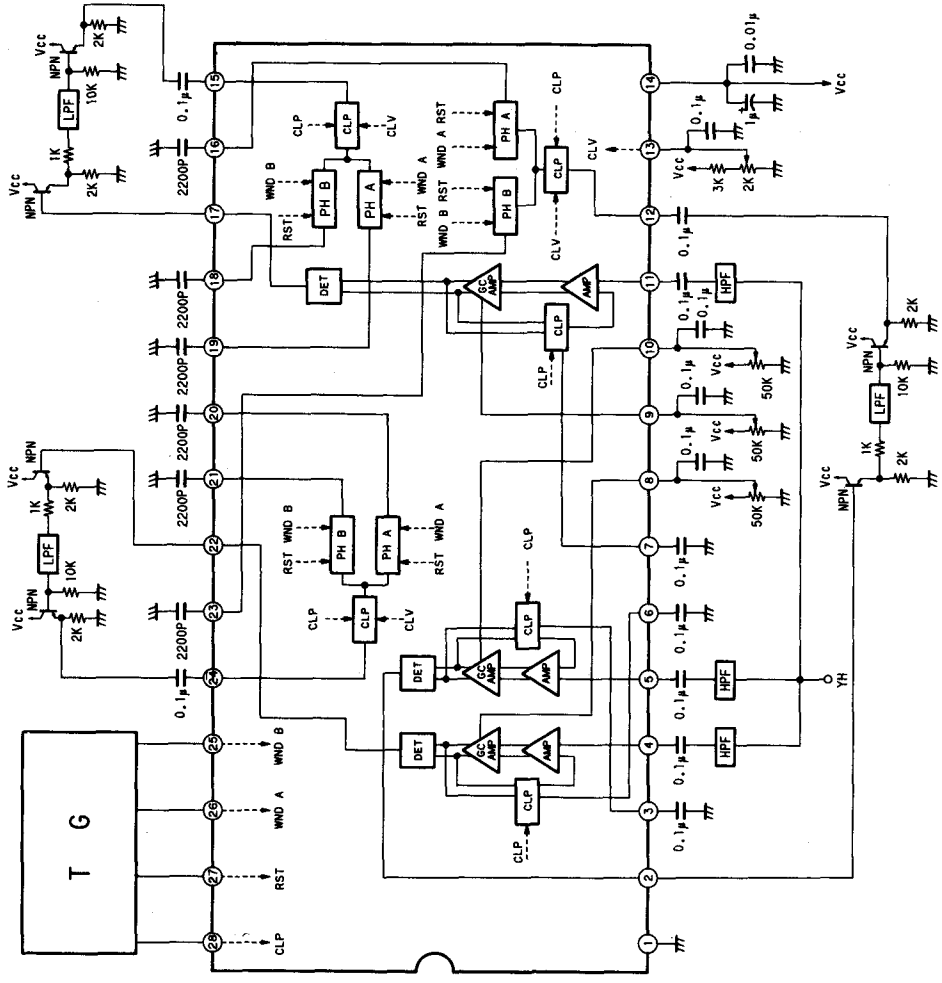
Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{CC}	CLP=RST=$\overline{WNDA}$=$\overline{WNDB}$=GAIN=0V	9	14	23	mA
Amplifier gain min1	Gmin1	Gain=5V, IN=400mV 	—	6	8	dB
Amplifier gain min2	Gmin2		—	6	8	dB
Amplifier gain min3	Gmin3		—	6	8	dB
Amplifier gain max1	Gmax1	Gain=0V, IN=20mV 	30	33	—	dB
Amplifier gain max2	Gmax2		30	33	—	dB
Amplifier gain max3	Gmax3		30	33	—	dB
CLV CLP1A	V_{CLV1A}	CLV=1V, WND=RST=0V, CLP=5V, SW1 : ON Test pin: OUT	0.96	1.00	1.04	V
CLV CLP2A	V_{CLV2A}		0.96	1.00	1.04	V
CLV CLP3A	V_{CLV3A}		0.96	1.00	1.04	V
CLV CLP1B	V_{CLV1B}		0.96	1.00	1.04	V
CLV CLP2B	V_{CLV2B}		0.96	1.00	1.04	V
CLV CLP3B	V_{CLV3B}		0.96	1.00	1.04	V
Reset current 1A	I_{RST1A}	$\overline{WNDA}$=$\overline{WNDB}$=RST=5V, OUT=1V SW2 to SW7: ON Test pin: OUT	110	200	—	μA
Reset current 2A	I_{RST2A}		110	200	—	μA
Reset current 3A	I_{RST3A}		110	200	—	μA
Reset current 1B	I_{RST1B}		110	200	—	μA
Reset current 2B	I_{RST2B}		110	200	—	μA
Reset current 3B	I_{RST3B}		110	200	—	μA

Electrical Characteristics Test Circuit



* Ⓐ indicates current test pins.
  Ⓥ indicates voltage test pins.

Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

The CXA1516 features 3channels for 6dB to 33dB (Typ.) gain control amplifiers, 3channels for double side wave detectors and 3channels ×2 for peak hold circuits.

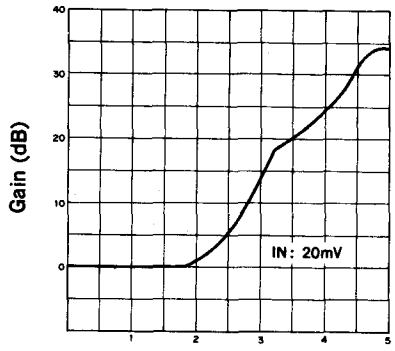
○ Gain control amplifier and double side wave detector

1) The luminance signal passed through HPF, is input to IN after passing through a capacitor.
2) Amplification is executed through a gain control amplifier where the gain is set through GAIN pin.
3) Double side wave detection is performed with output from MIDOUT.
4) Period when CLP is at high is judged as the black input period. Voltage during this period is kept at black level (2.2V Typ.).

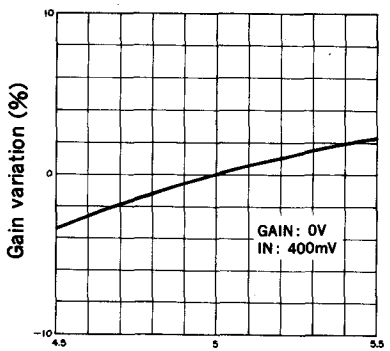
○ Peak hold

5) MIDOUT output is passed through LPF and input to MIDIN after passing through a capacitor.
6) During the period when $\overline{\text{WNDA}}$ and $\overline{\text{WNDB}}$ are at L, peak value input through MIDIN is held at the capacitor connected to OUT. (CLP=RST=L)
7) With CLP at H, voltage applied to CLV (1V: Typ.) is clamped at OUT. (RST=$\overline{\text{WND}}$=L)
8) During the period when RST is at H, the electric load charged to the capacitor connected to OUT, is discharged. ($\overline{\text{WND}}$=H)

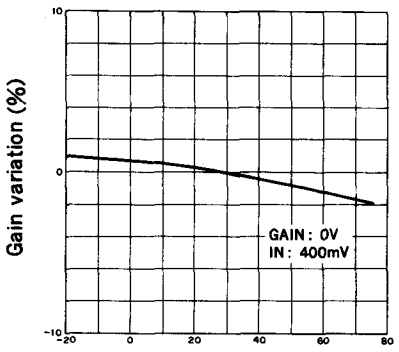
GAIN control characteristics



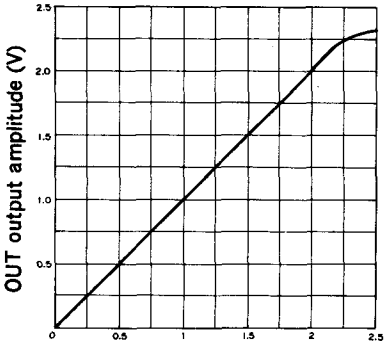
IN—MIDOUT supply voltage characteristics



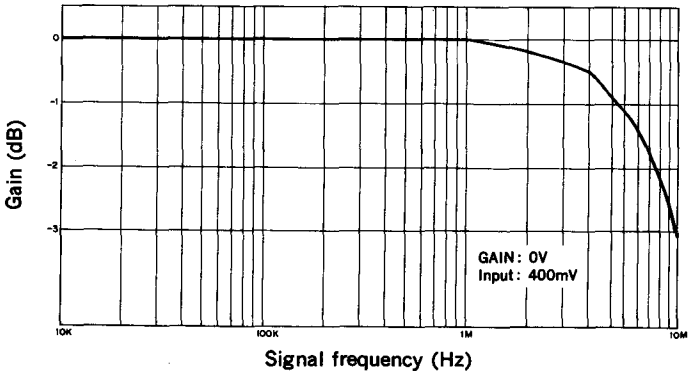
IN—MIDOUT temperature characteristics



MIDIN—OUT I/O characteristics



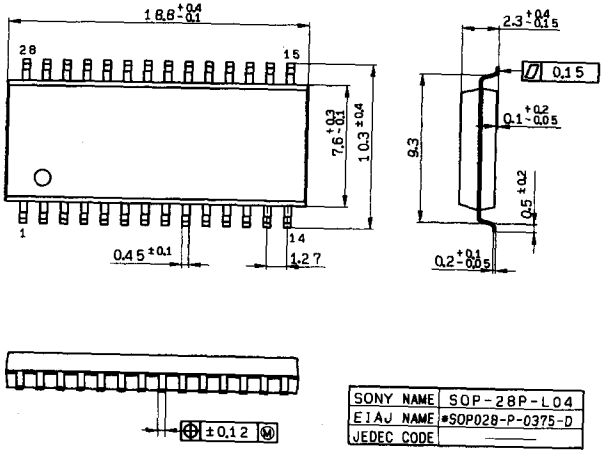
IN—MIDOUT frequency characteristics



Package Outline Unit : mm

CXA1516M

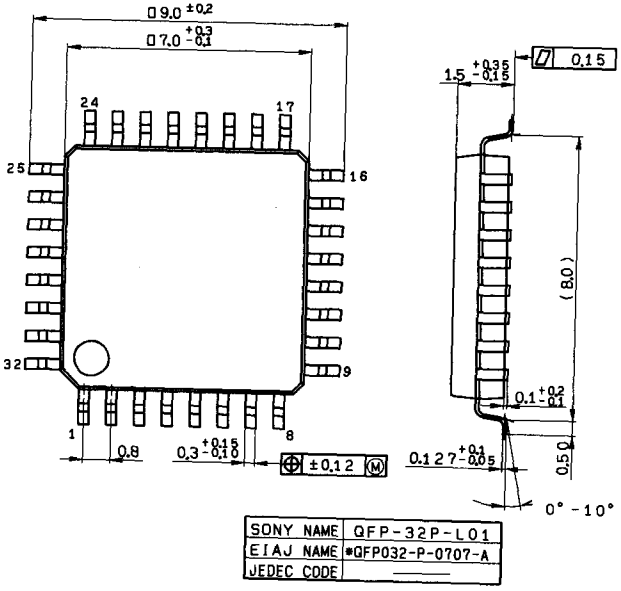
28pin SOP (Plastic) 375mil 0.7g



SONY NAME	SOP-28P-L04
EIAJ NAME	*SOP028-P-0375-D
JEDEC CODE	

CXA1516Q

32pin QFP (Plastic) 0.2g



SONY NAME	QFP-32P-L01
EIAJ NAME	*QFP032-P-0707-A
JEDEC CODE	

SONY

CXA1270N

IC for Vertical Direction Outline Compensation

Description

CXA1270N is a bipolar IC developed for vertical outline compensation of video camera. It contains all the required functions for vertical outline compensation in a single chip. Also, being a small package, this IC is most suitable for the use in video camera.

20pin VSOP (Plastic)

Features

- Low power consumption
- Usable both in 2H type and 1H type.
- Executes low level noise clip.
- Controlable output level.

Structure

Bipolar silicon monolithic IC

Applications

Video camera

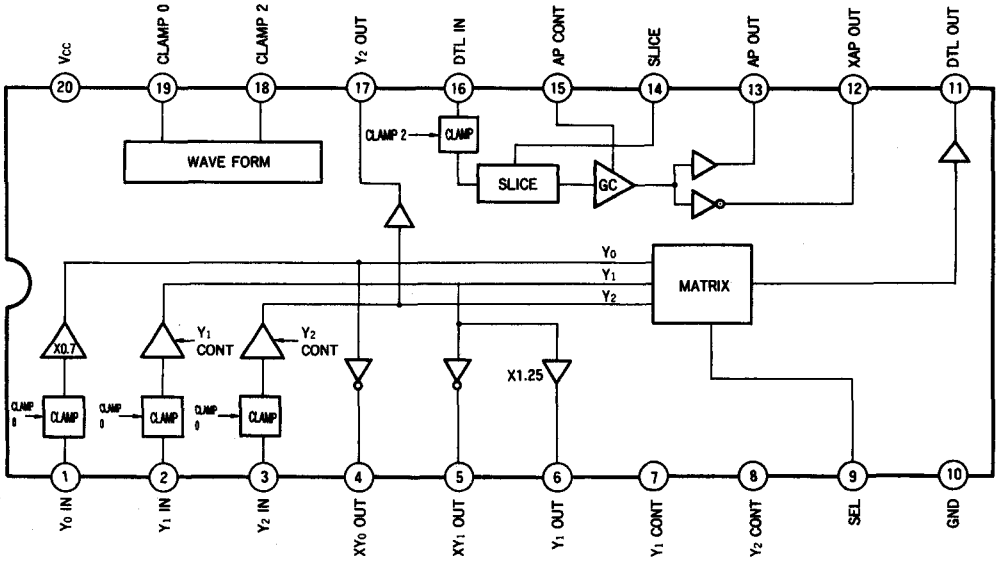
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	10	V
• Storage temperature	T_{stg}	−55 to +150	°C
• Operating temperature	T_{opr}	−20 to +75	°C
• Allowable power dissipation	P_D	375	mW

Recommended Operating Condition

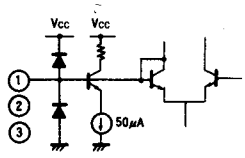
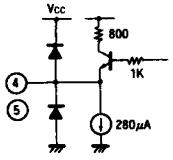
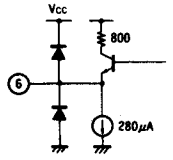
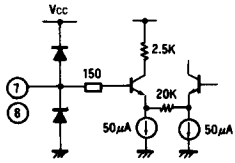
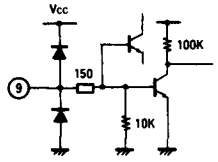
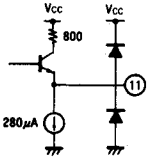
• Supply voltage	V_{CC}	4.75 to 5.25	V

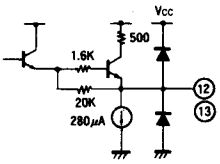
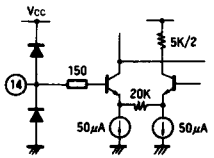
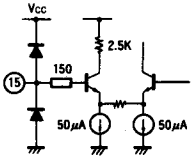
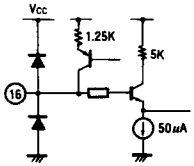
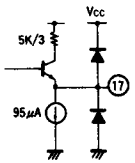
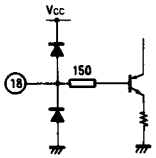
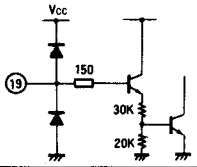
Block Diagram and Pin Configuration



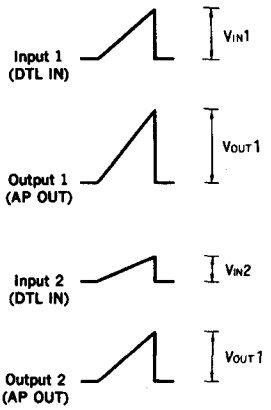
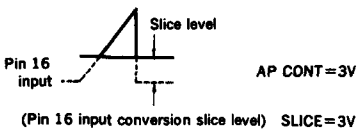
E89631-HP

Pin Description and Equivalent Circuit V_{CC}=5V

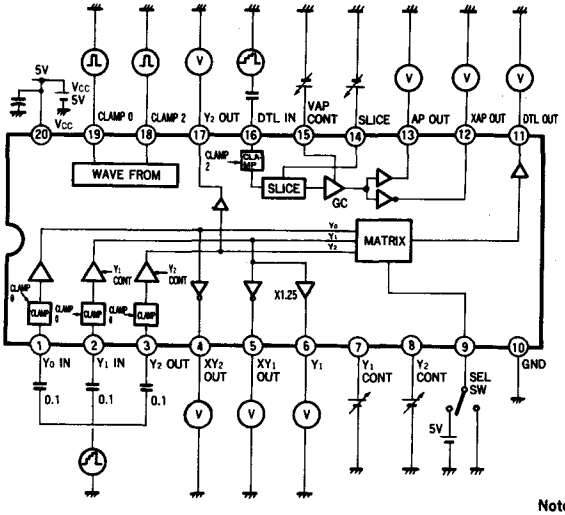
Pin No.	Symbol	Pin voltage	Equivalent Circuit	Description
1	V_0 IN	2.8V (Black level)		Y signal input pin (500Vp-p [Typ.])
2	Y_1 IN	2.8V (Black level)		Y signal input pin (1H delay) (150mVp-p [Typ.])
3	Y_2 IN	2.8V (Black level)		Y signal input pin (2H delay) (150mVp-p [Typ.])
4	XY_0 OUT	2.1V (Black level)		Y_0 A_{mp} inverse output pin
5	XY_1 OUT	2.0V (Black level)		Y_1 A_{mp} inverse output pin
6	Y_1 OUT	2.4V (Black level)		Y_1 A_{mp} output pin
7	Y_1 CONT	1.5V to 3.5V (Outside)		Y_1 A_{mp} gain control pin
8	Y_2 CONT	1.5V to 3.5V (Outside)		Y_2 A_{mp} gain control pin
9	SEL	Low 0V High 5V		Switching pin of 2H mode and 1H mode High (5V)=2H DL mode Low (0V)=1H DL mode
10	GND			GND pin
11	DTL OUT	2.9V		DETAIL signal output

Pin No.	Symbol	Pin voltage	Equivalent Circuit	Description
12	XAP OUT	2.8V		V aperture signal inverse output pin
13	AP OUT	2.8V		V aperture signal output pin
14	SLICE	2V to 4.0V (Outside)		Control pin at SLICE level
15	AP CONT	2V to 4.0V (Outside)		Aperture amplifier (AP AMP) gain control pin
16	DTL IN	3.1V (Black level)		Pin which inputs luminance difference signal (Pin 11) output [Input DTL (DETAIL) OUT signal through external low pass filter.]
17	Y_2 OUT	2.1V		Y_2 A_{mp} output pin
18	CLP2	Pulse		Clamp pulse input pin
19	CLP0	Pulse		Clamp pulse input pin
20	V_{CC}			Supply pin (5V)

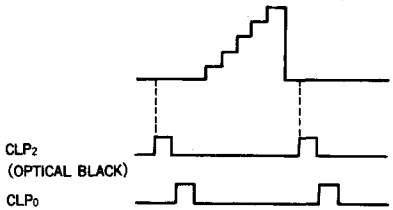
Electrical Characteristics Ta=25°C, V_{CC}=5V

No.	Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
1	Consumption current	ID		6	8	10	mA
2	XY_0 OUT GAIN	XY_0	20 log $\frac{\text{Pin 4 output level}}{\text{Pin 1 input level}}$	−4.6	−3.3	−2.0	dB
3	XY_1 OUT GAIN	XY_1 L	20 log $\frac{\text{Pin 5 output level}}{\text{Pin 2 input level}}$ Y_1 CONT=1.5V			7	dB
		XY_1 H	Y_1 CONT=3.8V	11			dB
4	Y_1 OUT GAIN	Y_1 L	20 log $\frac{\text{Pin 6 output level}}{\text{Pin 5 output level}}$ Y_1 CONT=1.5V	1	2	3	dB
5	Y_2 OUT GAIN	Y_2 L	20 log $\frac{\text{Pin 17 output level}}{\text{Pin 3 input level}}$ Y_2 CONT=1.5V			7	dB
		Y_2 H	Y_2 CONT=3.8V	11			dB
6	AP OUT GAIN	AP	Gain from Pin 16 input to Pin 13 output Conditions { SLICE=0V, AP CONT=1.5V  AP OUT GAIN=20 log $\frac{V_{OUT}\,2-V_{OUT}\,1}{V_{IN}\,2-V_{IN}\,1}$	6			dB
7	SLICE	SL	Slice level= DTL IN−(AP OUT×$\frac{V_{OUT}\,2-V_{OUT}\,1}{V_{IN}\,2-V_{IN}\,1}$)  (Pin 16 input conversion slice level) SLICE=3V	60	100	140	mV

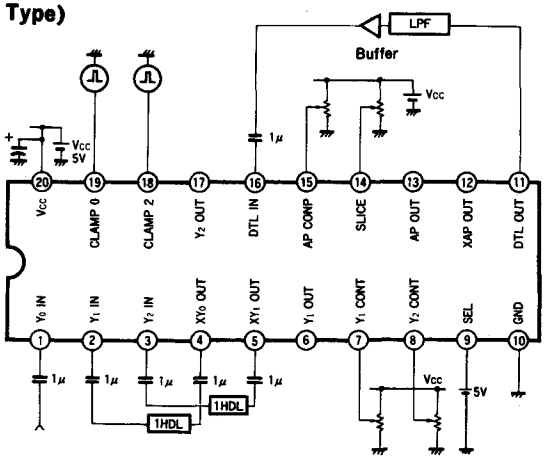
Electrical Characteristics Test Circuit



Note) 1. The unit of capacitor is in μF.
2. V indicate Test Pin.

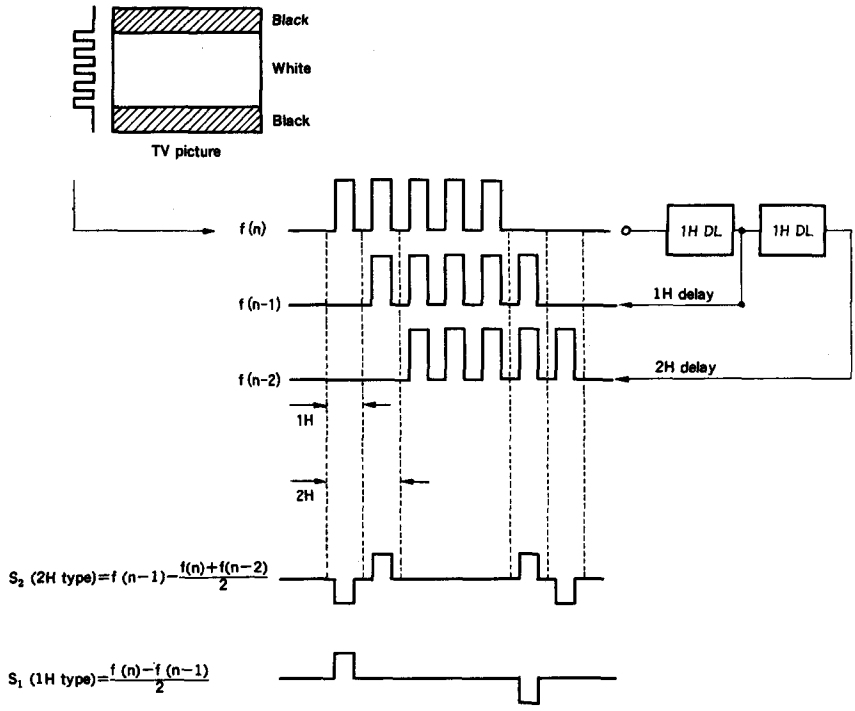


Application circuit (2H Type)



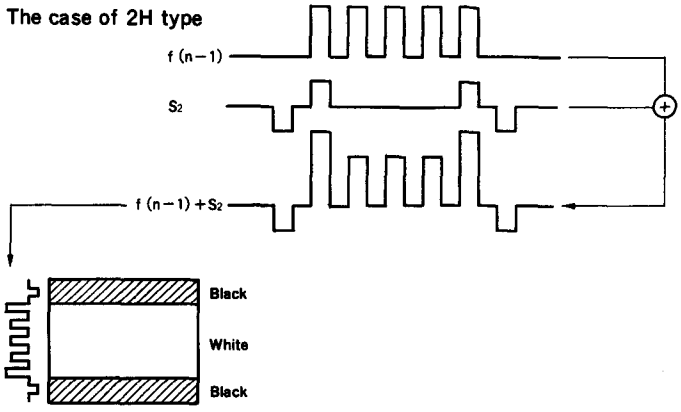
Note) 1. LPF is an abbreviation for Low Pass Filter.
2. DL is an abbreviation for Delay Line
3. DTL is an abbreviation for DETAIL

Operation

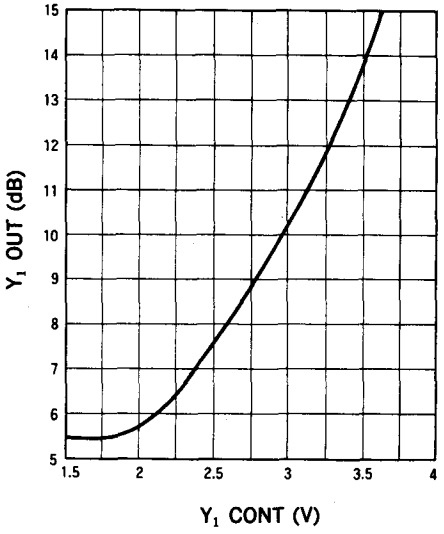


It can execute vertical direction outline emphasis by composing S_1 or S_2 with a Y signal.

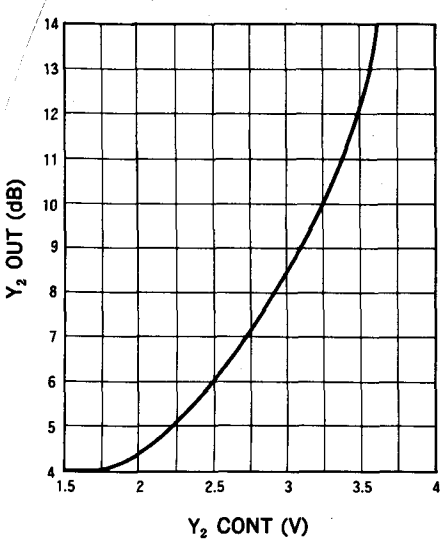
Example) The case of 2H type



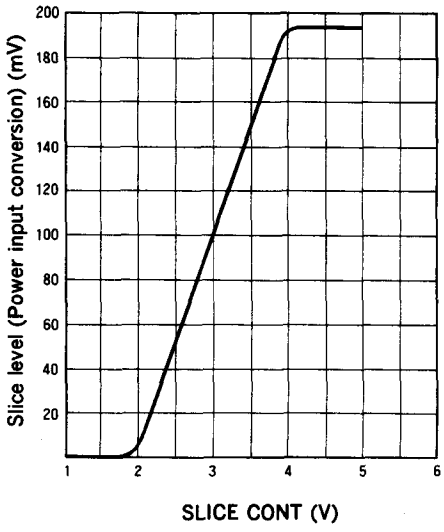
Y_1 Amp control characteristics



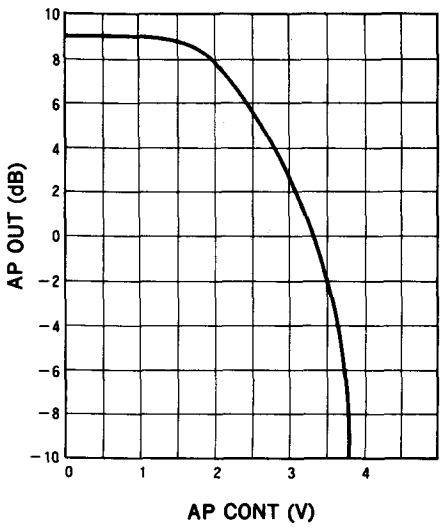
Y_2 Amp control characteristics



Slice level (Power input conversion)



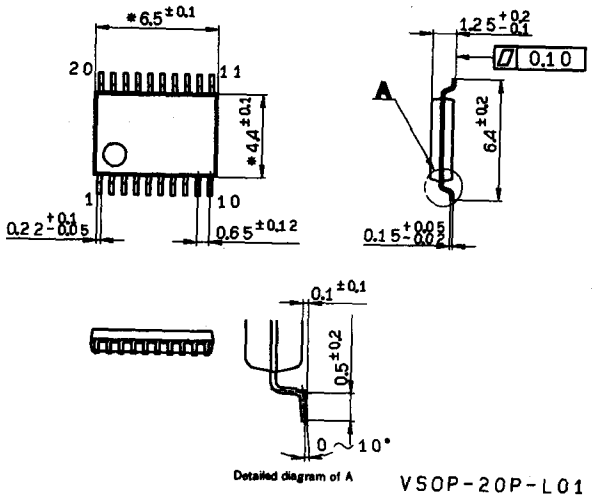
AP Amp control characteristics



Note) See the Electrical Characteristics P.4, No.7

Package Outline **Unit : mm**

20pin VSOP (Plastic) 250mil



Detailed diagram of A

VSOP-20P-L01

Note) Dimensions marked with * do not include residual resin.

SONY

CXA1310AQ

Single Chip Processing for CCD Monochrome Camera

Description

The CXA1310AQ is designed to perform the basic signal processing in CCD monochrome cameras through a single chip. This bipolar IC is most suitable for compact usage and low power consumption.

32 pin QFP (Plastic)

Features

- Processing from CCD output to 75 Ω video output with a single chip
- Wide variable AGC (4 to 32dB Typ.)
- Built-in operational amplifier for AGC loop
- 75 Ω line capacitance minimized using sag compensation function
- Variable white clip level realize wide dynamic range (140IRE)

Structure

Bipolar silicon monolithic IC

Applications

CCD monochrome camera

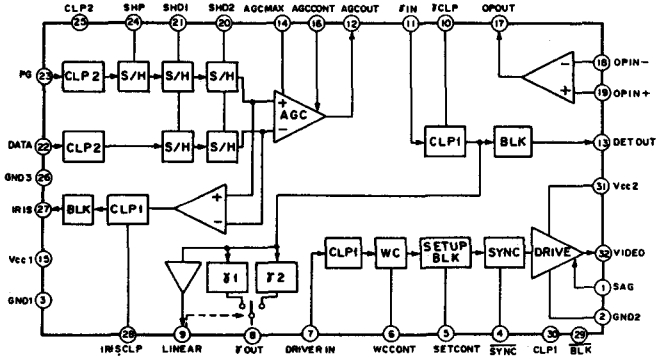
Absolute Maximum Ratings (Ta = 25°C)

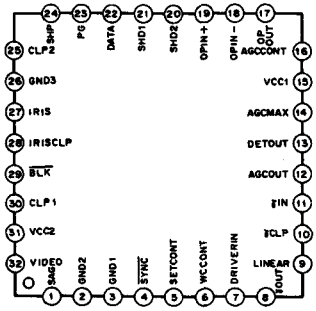
• Supply voltage	Vcc	7	V
• Storage voltage	Tstg	−65 to +150	°C
• Operating temperature	Topr	−20 to +75	°C
• Allowable power dissipation	PD	500	mW

Operating Conditions

Supply voltage	Vcc	4.75 to 5.25	V

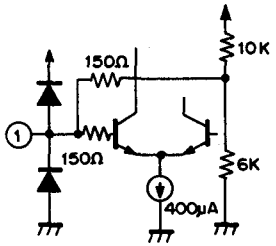
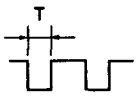
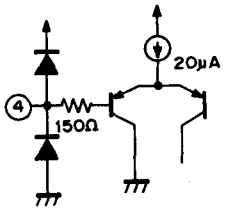
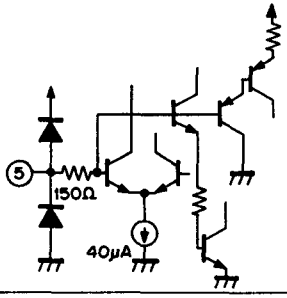
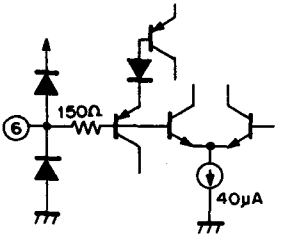
Block Diagram and Pin Configuration



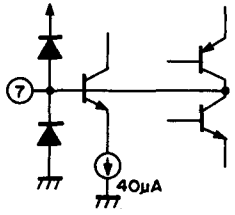
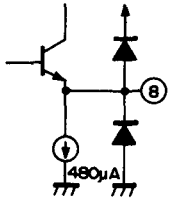
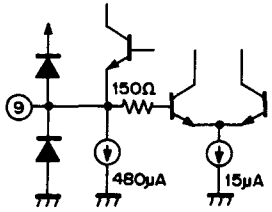
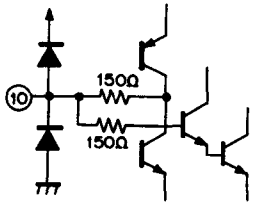


E89910 – ST

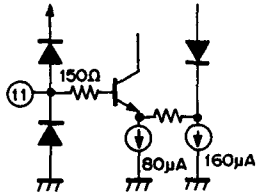
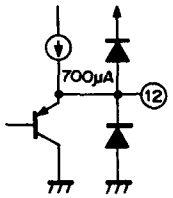
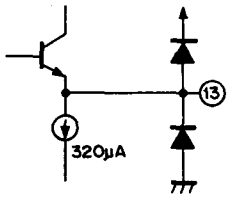
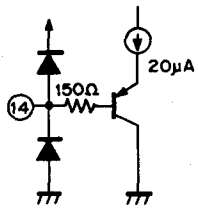
Pin Description

No.	Symbol	I/O signal	Equivalent circuit	Description
1	SAG	Inputs VIDEO OUT through capacitor		Input pin of sag compensation signal
2	GND2	*GND		GND for driver and IRIS
3	GND1	*GND		GND for other than driver and sample hold and IRIS
4	$\overline{\text{SYNC}}$	 * HI : 4.5V and above LO : 0.5V and below T : 5 μs		Sync pulse input pin (active at LO)
5	SET CONT			Set up level adjusting pin
		*GND		Turns to preset mode 1
		*2 to 3.5V		Control mode
		*Vcc		Turns to preset mode 2
6	WC CONT			White clip level adjusting pin
		*GND		Preset mode
		*2 to 3.5V		Control mode

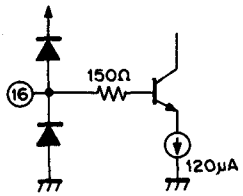
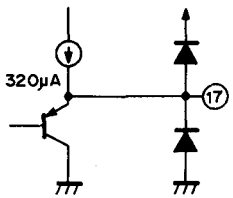
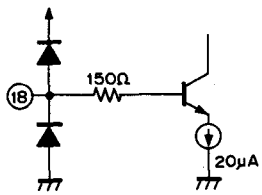
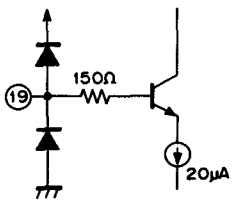
*External applied voltage

No.	Symbol	I/O signal	Equivalent circuit	Description
7	DRIVER IN	Inputs γ OUT through capacitor or LINEAR		Input pin to driver
8	γ OUT	 DC 2V		Gamma compensation signal output pin. Outputs γ 1 when Pin 9 at OPEN outputs γ 2 when Pin 9 turned to 5V
9	LINEAR	 DC 1.8V --- * Vcc		Linear signal (γ-OFF signal) output pin --- Pin 8 output signal turns to γ 2 output
10	γ CLP			Capacitor connecting pin for gamma input clamp

*External applied voltage

No.	Symbol	I/O signal	Equivalent circuit	Description
11	γ IN	Input DC permissible range *DC2 to 3V		Input pin of the gamma compensation circuit
12	AGC OUT	Vpp MAX 1300mV Vpp TYP 500mV DC 2.55V		Output pin of signal passed through AGC
13	DET OUT	MAX 1500mV TYP 500mV DC 2V		Output pin of AGC detection signal
14	AGC MAX	*DC		Maximum gain setting pin of AGC amplifier
15	V_{CC1}	*5V		Power supply for other than driver and IRIS

*External applied voltage

No.	Symbol	I/O signal	Equivalent circuit	Description
16	AGC CONT	*DC		Gain control pin of AGC amplifier
17	OP OUT			Output pin of the operational amplifier
18	OP IN −			Inverted input pin of the operational amplifier
19	OP IN +			Non inverted input pin of the operational amplifier (AGC detection signal input pin)

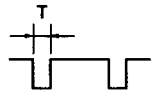
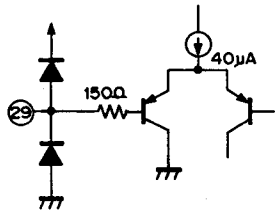
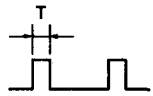
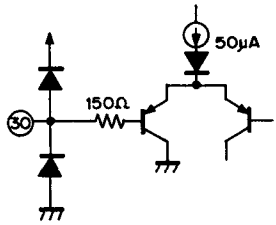
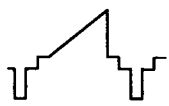
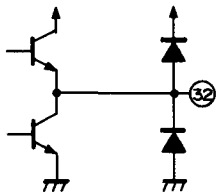
*External applied voltage

No.	Symbol	I/O signal	Equivalent circuit	Description
20	SHD2	T * HI : 4.5V and above LO : 0.5V and below T : 15ns and above	150Ω 100μA 20	Input pin of the sample hold pulse (active at HI)
21	SHD1	T * HI : 4.5V and above LO : 0.5V and below T : 15ns and above	150Ω 100μA 21	Input pin of the sample hold pulse (active at HI)
22	DATA	① ② ①MAX 800mV ②MAX 800mV	150μA 22	CCD signal input pin
23	PG	① ② ①MAX 800mV ②MAX 800mV	150μA 23	CCD signal input pin

*External applied voltage

No.	Symbol	I/O signal	Equivalent circuit	Description
24	SHP	T * HI : 4.5V and above LO : 0.5V and below T : 15ns	100μA 150Ω 24	Input pin of the sample hold pulse (active at HI)
25	CLP2	T * HI : 4.5V and above LO : 0.5V and below T : 2 μs	50μA 150Ω 25	CLP2 pulse input pin (active at HI)
26	GND3	*GND		Sample hold GND
27	IRIS	DC 1.3V	320μA 27	Output pin of the IRIS control signal
28	IRIS CLP		150Ω 150Ω 28	Capacitor connecting pin for IRIS output clamp

*External applied voltage

No.	Symbol	I/O signal	Equivalent circuit	Description
29	$\overline{BLK}$	 * HI : 4.5V and above LO : 0.5V and below T : 11 µs		BLK pulse input pin (active at LO)
30	CLP1	 * HI : 4.5V and above LO : 0.5V and below T : 2 µs		CLP1 pulse input pin (active at HI)
31	Vcc2	*5V		Driver and IRIS power supply
32	VIDEO	 BLK level 1.5V		VIDEO signal output pin

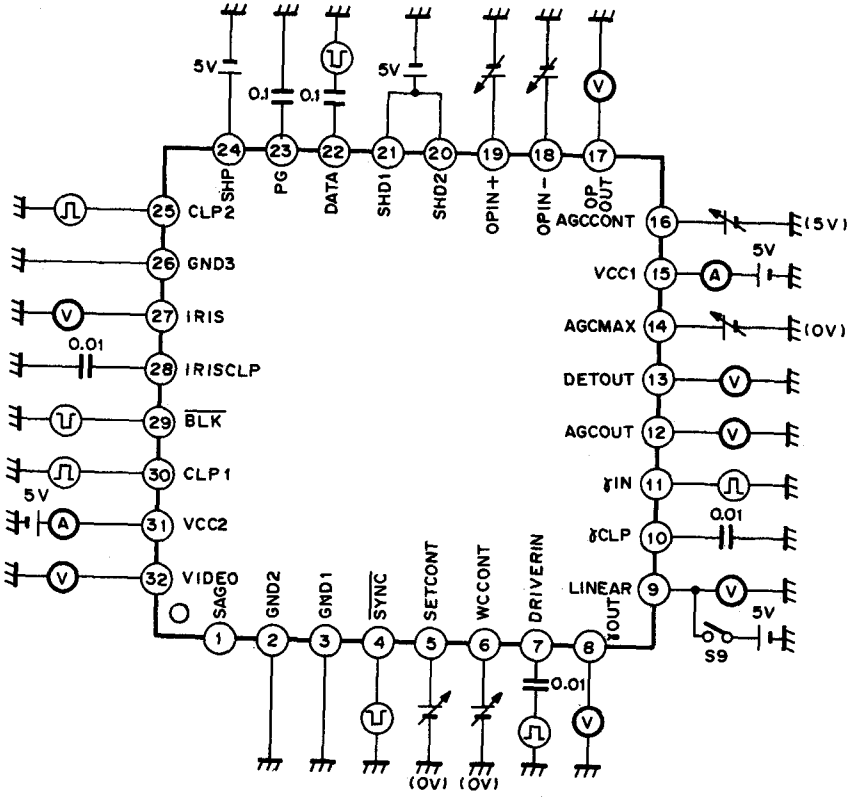
*External applied voltage

Electrical Characteristics (Ta = 25℃, Vcc = 5V, See Electrical Characteristics Test Circuit)

No.	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
1	Current consumption	Icc	Current value of Vcc1 and Vcc2 AGC CONT = 1.5V	30	45	60	mA
2	Min. value of AGC MAX	MAX	GAIN between DATA input and AGC OUT DATA input = 100mV AGC MAX = 4V, AGC CONT = 1.5V	—	18	20	dB
3	Min. value of AGC CONT	AG1	GAIN between DATA input and AGC OUT DATA input = 500mV, AGC CONT = 5V	—	4	6	dB
4	Max. value of AGC CONT	AG2	GAIN between DATA input and AGC OUT DATA input = 30mV, AGC CONT = 1.5V	30	32	—	dB
5	AGC CONT 10dB	AG3	GAIN between DATA input and AGC OUT DATA input = 320mV, AGC CONT = 3.55V	8	10	12	dB
6	AGC OUT DC	ADC	DC output level of AGC OUT	2.25	2.55	2.85	V
7	γ 1 output level	γ 1	Test value of γ 1 output level γ IN input = 500mV	530	630	730	mV
8	γ 2 output level	γ 2	Test value of γ 2 output level γ IN input = 500mV, S9 ON	580	680	780	mV
9	LINEAR AMP GAIN	LG	GAIN between γ IN input and LINEAR γ IN input = 500mV	1.6	2.6	3.6	dB
10	DET OUT DC	DDC	DC output level of DET OUT	1.8	2.0	2.2	V
11	IRIS AMP GAIN	IG	GAIN between DATA input and IRIS DATA input = 300mV	8	10	12	dB
12	IRIS OUT DC	IDC	DC output level of IRIS	1.1	1.3	1.5	V
13	DRIVER GAIN	DG	GAIN between DRIVER IN and VIDEO DRIVER IN = 700mV	5.7	6.0	6.3	dB
14	SYNC level	SY	SYNC level/DG* of VIDEO output	270	293	316	mV
15	SET UP 1	SE1	SET UP level of preset mode 1 SET UP level/DG* of VIDEO output	-15	0	15	mV
16	SET UP 2	SE2	SET UP level of preset mode 2 SET UP level/DG* of VIDEO output	0	20	40	mV
17	Min. value of SET CONT	SE3	SET UP level/DG* of VIDEO output SET CONT = 2V	—	-3	15	mV
18	Max. value of SET CONT	SE4	SET UP level/DG* of VIDEO output SET CONT = 3.3V	80	130	—	mV
19	W-CLIP level	WC1	W-CLIP level/DG* of VIDEO output DRIVER IN = 1500mV, WC CONT = GND	780	820	860	mV
20	Min. value of WC CONT	WC2	W-CLIP level/DG* of VIDEO output DRIVER IN = 1500mV, WC CONT = 2.2V	—	300	600	mV
21	Max. value of WC CONT	WC3	W-CLIP level/DG* of VIDEO output DRIVER IN = 1500mV, WC CONT = 3.3V	1000	1300	—	mV
22	OP AMP output D range Low level	OPL	DC output level of OP OUT OP IN + = 2.5V, OP IN − = 4V	—	0.8	1.2	V
23	OP AMP output D range High level	OPH	DC output level of OP OUT OP IN + = 4V, OP IN − = 2.5V	4.5	4.8	—	V

*Characteristics value at DRIVER GAIN item

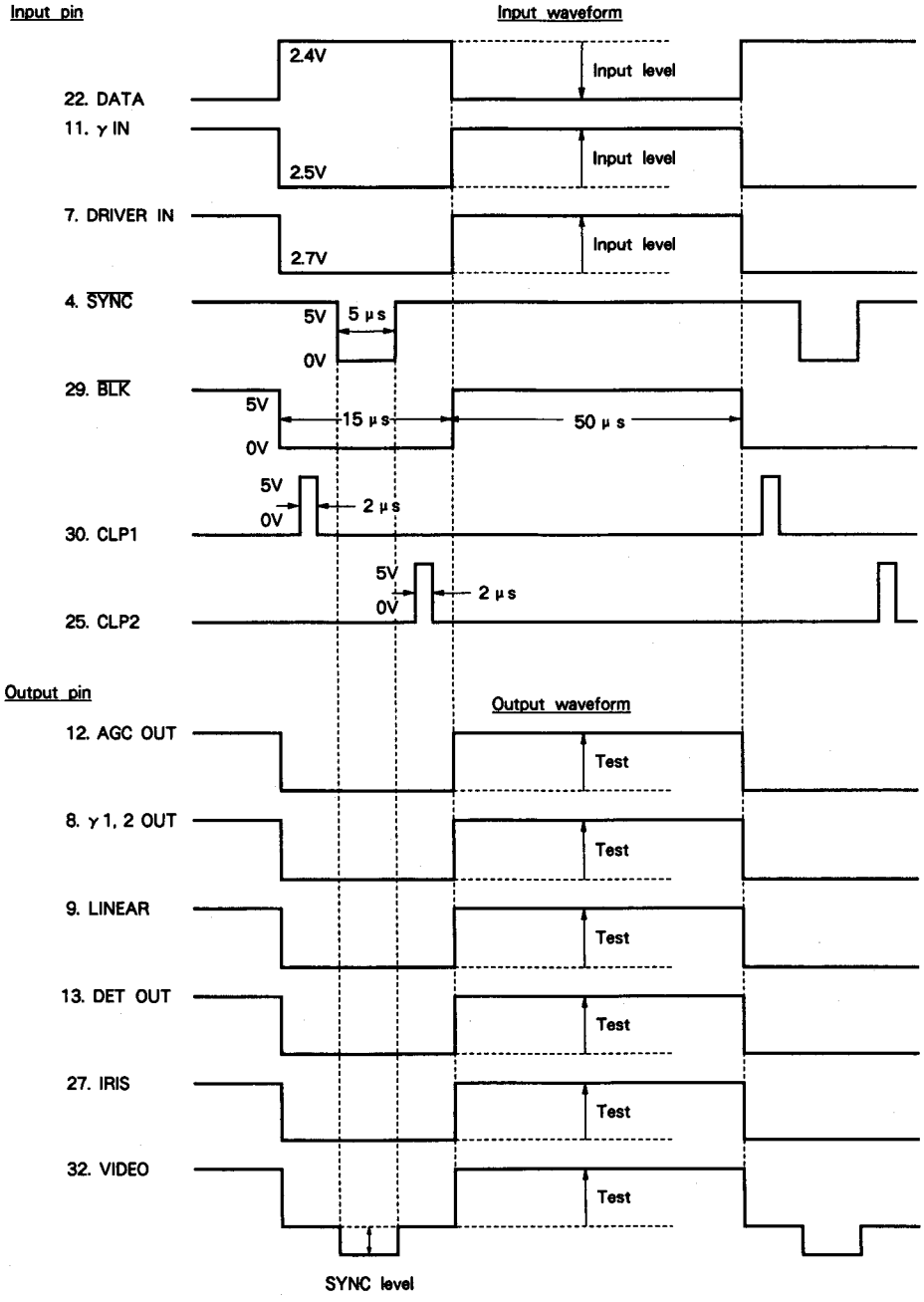
Electrical Characteristics Test Circuit



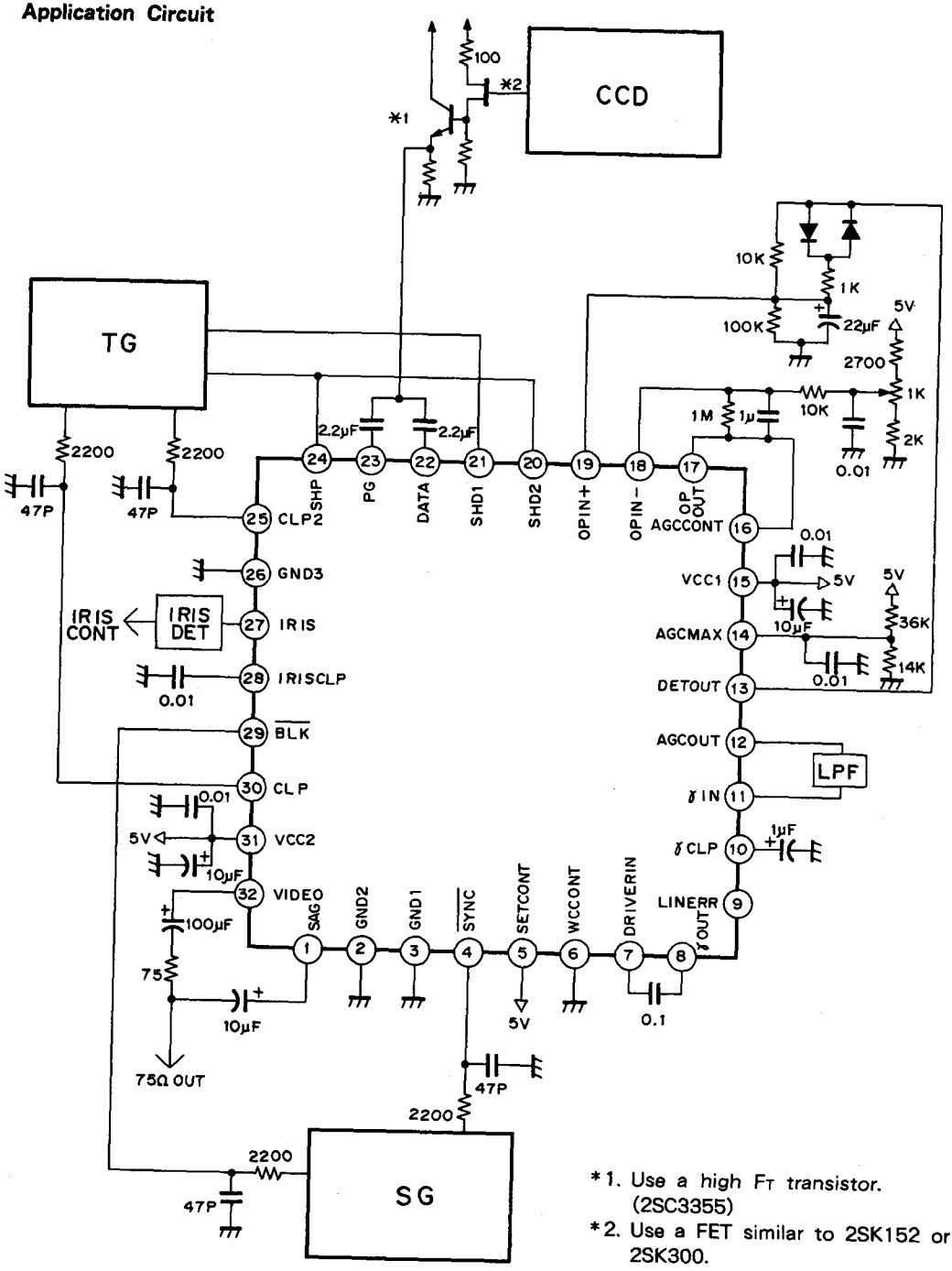
Note)

- μF is the capacitance unit of the capacitor.
- For Pins 5, 6, 14 and 16, apply voltage in brackets unless otherwise specified in the conditions column of the Electrical Characteristics.
- Ⓥ indicates a test pin. (Test AC, DC voltage)
- For Pins 7, 11 and 22, the input signal level is at 0mV, unless otherwise specified in the conditions column of the Electrical Characteristics.

Test Circuit I/O Waveform Diagram



Application Circuit

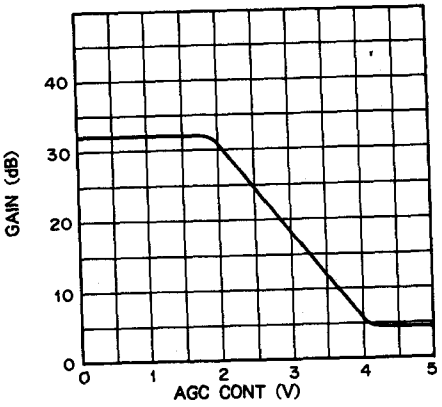


*1. Use a high F_T transistor. (2SC3355)

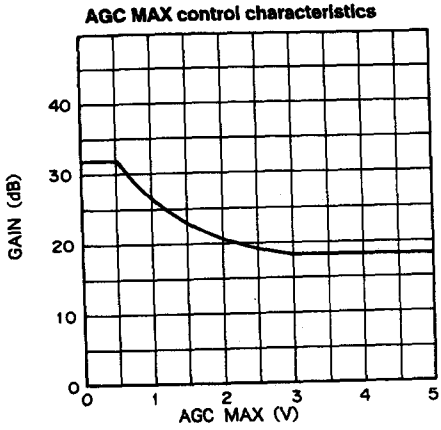
*2. Use a FET similar to 2SK152 or 2SK300.

Representative Characteristics (V_{CC} = 5V, Ta = 25°C)

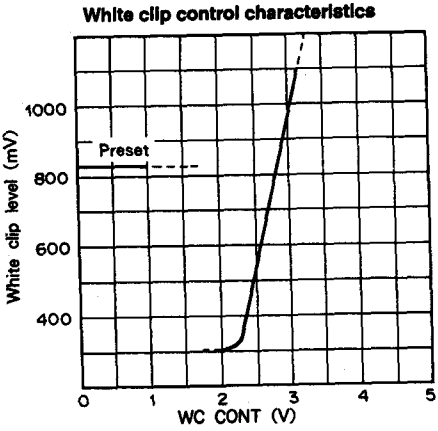
AGC control characteristics



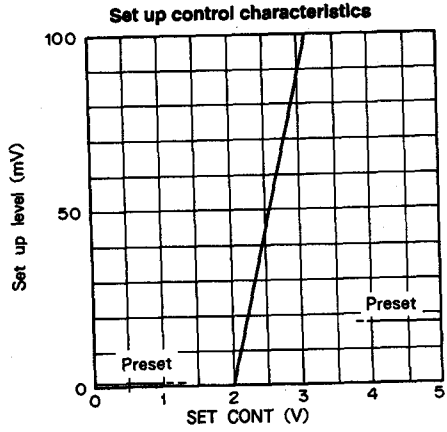
AGC MAX control characteristics



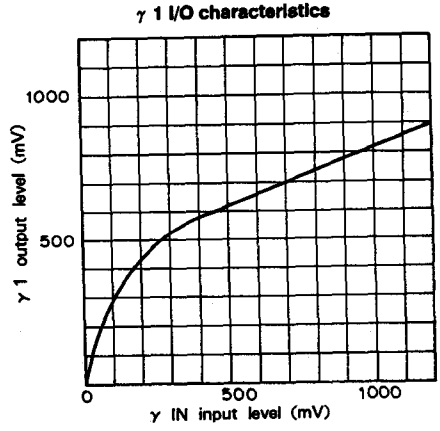
White clip control characteristics



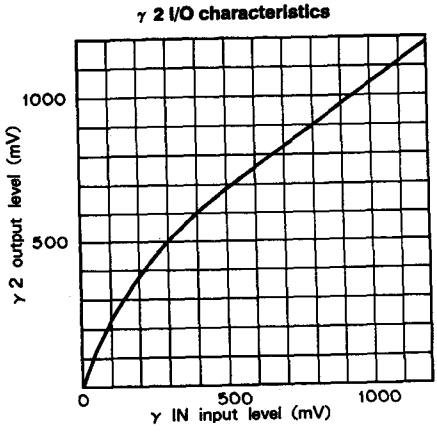
Set up control characteristics



γ 1 I/O characteristics

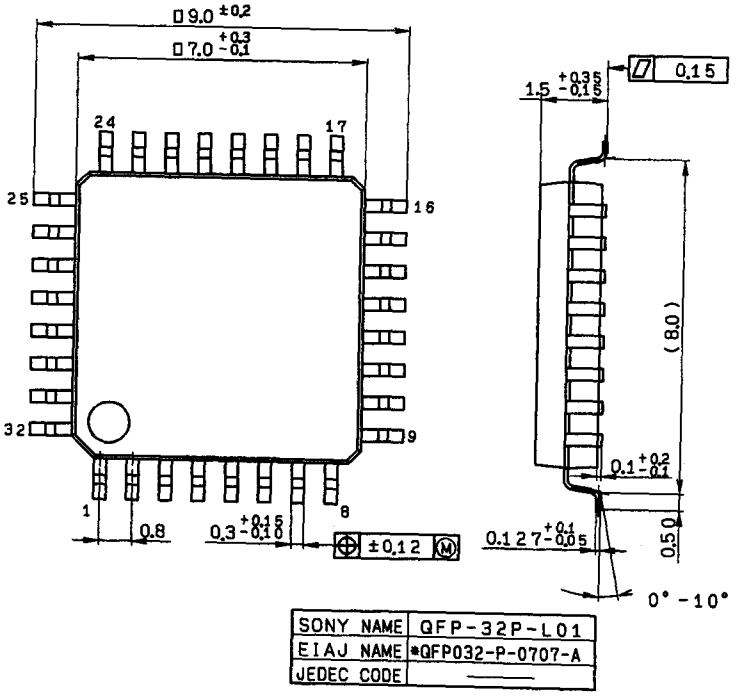


γ 2 I/O characteristics



Package Outline Unit : mm

32 pin QFP (Plastic) 0.2g



SONY NAME	QFP-32P-L01
EIAJ NAME	*QFP032-P-0707-A
JEDEC CODE	

SONY® CXA1337Q-Z/R

Processing system of a CCD Video Cameras

CXA1337Q-Z
48pin QFP (Plastic)

CXA1337R
48pin VQFP (Plastic)

Description

CXA1337Q-Z/R is designed to extract signals from the CCD output of stripe CCD cameras during signal processing.
This bipolar IC executes correlated double sampling, AGC and color separation.

Features

- Through the double sampling function it can inhibit low band noise in CCD signals.
- A wide coverage AGC amplifier enhances the camera sensitivity.
- Has output effective for image making such as : Iris adjustment output and High brightness detection output.

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	10	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	600	mW (QFP)
		950*	mW (VQFP)

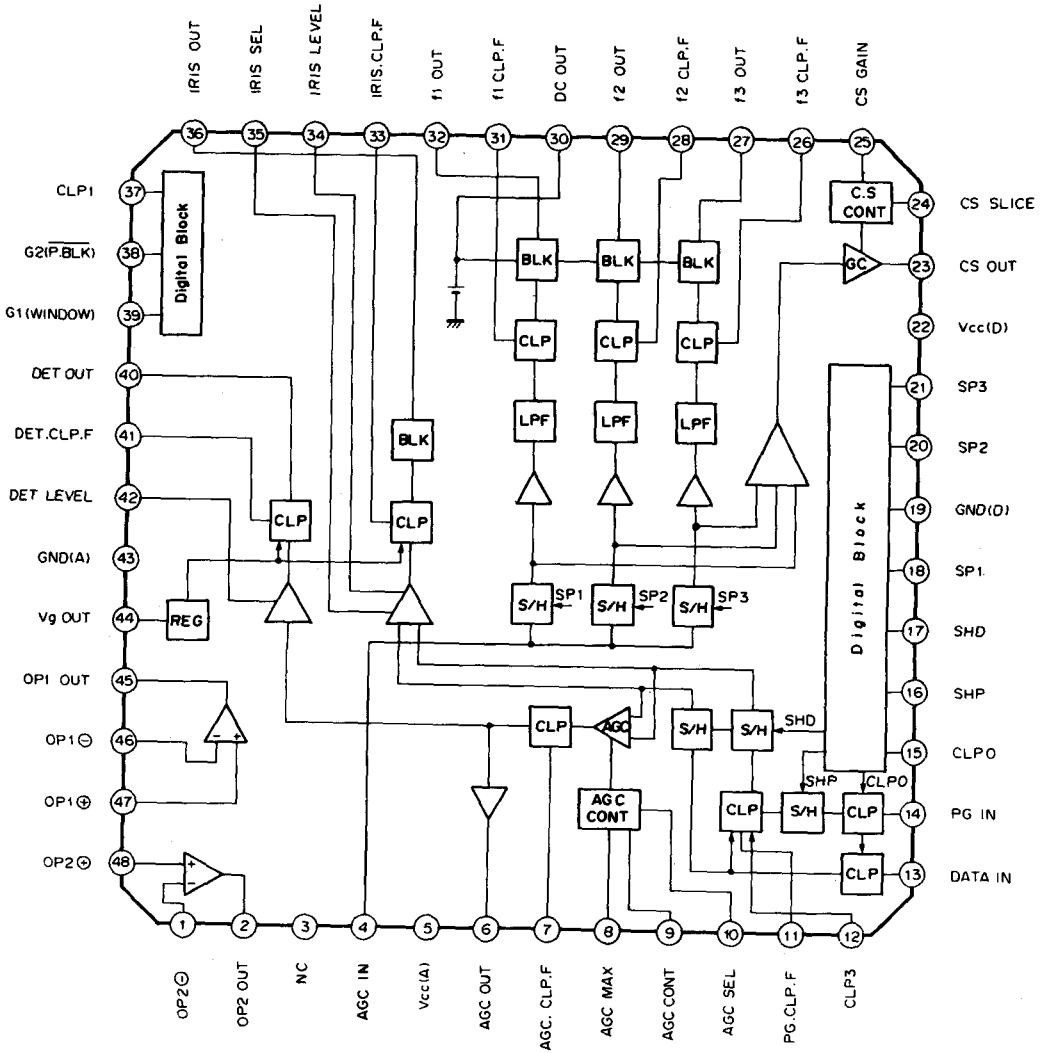
*When mounted on the glass epoxy board
40 mm x 40 mm
t = 0.8 mm

Recommended Operating Conditions

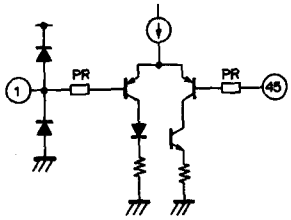
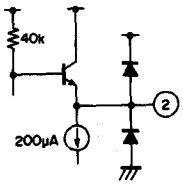
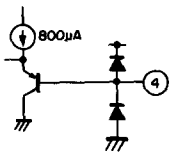
• Supply voltage	Vcc	4.75 to 5.25	V

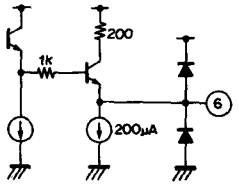
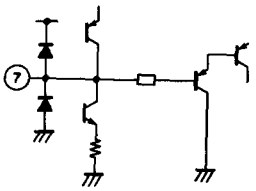
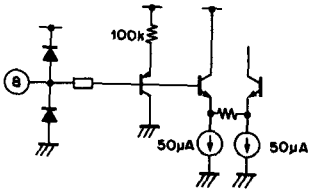
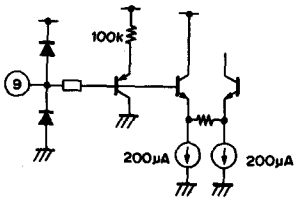
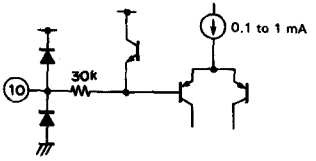
E90111-YA

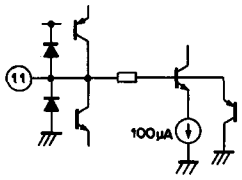
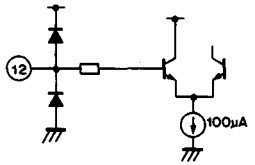
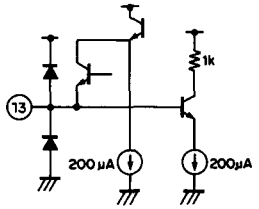
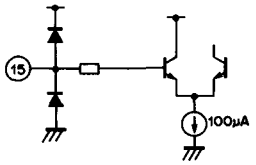
Pin Description

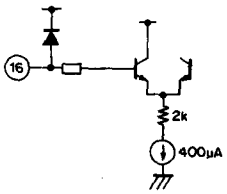
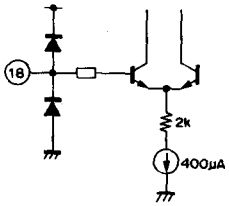


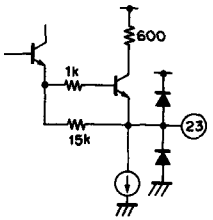
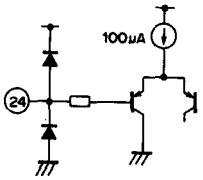
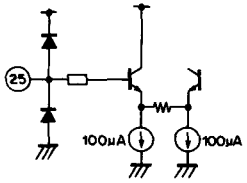
Pin Description and Equivalent Circuit (Vcc = 5V)

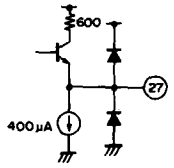
No.	Symbol	Standard DC	Equivalent Circuit	Description
1	OP2 ⊖	0.7 to 3.5V		Inverted operational. amplifier input.
2	OP2 OUT	1 to 4V		Operational amplifier output.
3	N.C.			
4	AGC IN	1.8 V		Color separation input
5	Vcc (A)	5V		Power supply for analog signal processing.

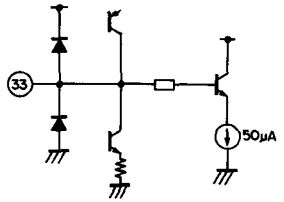
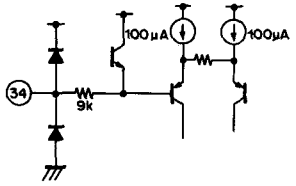
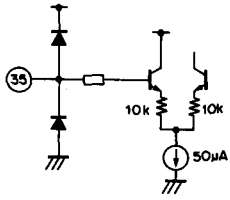
No.	Symbol	Standard DC	Equivalent Circuit	Description
6	AGC OUT	1.8V		AGC amplifier output
7	AGC.CLP.F	2.3V		Connecting pin for the AGC clamping capacitor.
8	AGC.MAX	2 to 4V		Maximum gain control pin for AGC amplifier.
9	AGC CONT	2 to 4V		Gain control pin for AGC amplifier.
10	AGC SEL	0 to 5V		Gain control range shifting pin for the AGC amplifier H: 4V or more, high gain mode L: 1V or less, low gain mode

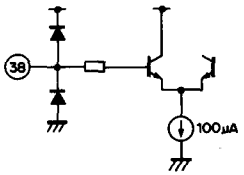
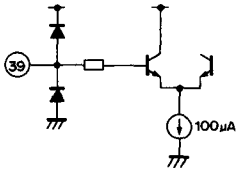
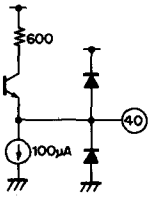
No.	Symbol	Standard DC	Equivalent Circuit	Description
11	PG.CLP.F	3.3V		Pin connecting the CLP 3 clamping circuit capacitor.
12	CLP3	–		CLP 3 pulse input (active H) H: 3V or more L: 2V or less
13	DATA IN	3.3V		CCD signal input
14	PG IN	3.3V	Same as pin 13 (DATA IN)	CCD signal input
15	CLP0	–		CLP 0 pulse input (active H) H: 3V or more L: 2V or less

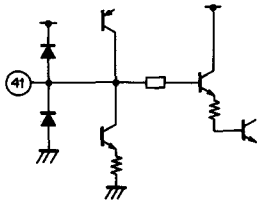
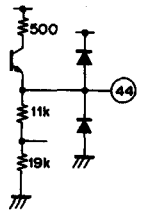
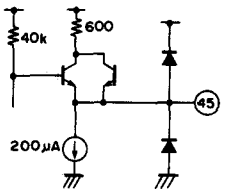
No.	Symbol	Standard DC	Equivalent Circuit	Description
16	SHP	–		SHP pulse input (active H) H: 3V or more L: 2V or less
17	SHD	–	Same as pin 16 (SHP)	SP1 pulse input (active H) H: 3V or more L: 2V or less
18	SP1	–		SP 1 pulse input (active H) H: 3V or more L: 2V or less
19	GND(D)	GND		Ground for digital (pulse) block
20	SP2	–	Same as pin 18 (SPI)	SP2 pulse input (active H) H: 3V or more L: 2V or less

No.	Symbol	Standard DC	Equivalent Circuit	Description
21	SP3	—	Same as pin 18 (SPI)	SP3 pulse input (active H) H: 3V or more L: 2V or less
22	Vcc(D)	5V		Power supply for digital (pulse) block.
23	CS.OUT	2.1V		High brightness detection output.
24	CS.SLICE	1.8 to 3.3V		Level adjustment pin for high brightness detection.
25	CS.GAIN	2 to 4V		Output level adjustment pin for high brightness detection.

No.	Symbol	Standard DC	Equivalent Circuit	Description
26	f_3 CLP.F	1.4V	Same as pin 7 (AGC.CLP.F)	Pin connecting the f_3 output clamping capacitor.
27	f_3 OUT	1.9V		f_3 output (signal output from AGC output, sample-hold and color separated at SP3.)
28	f_2 CLP.F	1.4V	Same as pin 7 (AGC.CLP.F)	Pin connecting the f_2 output clamping capacitor.
29	f_2 OUT	1.9V	Same as pin 27 (f_3 OUT)	f_2 output (signal output from AGC output, sample-hold and color separated at SP2.)
30	DC OUT	1.9V	Same as pin 27 (f_3 OUT)	Black level DC output of f_1, f_2 and f_3 outputs.

No.	Symbol	Standard DC	Equivalent Circuit	Description
31	f_1 CLP.F	1.4V	Same as pin 7 (AGC.CLP.F)	Pin connecting the f_1 output clamping capacitor.
32	f_1 OUT	1.9V	Same as pin 27 (f_3 OUT)	f_1 output (signal output from AGC output, sample-hold and color separated at SP1.)
33	IRIS.CLP.F	3.3V		Pin connecting the iris output clamping capacitor.
34	IRIS.LEVEL	1 to 3V		Iris output gain control pin (effective only when G_1 (pin 39) is L level.)
35	IRIS SEL	0 to 5V		Gain control range shifting pin for iris output. H: 4 V or more, High gain mode L: 1 V or less, Low gain mode

No.	Symbol	Standard DC	Equivalent Circuit	Description
36	IRIS OUT	1.9V	Same as pin 27 (f_3 OUT)	Iris output (iris control signal output)
37	CLP1	—	Same as pin 12 (CLP3)	CLP pulse input (active H) H: 3V or more L: 2V or less
38	G2	—		Blanking pulse input (active L) H: 3V or more L: 2V or less
39	G1	—		Window pulse input (active L) H: 3V or more L: 2V or less
40	DET OUT	1.9V		Detection signal output for AGC loop formation (DET output)

No.	Symbol	Standard DC	Equivalent Circuit	Description
41	DET.CLP.F	3.3V		Pin connecting the detection input clamping capacitor.
42	DET LEVEL	1 to 3V	Same as pin 34 (IRIS LEVEL)	Detection output gain control pin (effective only when G1 (pin 39) is L level.)
43	GND(A)	GND		Ground for analog signal processing.
44	Vg OUT	3V		Regulator output Output current: +1mA (outgoing direction) −80μA (incoming direction)
45	OP1 OUT	1 to 4V		Operational amplifier output

No.	Symbol	Standard DC	Equivalent Circuit	Description
46	CP1 ⊖	0.7 to 3.5V	Same as pin 1 (OP2 ⊖)	Inverted operational amplifier input.
47	OP1 ⊕	0.7 to 3.5V	Refer to pin 1.	Non-inverted operational amplifier input
48	OP2 ⊕	0.7 to 3.5V	Refer to pin 1.	Non-inverted operation amplifier input.

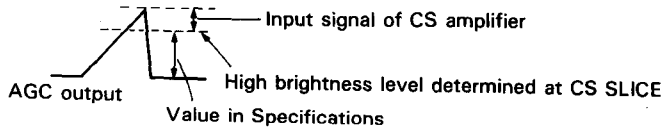
Electrical Characteristics

Vcc = 5V, Ta = 25°C

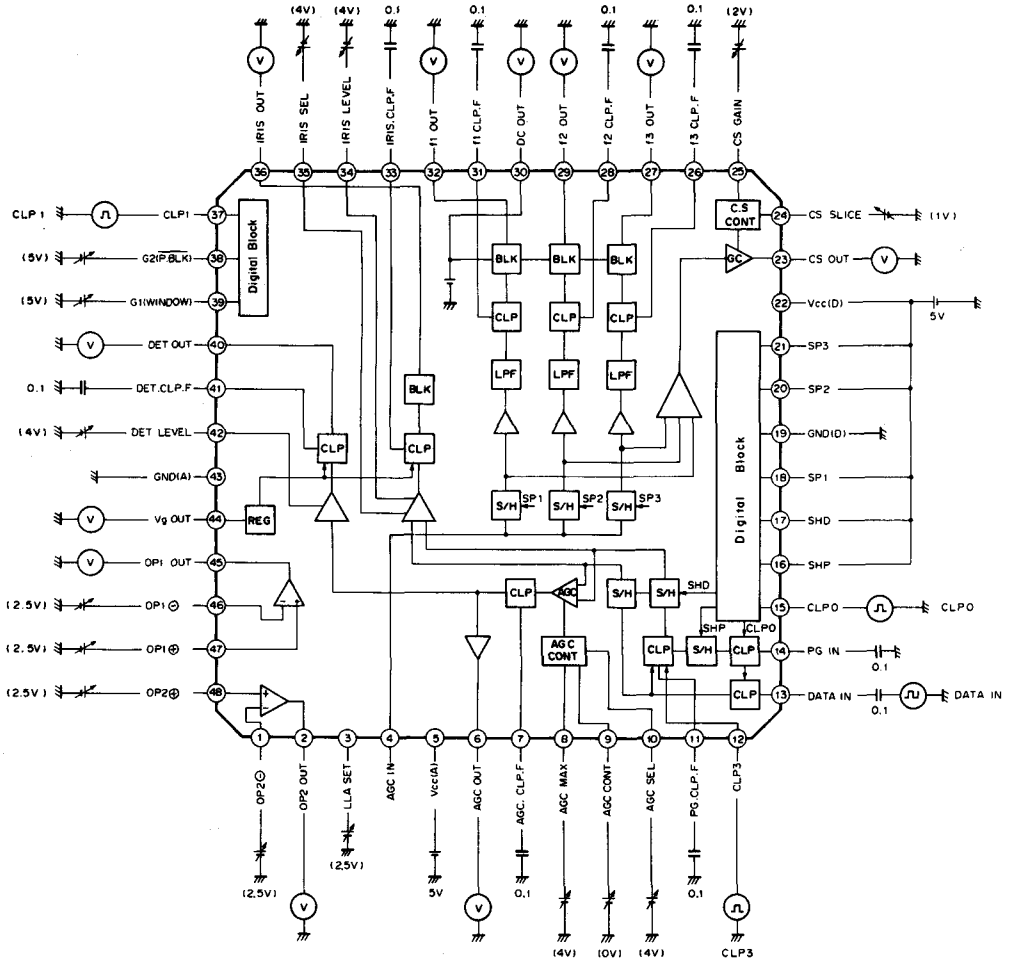
Item	Rate value	Test condition	Min.	Typ.	Max.	Unit
Power consumption	ID		45	60	75	mA
AGC amplifier		AGC OUT/DATA IN				
Gain control	ACONT Min.	AGC CONT = 2V, AGC.MAX = 4V, AGC SEL = 4V	0.5	2	3.5	dB
	ACONT Max.	AGC CONT = 4V, AGC.MAX = 4V, AGC SEL = 4V	28	30	32	dB
Maximum gain control	AMAX Min.	AGC CONT = 4V, AGC.MAX = 2V, AGC SEL = 4V	13.5	15.5	17.5	dB
Low gain mode	AG LOW	AGC CONT = 3V, AGC.MAX = 4V, AGC SEL = 2V	10.7	12.7	14.7	dB
Fixed gain mode	ACONT F	AGC CONT = 0V, AGC.MAX = 4V, AGC SEL = 4V	4.5	6.5	8.5	dB
Fixed maximum gain mode	AMAX F	AGC CONT = 4V, AGC.MAX = 0V, AGC SEL = 4V	19.5	21.5	23.5	dB
Color separator		f1 output/AGC output				
f1 channel gain	f1 G		−1.8	−1	−0.2	dB
Matching between channels	Δf	f2 output/f1 output and f3 output/ f1 output	−0.6	0	+0.6	dB
DC OUT	DC	Output voltage at DC OUTPUT (30-pin)	1.8	1.9	2.0	V
Iris amplifier		Iris output/DATA IN				
Window control	IR Min.	IRIS LEVEL = 1V, G1 = 0V, G2 = 5V, IRIS SEL = 4V			−30	dB
	IR Max.	IRIS LEVEL = 4V, G1 = 0V, G2 = 5V, IRIS SEL = 4V	4	5.5	7.0	dB
Low gain mode	IR LOW	IRIS LEVEL = 4V, G1 = 0V, G2 = 5V, IRIS SEL = 1V	−0.7	0.3	1.3	dB
Clamp voltage	IR DC		1.8	1.9	2.0	V
Maximum output level	IR MAX		1.5			V

Item		Rate value	Test condition	Min.	Typ.	Max.	Unit
Detection amplifier			Detection output/AGC output				
Window control		DET Min	DET LEVEL = 1V, G1 = 0V, G2 = 5V			−30	dB
		DET Max	DET LEVEL = 4V, G1 = 0V, G2 = 5V	−1.5	0	+1.5	dB
Clamp voltage		DET DC		1.8	1.9	2.0	V
Maximum output level		DET Max.		1.4			V
CS amplifier			CS output/AGC output				
Gain control		C CONT Min.	CS GAIN = 2V, CS SLICE = 1V	−5	−3.5	−2	dB
		C CONT Max.	CS GAIN = 4V, CS SLICE = 1V	5.5	7.5	9.5	dB
High brightness detection level (slice control)		SLICE	Detection level calculated as AGC output with 2.5 V CS slice.*	410	570	730	mV
Operational amplifier			Maximum output with no load, OP1 ⊕ − OP1 ⊖ ≧ 10 mV				
OP1	high level	OP1 H		4.1			V
	low level	OP1 L	Minimum output with no load, OP1 ⊕ − OP1 ⊖ ≦ −10 mV	0.9	1.0	1.1	V
OP2	high level	OP2 H	Maximum output with no load, OP2 ⊕ − OP2 ⊖ ≧ 10 mV	4			V
	low level	OP2 L	Minimum output with no load, OP2 ⊕ − OP2 ⊖ ≦ −10 mV			1.1	V
Vg OUT		VG	Regulator output with no load	2.9	3.0	3.1	V
ΔVg		ΔVG	Regulator output variation when Vcc varies from 5V to 4.5V with no load.	−60	−30	0	mV

***Note)** Voltage between the black level of the AGC output (main line signal) and the high brightness level determined by the voltage at CS SLICE pin.

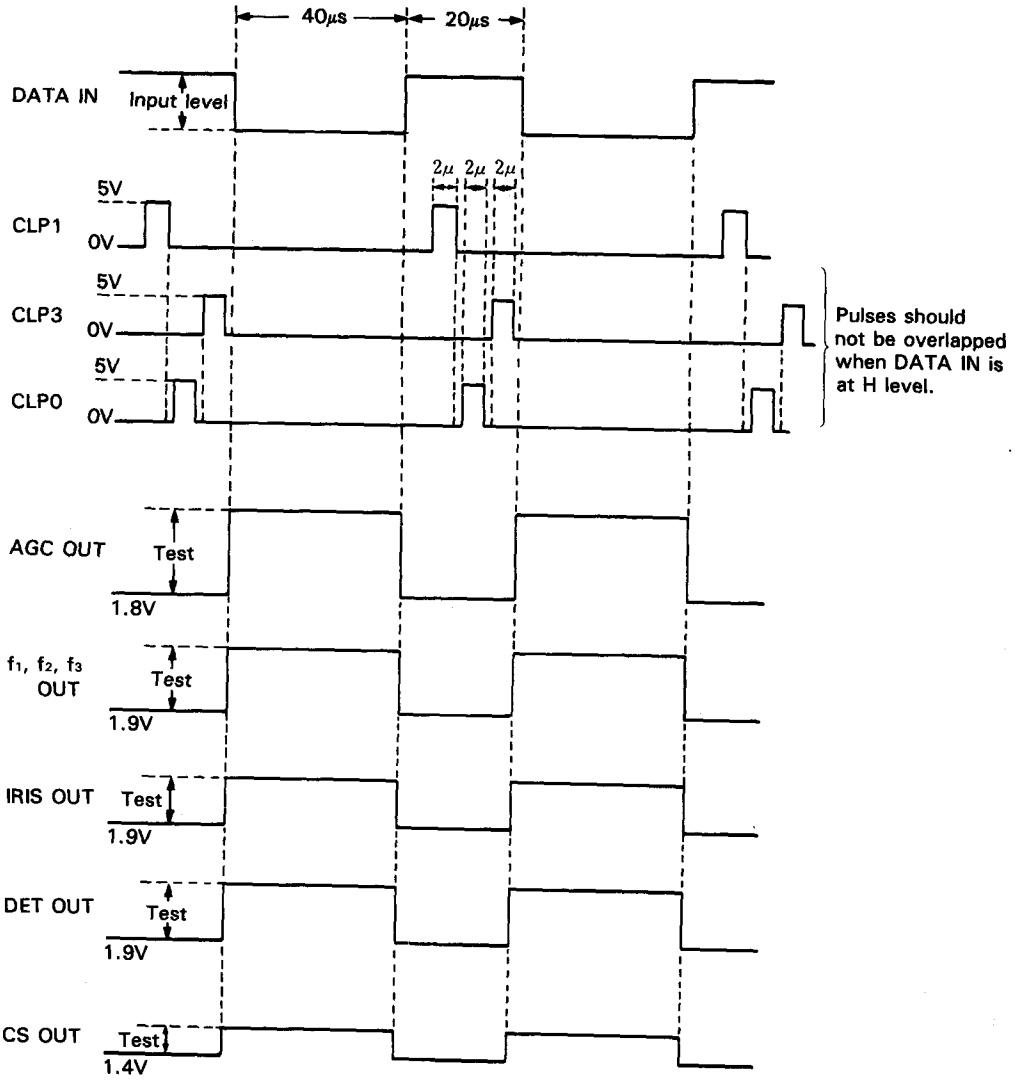


Electrical Characteristics Test Circuit

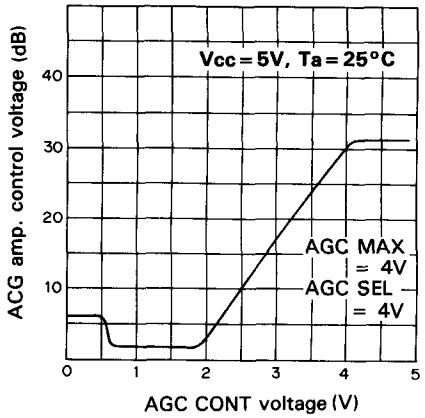


***Note)** 1. The capacitor unit value is μF.
2. Voltages in parentheses are those not specified in "Test condition" of the Electrical Characteristics.
3. Ⓥ indicates a test pin. (Test of AC and DC voltages)

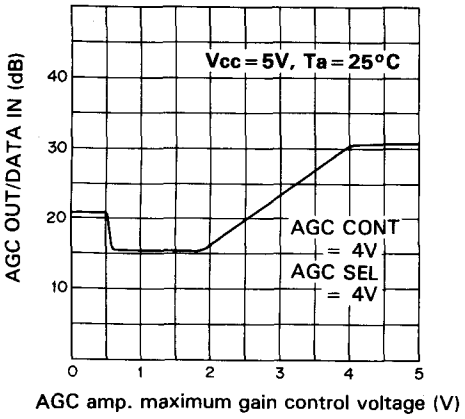
I/O Waveform for the Electrical Characteristics Test Circuit



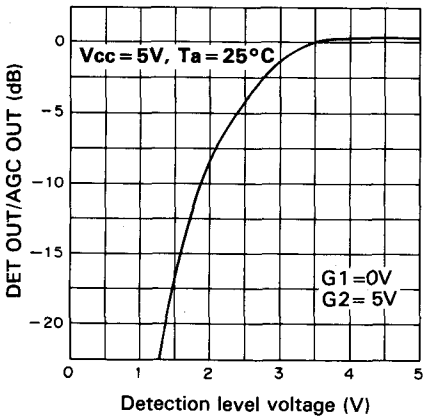
ACG Amplifier gain control characteristics



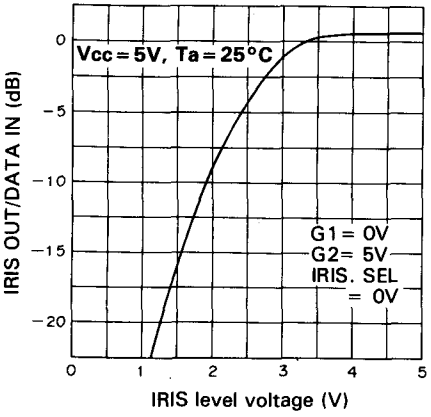
AGC Amplifier maximum gain control characteristics



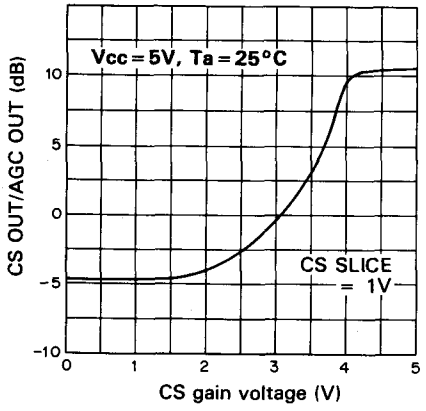
Detection amplifier window control characteristics



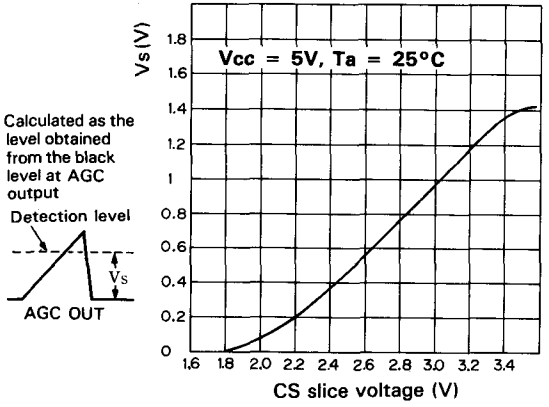
Iris amplifier window control characteristics (low gain mode)



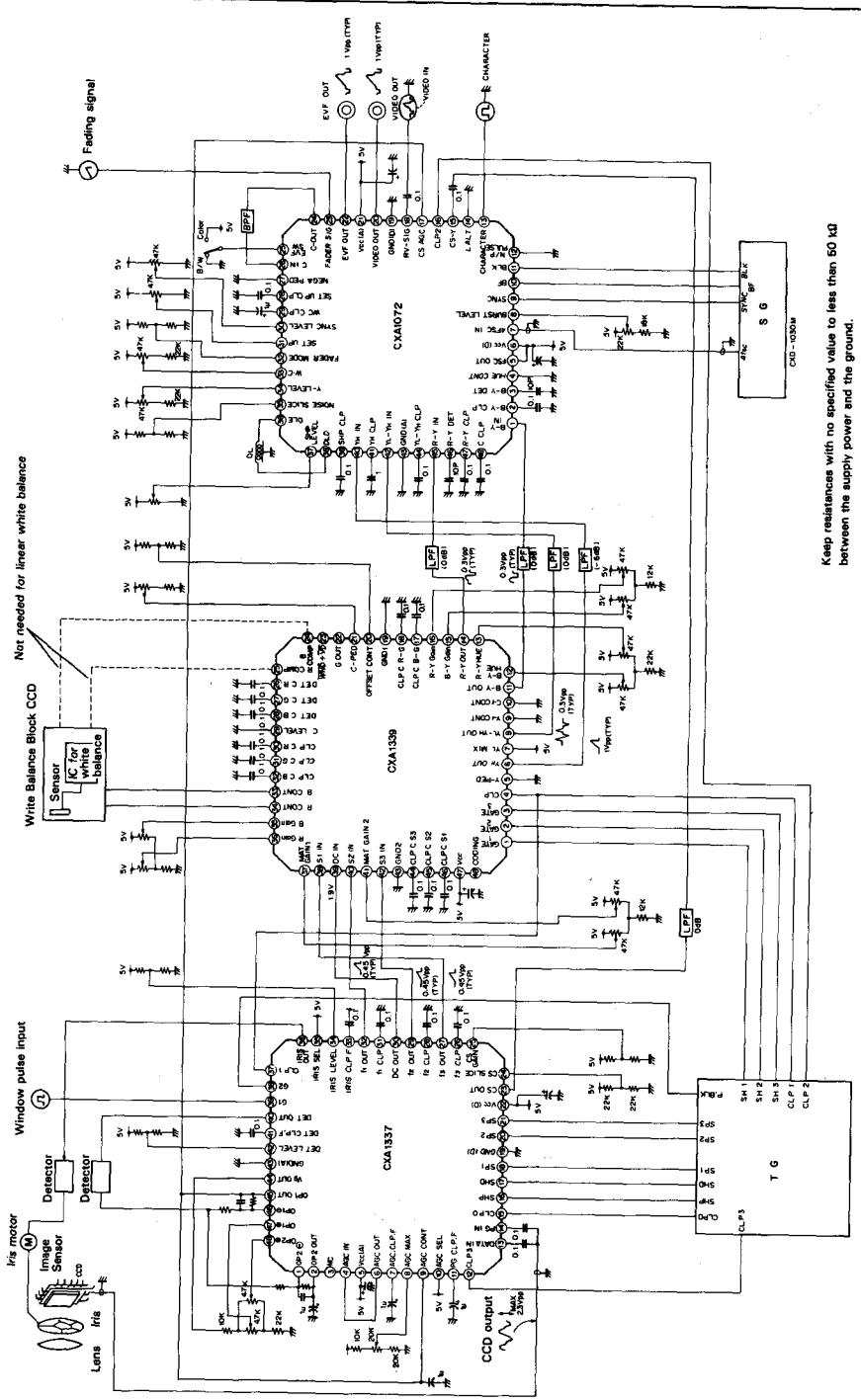
CS amplifier gain control characteristics



CS Amplifier slice control characteristics (high brightness detection level)

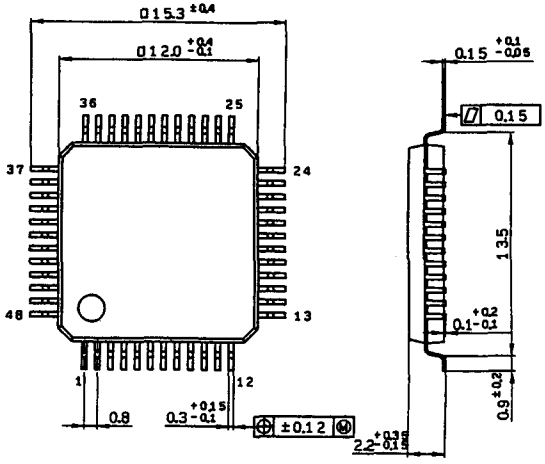


760 H Complementary Color Stripe CCD Video Camera System



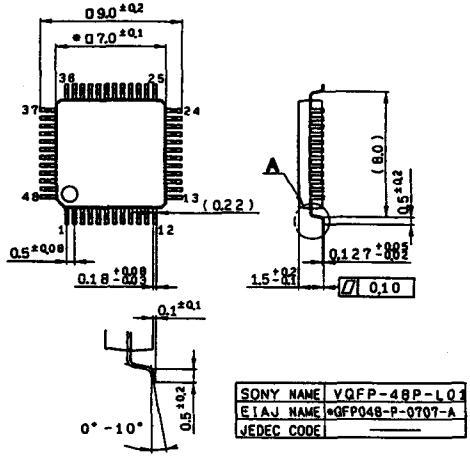
Package Outline Unit: mm

CXA1337Q-Z 48pin QFP (Plastic) 0.7g



SONY NAME	QFP-48P-L04
EIAJ NAME	*QFP048-P-1212-B
JEDEC CODE	———

CXA1337R 48pin VQFP (Plastic) 0.2g



SONY NAME	VQFP-48P-L01
EIAJ NAME	*QFP048-P-0707-A
JEDEC CODE	———

Detailed diagram of A.
Note) Dimension with * mark shows the status without residual resin.

SONY CXA1390AQ/AR

S/H and AGC for CCD Camera

Description

The CXA1390AQ/AR are CCD camera's signal processing ICs which extract signals from the CCD output. These bipolar ICs perform correlated double sampling, AGC, color separation, high luminance detection and others. Additionary, these ICs are not affected by irregular pulses which occure during the CCD shutter mode.

Features

- Pin compatible upgraded version of CXA1390Q/R which can be swapped out while using same peripheral chips.
- Almost completely corrects irregular pulses and their negative affects.
- Correlated double sampling function allows for the suppression of low band noise in the CCD output
- AGC amplifier, which has High S/N ratio and wide gain control range, enhances the camera sensitivity
- Output for iris adjustment. High luminance detection output
- Usage of Vg (regulator) output allows for the formation of IRIS and AGC LOOP which are not affected by supply voltage fluctuation.

Operating Conditions

Supply voltage	Vcc	4.75 to 5.25	V

CXA1390AQ
48 pin QFP (Plastic)

CXA1390AR
48 pin VQFP (Plastic)

Structure

Bipolar silicon monolithic IC

Application

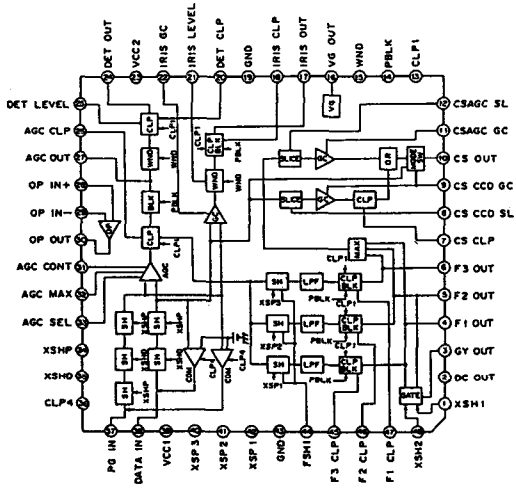
S/H and AGC for CCD camera

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	Vcc	12	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−65 to +150	°C
• Allowable power dissipation			
	PD	600 (QFP)	mW
		950 (VQFP)*	mW

* (40mm × 40mm, t=0.8mm with a mounted glass epoxy substrate)

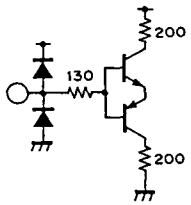
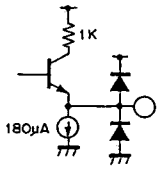
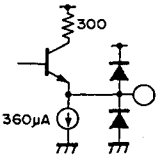
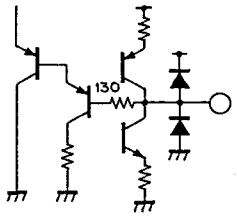
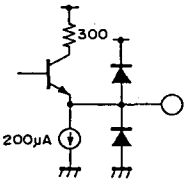
Block Diagram and Pin Configuration (Top View)

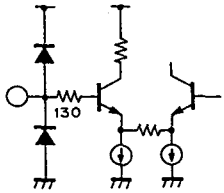
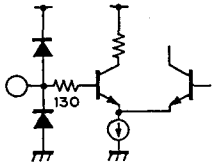
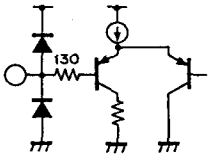
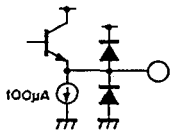


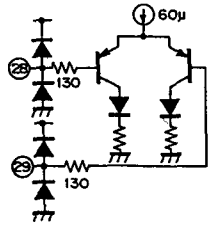
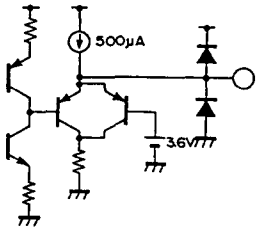
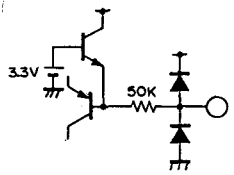
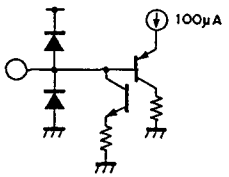
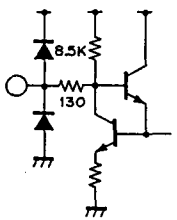
E90941 – ST

Pin Description and Standard Pin Voltage

(Vcc=5V)

No.	Symbol	Voltage	Equivalent circuit	Description
1	XSH1	H: 4V and above L: 1V and below		High speed pulse input pin for S/H (active at L)
34	XSHP			
35	XSHD			
40	XSP3			
41	XSP2			
42	XSP1			
48	XSH2			
2	DC OUT	1.8 to 2.1V		DC output pin of f_1 to f_3 output black level
3	GY OUT	Black level 1.8 to 2.1V		Signal output pin
4	F1 OUT			
5	F2 OUT			
6	F3 OUT			
27	AGC OUT			
7	CS CLP	2.6 to 3.3V		Capacitor connecting pin for clamp
18	IRIS CLP	2.0 to 2.6V		
20	DET CLP	1.9 to 2.6V		
26	AGC CLP	2.3 to 2.8V		
45	F3 CLP	2.0 to 2.6V		
46	F2 CLP	2.0 to 2.6V		
47	F1 CLP	2.0 to 2.6V		
10	CS OUT	1.7 to 2.2V		Signal output pin
17	IRIS OUT	1.7 to 2.0V		Signal output pin Vcc fluctuations effect is minor on DC level
24	DET OUT	1.7 to 2.0V		

No.	Symbol	Voltage	Equivalent circuit	Description
8	CS CCD SL	(Test mode at 0V)		Level adjustment pin of high luminance detection pin of the input signal
9	CS CCD GC			Gain adjustment pin of input signal high luminance part
11	CSAGC GC			Gain adjustment pin of high luminance part after AGC
12	CSAGC SL			Level adjustment pin of high luminance detection after AGC
21	IRIS LEVEL			Adjustment pin of IRIS output weighting (Active at WND=L)
22	IRIS GC			Gain adjustment pin of IRIS output
25	DET LEVEL			Adjustment pin of DET output weighting (Active at WND=L)
31	AGC CONT			AGC amplifier gain adjustment pin
32	AGC MAX			AGC amplifier MAX gain adjustment pin
13	CLP1	H: 4V and above L: 1V and below		CLP1 pulse input pin Active at H (OPB clamp)
14	P BLK			Pre BLK pulse input pin Active at L
15	WND			Window pulse input pin Active at L
36	CLP4			CLP4 pulse input pin Active at H
16	VG OUT	2.6 to 3.1V		Regulator output pin (Used for the formation of AGC and IRIS loop)

No.	Symbol	Voltage	Equivalent circuit	Description
28	OP IN+	1 to 3.3V		Operation amplifier non inverted input pin
29	OP IN −			Operation amplifier inverted input pin
30	OP OUT	H: 4.2V and above L: 1.2V and below		Output pin
33	AGC SEL	Vcc: Low gain mode GND: High gain mode		AGC amplifier gain selection pin
37 38	PG IN DATA IN	Black level 2.7 to 3.2V		CCD signal input pin
44	FSHI	1.4 to 1.8V		Adjustment pin for color separation S/H follow up speed (Normally used OPEN)

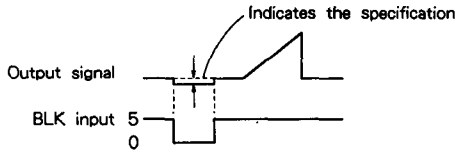
Electrical Characteristics

(Ta=25°C, Vcc=5.0V)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption		ID		32	48	65	mA
AGC	CONT Min.	ACON Min.	AGC OUT/DATA IN AGC CONT=1.5V AGC MAX=5V AGC SEL=0V		6	8	dB
	CONT Max.	ACON Max.	AGC OUT/DATA IN AGC CONT=4.5V AGC MAX=5V AGC SEL=0V	30	32		dB
	Max. Min.	MAX Min.	AGC OUT/DATA IN AGC CONT=4.5V AGC MAX=1.5V AGC SEL=0V		17	20	dB
	Gain shift	GSHI	AGC OUT (SEL=5V)/AGC OUT (SEL=0V)	−5	−4	−3	dB
	BLK offset	Δ BLK	Note 1)	−10	0	+10	mV
Color separation	Gain	f Gain	Color separation output/AGC OUT (f_1, f_2, f_3)	−0.5	0	+0.5	dB
	BLK offset	f Δ BLK	Note 1)	−10	0	+10	mV
DC OUT		DC		1.8	1.95	2.1	V
Gate gain		GY	GY OUT/AGC OUT	−0.5	0	+0.5	dB
IRIS	Gain Cont Max.	IR Max.	IRIS OUT/DATA IN IRIS GC=5V WND=5V	18	22		dB
	Gain Cont Min.	IR Min.	IRIS OUT/DATA IN IRIS GC=1.5V WND=5V		4	8	dB
	Window Level Max.	IRW Max.	Gain Cont Max. ratio (attenuation) IRIS GC=1.5V IRIS LEVEL=5V WND=0V	−1	0		dB
	Window Level Min.	IRW Min.	Gain Cont Max. ratio (attenuation) IRIS GC=1.5V IRIS LEVEL=1.5V WND=0V			−14	dB
DET	Gain	DET G	DET OUT/AGC OUT WND=5V	−2	−1	+0.5	dB
	Window Level Max.	DET Max.	DET OUT/AGC OUT DET LEVEL=5V WND=0V	−2	−1	+0.5	dB
	Window Level Min.	DET Min.	Level Max. ratio DET LEVEL=1.5V WND=0V			−13	dB

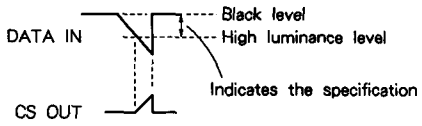
Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
CS CCD	Max. Gain	CSC Max.	CS OUT differential/DATA IN differential CS CCD SL=4.1V CS CCD GC=5V PBLK=0V	13	16		dB
	Min. Gain	CSC Min.	CS OUT differential/DATA IN differential CS CCD SL=4.1V CS CCD GC=1.5V PBLK=0V		–1	1	dB
	Max. SLICE	CSC Max. SL	Input conversion slice level CS CCD SL=1.5V Note 1)	0.7			V
	Min. SLICE	CSC Min. SL	Input conversion slice level CS CCD SL=5V Note 1)		40	100	mV
CS AGC	Max. Gain	CSA Max.	CS OUT DATA IN=0.2Vpp CS AGC GC=5V CS AGC SL=4.2V CS CCD GC=1.5V CS CCD SL=1.5V Note 2)	0.5			Vpp
	Min. Gain	CSA Min.	CS OUT differential/ AGC OUT differential CS AGC GC=1.5V CS AGC SL=4.2V CS CCD GC=1.5V CS CCD SL=1.5V Note 2)		–1	1	dB
	Max. SLICE	CSA Max. SL	AGC OUT conversion CS AGC SL=1.5V Note 3)	1.2			V
	Min. SLICE	CSA Min. SL	AGC OUT conversion CS AGC SL=5V Note 3)		0.06	0.1	V
TEST mode		TEST	DATA IN=0.5Vpp CS CCD GC=0V Note 4)		0.5		Vpp
OP-Amp	H level	OPH	OP IN+=2.1V OP IN–=2.0V	4.2			V
	L level	OPL	OP IN+=2.0V OP IN–=2.1V		0.9	1.2	V
Vg OUT		Vg	At no load	2.6	2.85	3.1	V

Note 1)



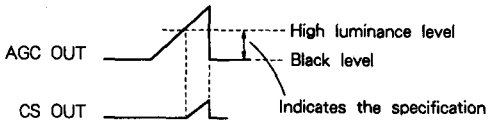
Note 2)

Voltage between DATA IN input black level and the high luminance level determined by CS CCD SL pin voltage.



Note 3)

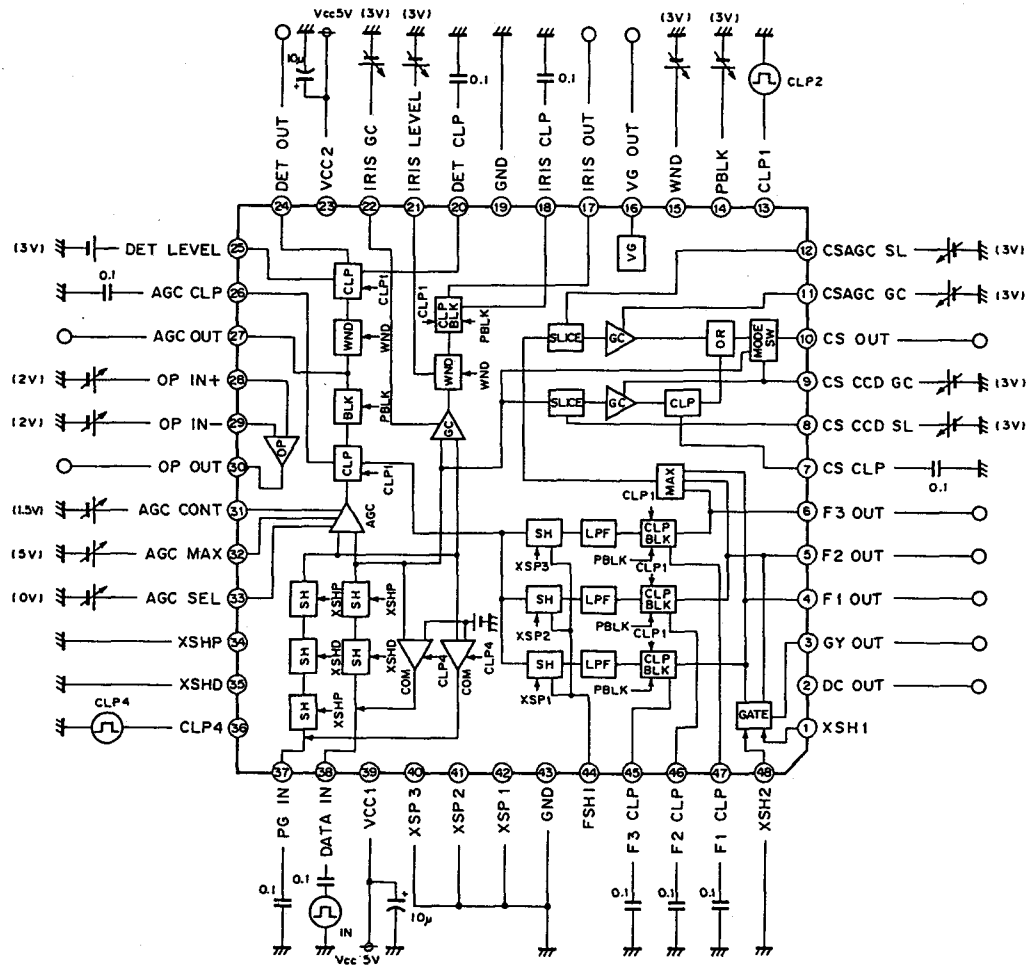
Voltage between the black level at AGC OUT and the high luminance level determined by CS AGC SL pin voltage.



Note 4)

S/H output of DATA IN input can be monitored by turning CS CCD GC (Pin 9) to 0V.

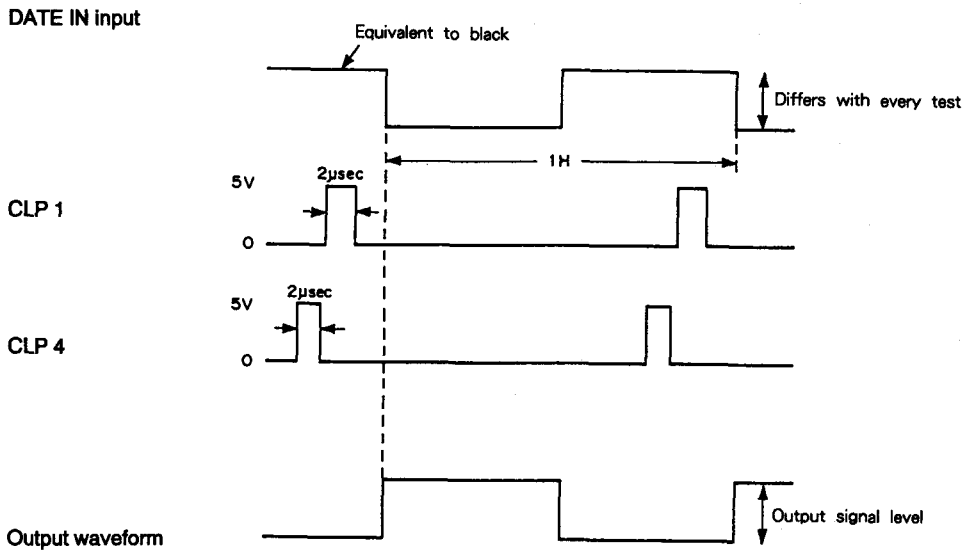
Test Circuit



Note)

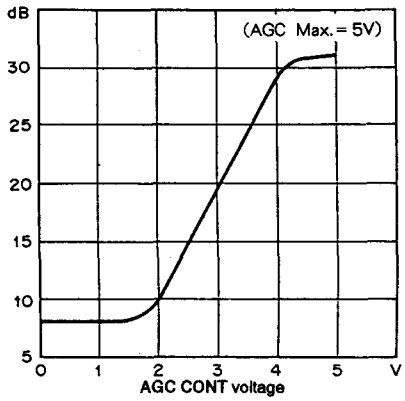
1. Capacitor unit value at μF.
2. Voltage in parentheses are those not specified in the Electrical Characteristics Test Conditions.
3. —○ indicates a test pin. (For both AC and DC)

Timing Diagram for Testing

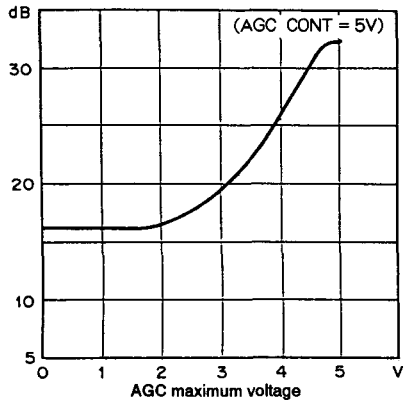


Standard Control Characteristics (Vcc=5V, Ta=25°C)

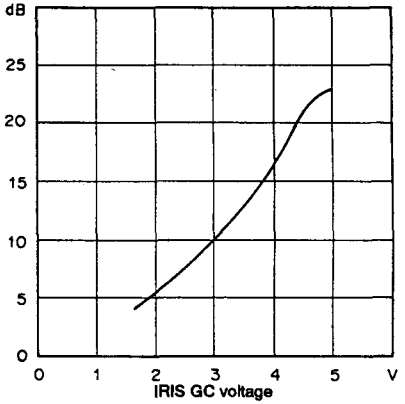
AGC amplifier gain control characteristics



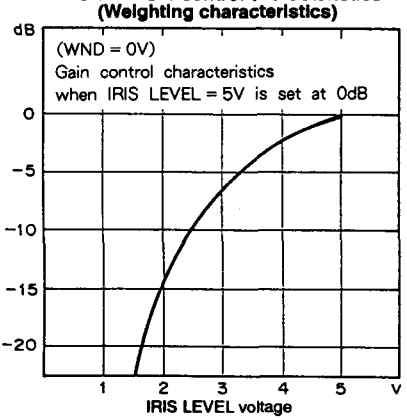
AGC maximum control characteristics



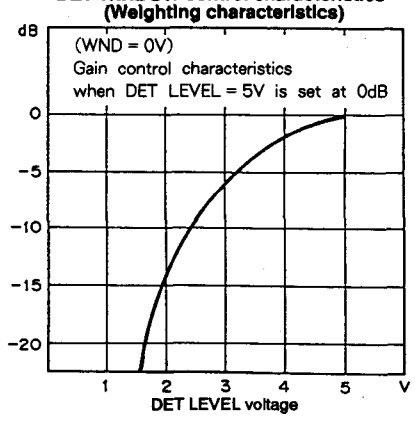
IRIS gain control characteristics



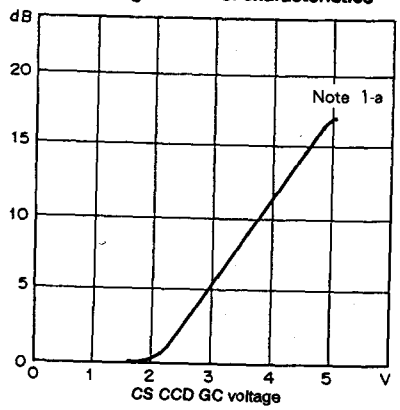
IRIS WINDOW control characteristics (Weighting characteristics)



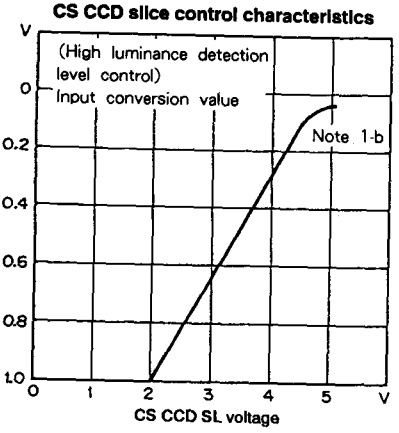
DET WINDOW control characteristics (Weighting characteristics)



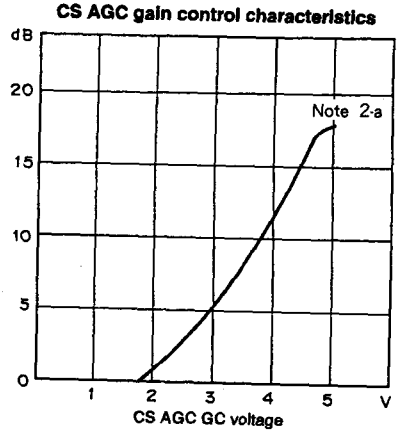
CS CCD gain control characteristics



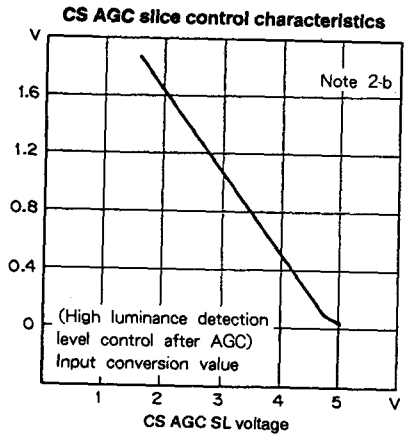
CS CCD slice control characteristics



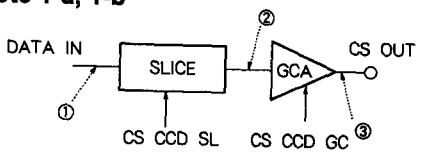
CS AGC gain control characteristics

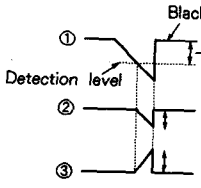


CS AGC slice control characteristics



Note 1-a, 1-b

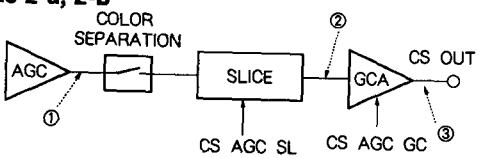


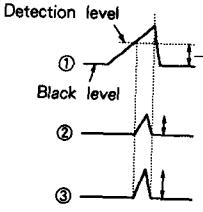


Note 1-b
Voltage indicated at CS CCD slice control characteristics

Note 1-a
Characteristics indicated at CS CCD gain control characteristics = ratio of 3 and 2 (dB)

Note 2-a, 2-b



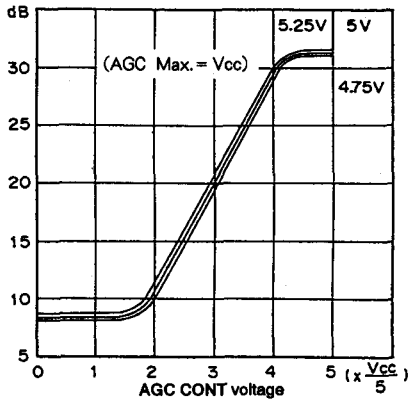


Note 2-b
Voltage indicated at CS AGC slice control characteristics

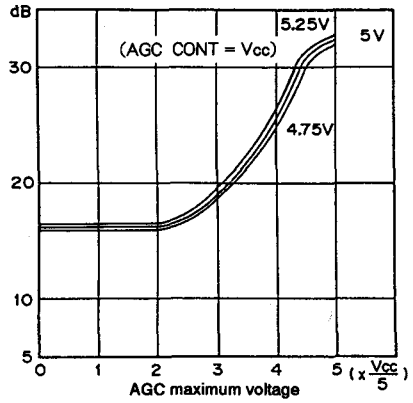
Note 2-a
Characteristics indicated at CS AGC slice control characteristics = ratio of 3 and 2 (dB)

Supply Voltage Characteristics Standard Design Documentation (Ta=25°C)

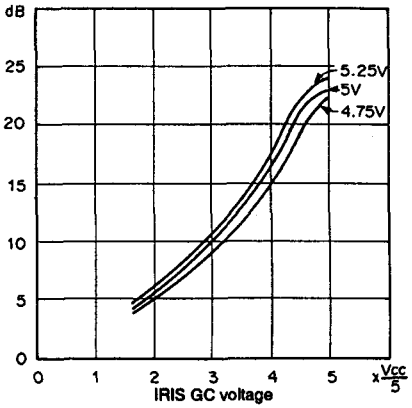
AGC amplifier gain control characteristics



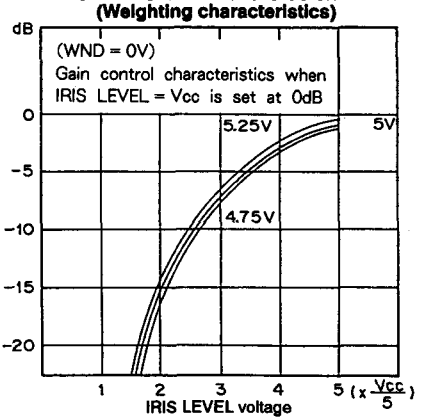
AGC maximum control characteristics



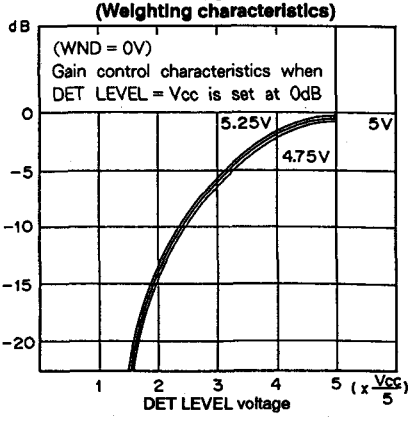
IRIS gain control characteristics



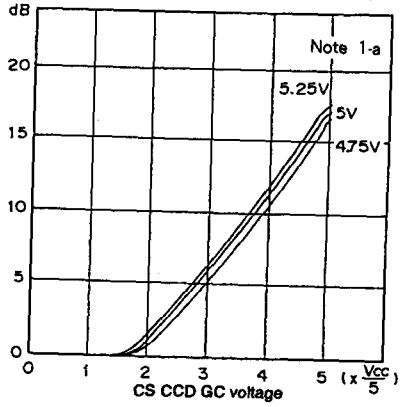
IRIS WINDOW control characteristics (Weighting characteristics)



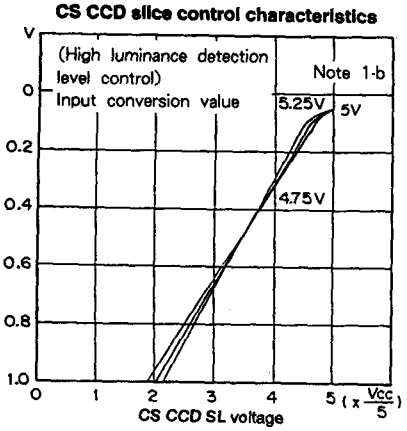
DET WINDOW control (Weighting characteristics)



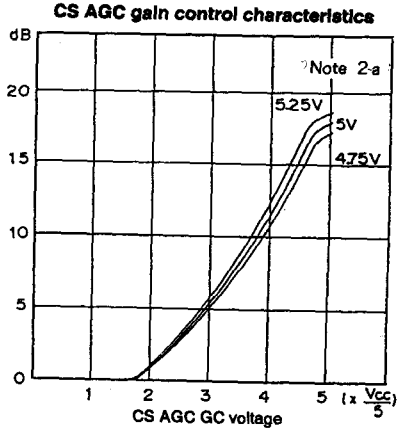
CS CCD gain control characteristics



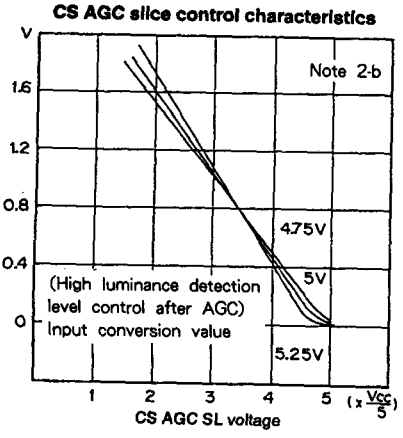
CS CCD slice control characteristics



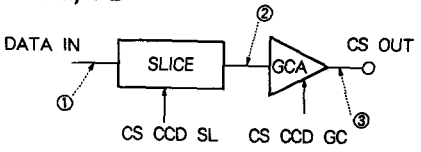
CS AGC gain control characteristics

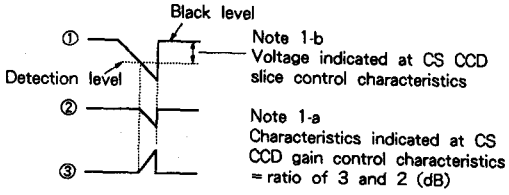


CS AGC slice control characteristics



Note 1-a, 1-b

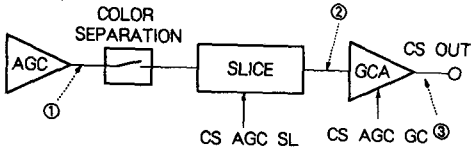


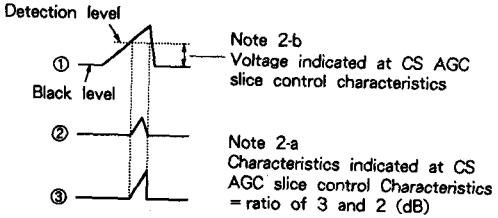


Note 1-b
Voltage indicated at CS CCD slice control characteristics

Note 1-a
Characteristics indicated at CS CCD gain control characteristics = ratio of 3 and 2 (dB)

Note 2-a, 2-b



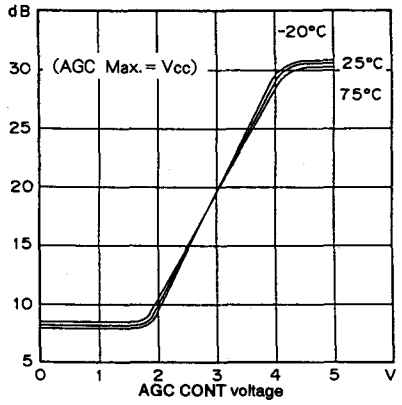


Note 2-b
Voltage indicated at CS AGC slice control characteristics

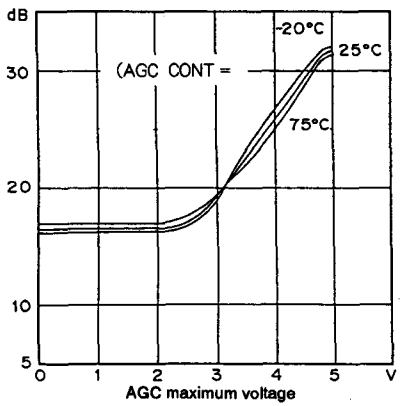
Note 2-a
Characteristics indicated at CS AGC slice control characteristics = ratio of 3 and 2 (dB)

Standard Design Documentation Temperature Characteristics (Vcc=5V)

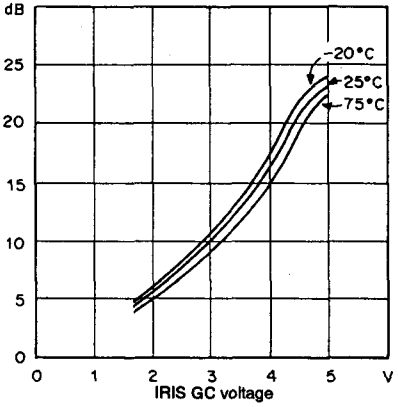
AGC amplifier gain control characteristics



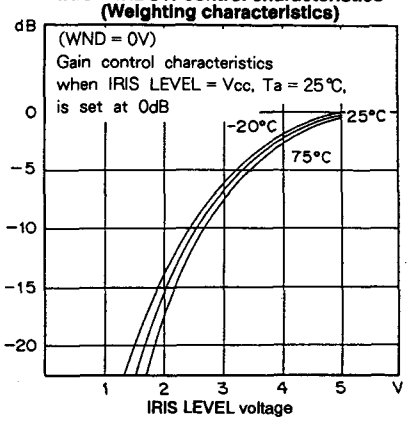
AGC maximum control characteristics



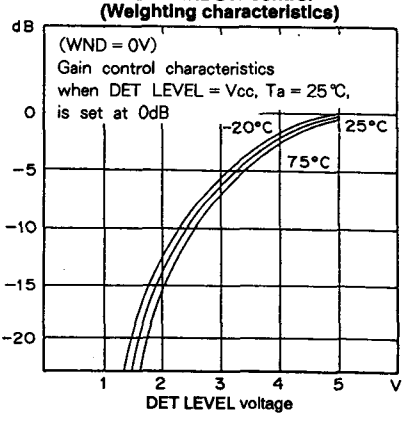
IRIS gain control characteristics



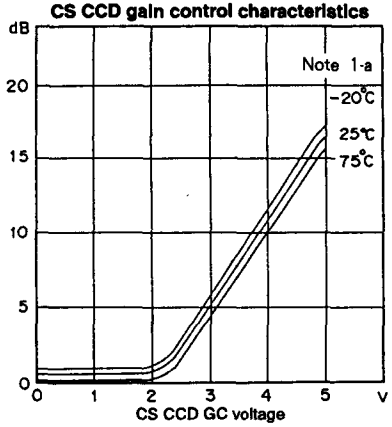
IRIS WINDOW control characteristics (Weighting characteristics)



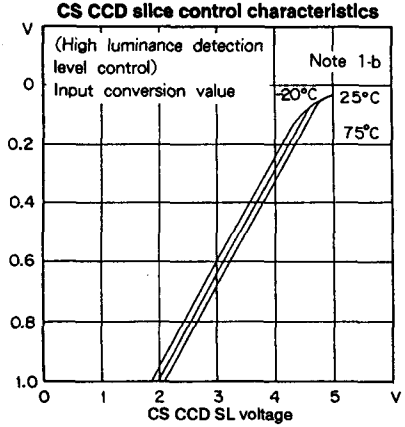
DET WINDOW control (Weighting characteristics)



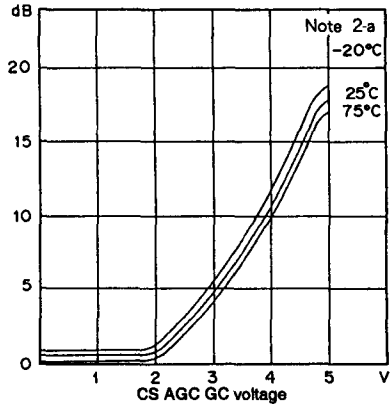
CS CCD gain control characteristics



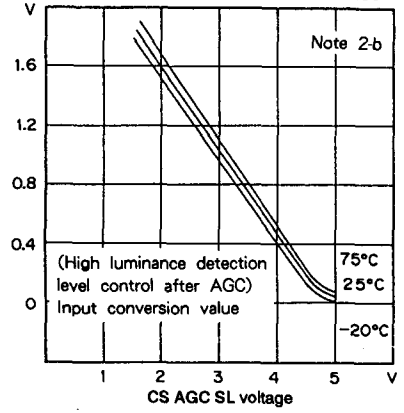
CS CCD slice control characteristics



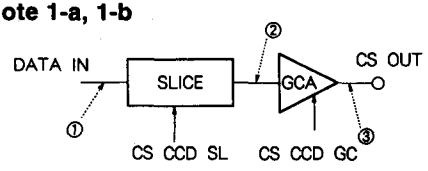
CS AGC gain control characteristics

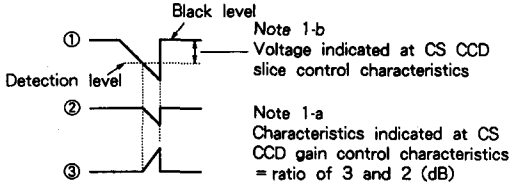


CS AGC slice control characteristics



Note 1-a, 1-b

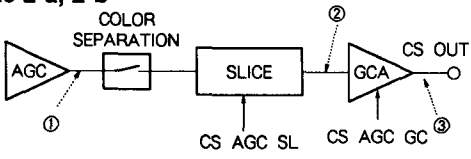


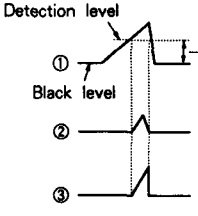


Note 1-b
Voltage indicated at CS CCD slice control characteristics

Note 1-a
Characteristics indicated at CS CCD gain control characteristics = ratio of 3 and 2 (dB)

Note 2-a, 2-b



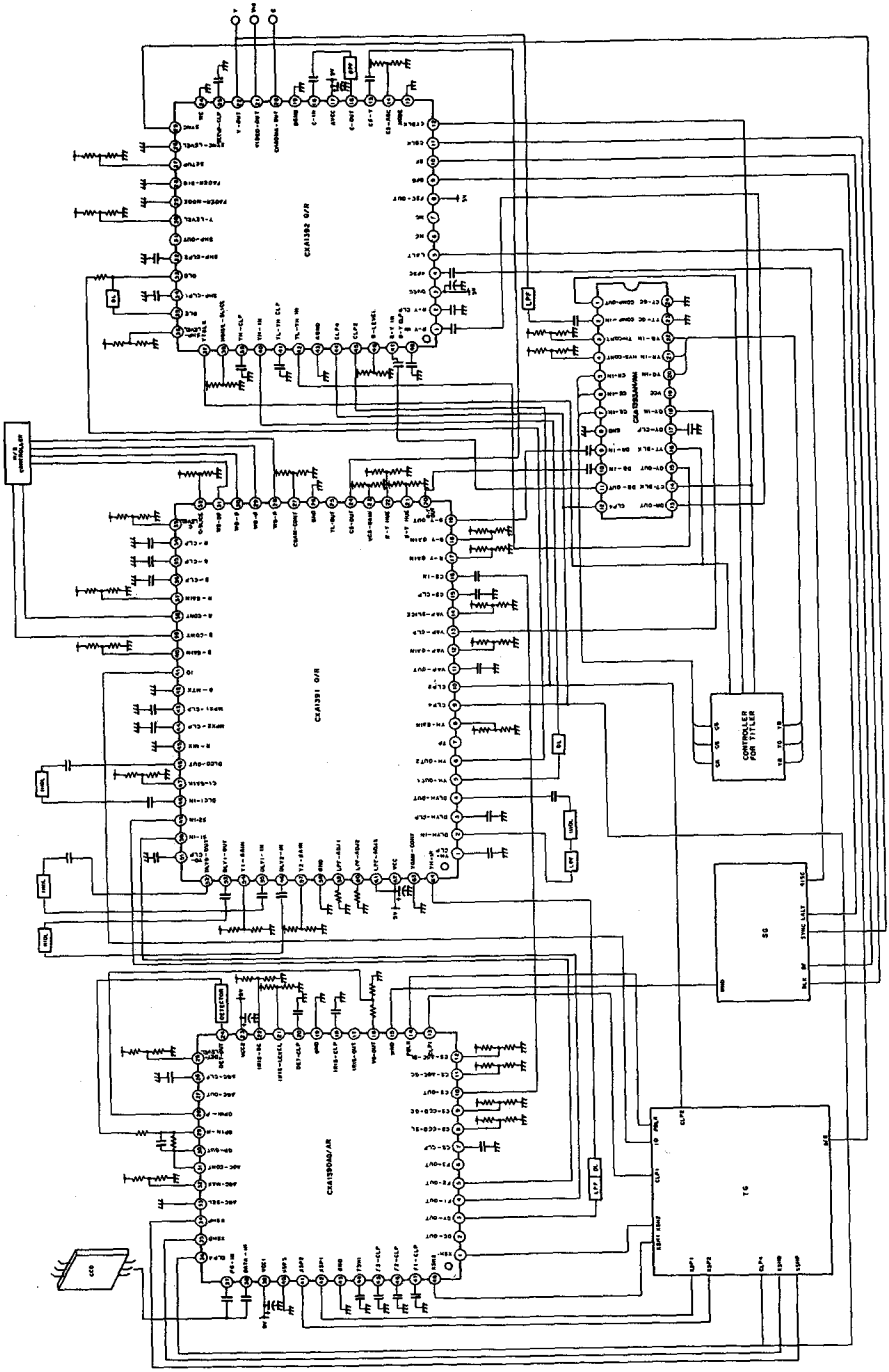


Note 2-b
Voltage indicated at CS AGC slice control characteristics

Note 2-a
Characteristics indicated at CS AGC slice control Characteristics = ratio of 3 and 2 (dB)

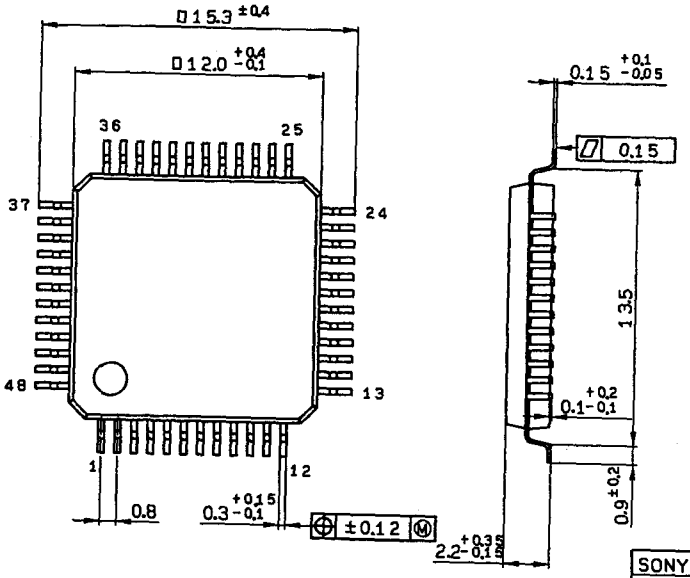
CXA1390 Series System Diagram

(The title insertion function can be removed by doing away with CXA1393AN)



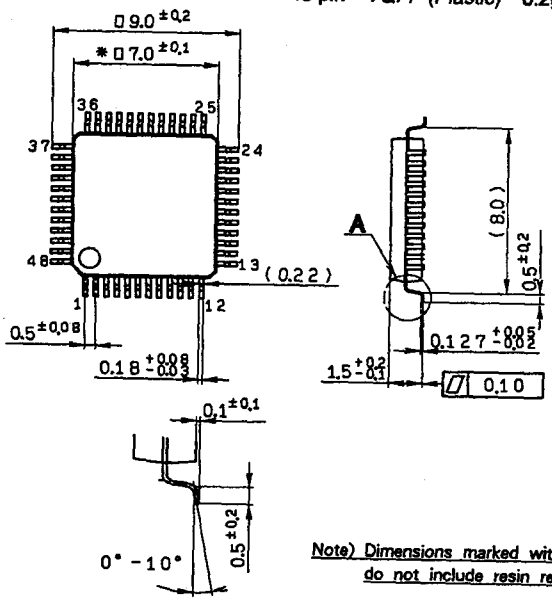
Package Outline Unit : mm

CXA1390AQ 48 pin QFP (Plastic) 0.6g



SONY NAME	QFP-48P-L04
EIAJ NAME	*QFP048-P-1212-B
JEDEC CODE	———

CXA1390AR 48 pin VQFP (Plastic) 0.2g



Note) Dimensions marked with * do not include resin residue.

Detailed diagram of A

SONY NAME	VQFP-48P-L01
EIAJ NAME	*QFP048-P-0707-A
JEDEC CODE	———

SONY

CXA1338Q-Z/R

CCD Camera Matrix

Description

CXA1338Q-Z and CXA1338R are matrix ICs for CCD cameras and are used for the system with complementary color checkers coding imager ICX026AK. They perform the vertical correlation process by using 1HDL and outputs the RGB signal from the magenta, green, yellow, and cyan input signals.

Features

- Excellent color reproduction as a result of the primary color separation system.
- Two modes are provided for the matrix factor ; PRESET and CONTROL.
- The aperture signal in the V direction is output.
- The chroma suppress signal is output.
- The Y_H and Y_L-Y_H signals are output.

Structure

Bipolar silicon monolithic IC

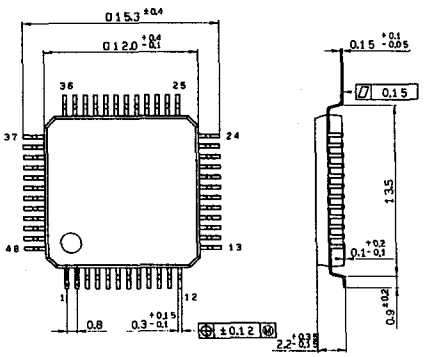
Application

- Complementary color checkers CCD color camera

Package Outline

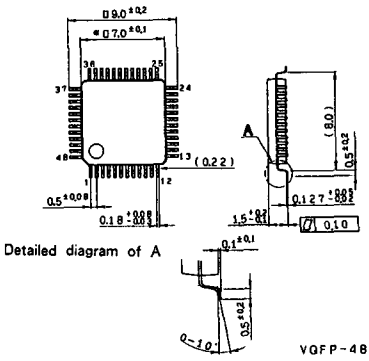
Unit : mm

CXA1338Q-Z 48 pin QFP (Plastic)



QFP-48P-L04

CXA1338R 48 pin VQFP (Plastic)



VQFP-48P-L01

Note) Dimensions marked with * does not include residual resin.

Absolute Maximum Ratings (Ta=25°C)

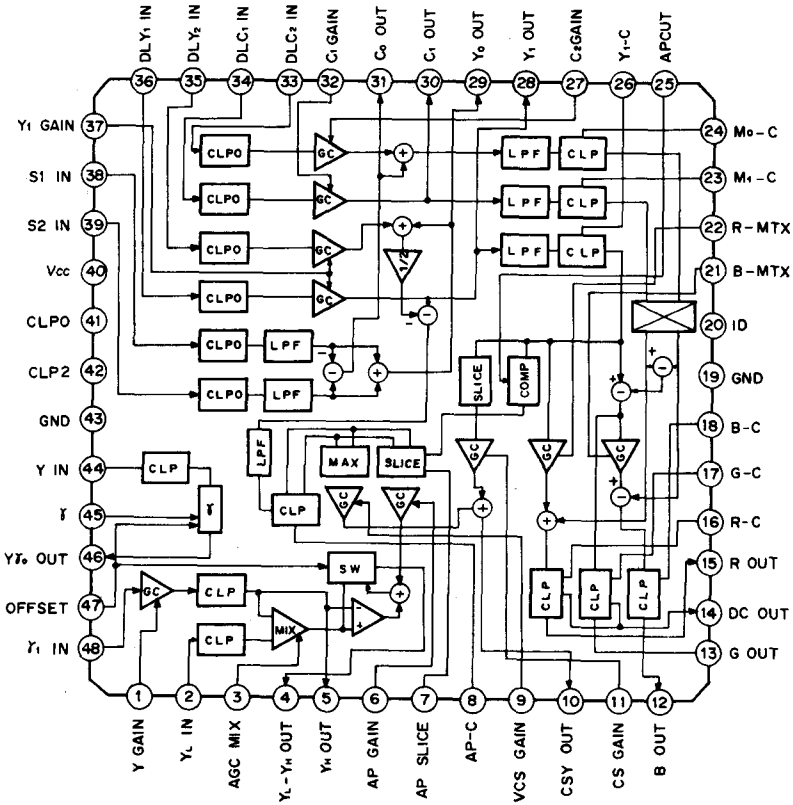
• Supply voltage	Vcc	7	V
• Storage temperature	Tstg	−55 to +150	°C
• Operating temperature	Topr	−20 to +75	°C
• Allowable power dissipation	P_D	600	mW

Recommended Operating Condition

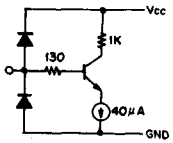
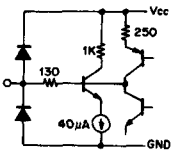
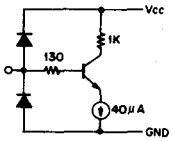
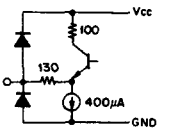
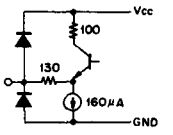
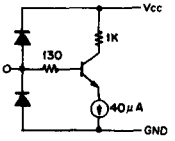
• Supply voltage	Vcc	4.75 to 5.25	V

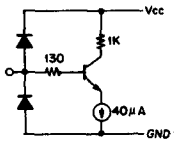
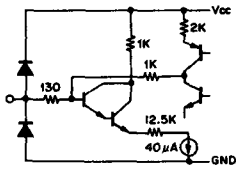
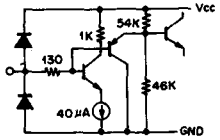
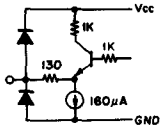
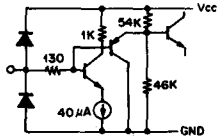
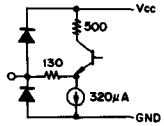
80712-ST

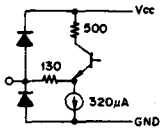
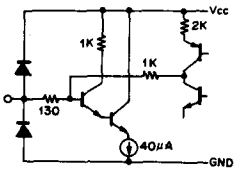
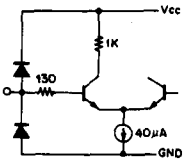
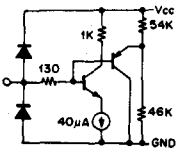
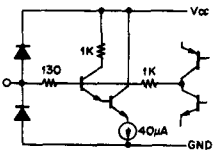
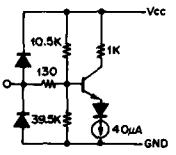
Block Diagram and Pin Configuration

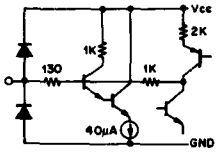
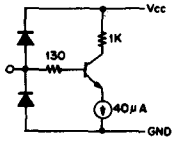
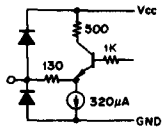
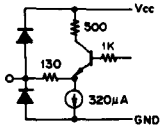
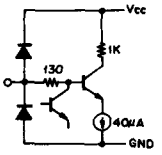
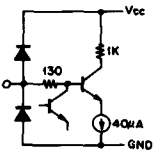
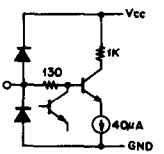


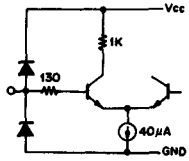
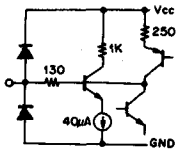
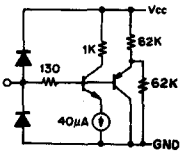
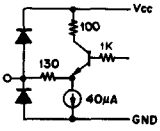
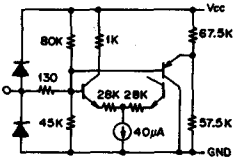
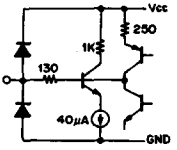
Pin Description

No.	Symbol	Voltage	Equivalent circuit	Description
1	Y GAIN	3.0V		Gain control pin for the signal input to Y $_{Y}$ IIN. 1.8V (Min.) to 5.0V (Max.)
2	Y_L IN	3.4V		Y_L input, which is clamped by the input connected to the capacitor. 250mV (Typ.)
3	AGC MIX	3.0V		Y_M factor (Y_L/Y_H ratio) control. 3.0V (Y_L) to 4.0V (Y_H)
4	Y_L-Y_H OUT	2.9V		Y_L-Y_H signal and V aperture signal output pin. Black level 3V. If the 47 pin OFFSET pin is set to GND in test mode, Y_M signal (that has mixed Y_L and Y_H) is output.
5	Y_H OUT	2.2V		Y_H output. 1000mV (Typ.), 1300mV (Max.) Black level 2.4V
6	AP GAIN	3V		V aperture gain control. 1.8V (Max.) to 5.00V (OFF)

No.	Symbol	Voltage	Equivalent circuit	Description
7	AP SLICE	3V		V aperture slice level control. 1.8V (Min.) to 5.0V (Max.)
8	AP-C	3.7V		Pin that connects the V aperture signal capacitor CLP capacitor.
9	VCS GAIN	3V		Chroma suppress signal level control with V aperture. 1.8V (Min.) to 5.0V (Max.) GND : OFF
10	CSY OUT	2.1V		Chroma suppress signal output.
11	CS GAIN	3V		Chroma suppress signal level control with Y signal. 1.8V (Min.) to 5.0V (Max.) GND : OFF
12 13 15	B OUT G OUT R OUT	1.9V 1.9V 1.9V		R, G, B output pin. Black level 1.9V. If the 21-pin B MTX pin is set to GND in test mode, each pin outputs a signal as shown below. R OUT ··· C_R signal B OUT ··· C_B signal G OUT ··· Y signal The C_R, C_B, and Y signal are provided before the matrix.

No.	Symbol	Voltage	Equivalent circuit	Description
14	DC OUT	1.9V		DC output of 1.9V that is equivalent to R, G, B OUT black level.
16 17 18	R-C G-C B-C	3.2V 3.3V 3.3V		Pin that is connected to the R, G, B OUT clamping capacitor.
19	GND	0V		
20	ID			Inverted pulse is input every 1H. The C1 signal is output to B OUT for HI. The C1 signal is output to R OUT for LOW. V_{TH} = 2.5V
21 22	B MTX R MTX	3V 0V		Matrix factor control for B and R. 1.8V (Max.) to 3.9V (Min.) In test mode : B MTX : C_R/C_B mode with GND R MTX : MTX preset mode with GND
23 24	M_1-C M_0-C	3.0V 3.0V		M_1-C : Connects the 1H line chroma signal clamping capacitor. M_0-C : Connects the 0H/2H line chroma signal clamping capacitor.
25	APCUT	3.95V		Controls the level that suppresses the V aperture signal. Internally biased to 3.95V in preset mode.

No.	Symbol	Voltage	Equivalent circuit	Description
26	Y_1-C	3.0V		Pin that connects the 1H line Y signal clamping capacitor.
27 32 37	C_2- GAIN C_1- GAIN Y_1- GAIN	3V 3V 3V		C1, C2, Y1 signal gain control. 1.8V (Min.) to 5.0V (Max.)
28 29	Y_1 OUT Y_0 OUT	2.6V 2.6V		1H/0H line Y signal output. Inverted output 200mV (Typ.)
30 31	C_1 OUT C_0 OUT	2.6V 2.6V		1H/0H line chroma signal output. Inverted output ± 100mV (Typ.)
33 34	DLC_2 IN DLC_1 IN	2.9V 2.9V		2H/1H line chroma signal input. Positive phase input ± 75mV (Typ.)
35 36	DLY_2 IN DLY_1 IN	2.9V 2.9V		2H/1H line Y signal input. Positive phase input 150mV (Typ.)
38 39	S_1 IN S_2 IN	3.3V 3.3V		S1/S2 signal input. 500mV (Typ.) 1500mV (Max.)

No.	Symbol	Voltage	Equivalent circuit	Description
40	Vcc	5V		Vcc
41 42	CLP0 CLP2	5V 0V 5V 0V		Clamp pulse input V_{TH} = 2.5V
43	GND	0V		GND
44	Y IN	2.7V		Y signal input. 220mV (Typ.) 660mV (Max.)
45	γ	0V		γ curve control. 1.8V to 5.0V GND : Preset
46	$Y_{\gamma 0}$ OUT	3.0V		Y γ signal output. Inverted output 400mV (Typ.) 520mV (Max.)
47	OFFSET	1.8V		γ offset control. 1.8V to 5.0V If the pin is set to OPEN, bias to 1.8V is internally performed. If the pin is set to GND in test mode, the Y_M signal is output from the 4 pin, Y_L-Y_H OUT pin.
48	$Y_{\gamma 1}$ IN	2.9V		1H line Y γ signal output. 150mV (Typ.)

Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current	I_{CC}	Vcc=5V	20	33	45	mA
S_1, S_2 LPF	$F_{S1, S2}$	4.77MHz gain for ㊳ S_1 IN→㉘ Y_0 OUT 300kHz	−28	−20	−11	dB
S_1-Y_0 gain	$G_{S1\text{-}Y0}$	㊳ S_1IN→ ㉘ Y_0 OUT gain	−14.2	−13.0	−11.8	dB
Gain difference between S_1 -Y_0 and S_2-Y_0	ΔG_{Y0}	Gain difference between ㊳ S_1 IN→㉘ Y_0OUT and ㊴ S_2IN→ ㉘ Y_0OUT	−0.7	0	0.7	dB
S_1-C_0 gain	$G_{S1\text{-}S0}$	㊳ S_1 IN→㉛ C_0OUT gain	−3.2	−1.9	−0.8	dB
Gain difference between S_1-C_0 and S_2-C_0	ΔG_{C0}	Gain difference between ㊳ S_1 IN→ ㉛ C_0OUT and ㊴ S_2IN→㉛ C_0OUT	−0.7	0	0.7	dB
Y_1 gain Min.	G_{Y1} Min.	㊱ DLY1 IN→㉘ Y_1 OUT gain ㊲ Y_1 GAIN=1.8V	−	−2.5	−1.3	dB
Y_1 gain Max.	G_{Y1} Max.	㊱ DLY1 IN→㉘ Y_1 OUT gain ㊲ Y_1 GAIN=5V	8.8	12.0	−	dB
C_1 gain Min.	G_{C1} Min.	㉞ DLC1 IN→㉚ C_1 OUT gain ㉜ C_1 GAIN=1.8V	−	−2.5	−1.3	dB
C_1 gain Max.	G_{C1} Max.	㉞ DLC1 IN→㉚ C_1 OUT gain ㉜ C_1 GAIN=5V	8.8	12.0	−	dB
C_2 gain Min.	G_{C2} Min.	㉞ DLC1 IN→⑮ ROUT GAIN that is twice as much as ㉝ DLC2IN →⑮ ROUT, ㉑ BMTX=GND, ⑳ ID=GND, ㉗ C_2GAIN=1.8V for ㉑ BMTX=GND, ID=5V⑳	−	−2.8	−1.3	dB
C_2 gain Max.	G_{C2} Max.	㉞ DLC1 IN→⑮ ROUT Gain that is twice as much as ㉝ DLC2 IN →⑮ ROUT, ㉑ BMTX=GND, ⑳ ID=GND, ㉗ C2GAIN=1.8V for ㉑ BMTX=GND, ⑳ ID=5V	8.8	12.0	−	dB
Y_2 gain Min.	G_{Y2}Min.	Ratio of the output of ㉟ DLY2 IN (200mV) →④ Y_L-Y_HOUT, ㊲ Y_1 GAIN=1.8V to the output of ㊱ DLY1 IN (100mV) → ④ Y_L-Y_HOUT, ㊲ Y1GAIN=1.8V	−1.4	0	1.4	dB
Y_2 gain HI	G_{Y2}Max.	Ratio of the output of ㉟ DLY2 IN (100mV) →④ Y_L-Y_HOUT, ㊲ Y_1 GAIN=1.8V to the output of ㊱ DLY1 IN (50mV) → ④ Y_L-Y_HOUT, ㊲ Y GAIN=3.9V	−1.4	0	1.4	dB
C_0 LPF	F_{C0}	4.77MHz gain for ㉝ DLC2IN→⑮ ROUT, ⑳ ID=GND, 300kHz	−28	−18	−8	dB
C_1 LPF	F_{C1}	4.77MHz gain for ㉞ DLC2IN→⑮ ROUT, ⑳ ID=5V, 300kHz	−28	−18	−8	dB

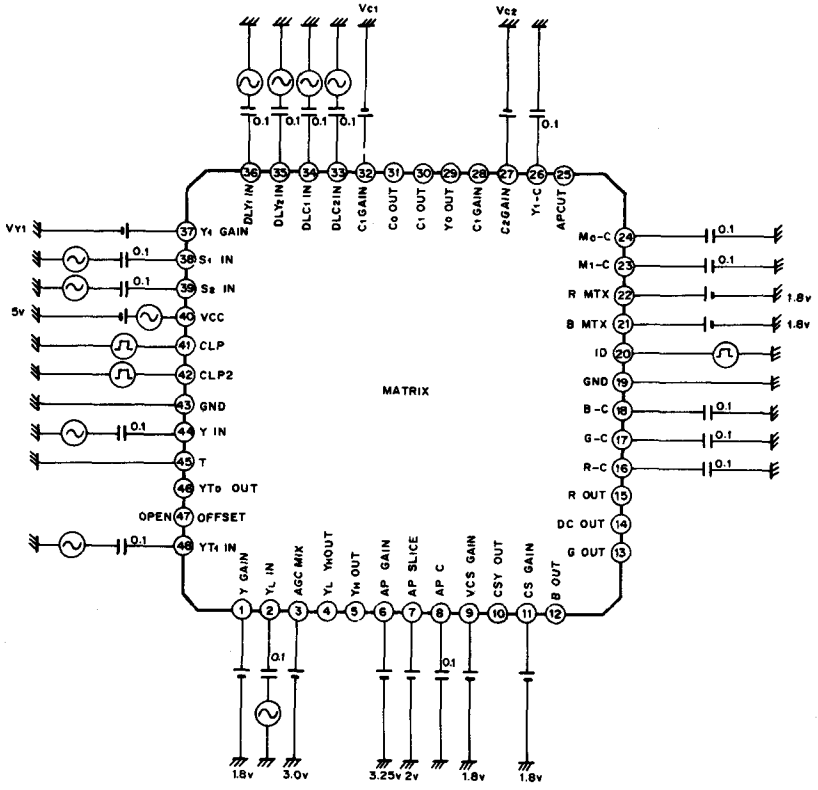
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Y_1 LPF	F_{Y1}	4.77MHz gain for ㊱ DLY1 IN→⑲ GOUT, 300kHz	−28	−18	−8	dB
V apperture LPF	F_{AP}	4.77MHz gain for ㊱ DLY_1 IN→ ④ Y_L-Y_H OUT, 300kHz	−28	−18	−8	dB
DLY_1 → Y_L-Y_H gain	G_{DLY1}	㊱ DLY1 IN (100mV) →④ Y_L-Y_H OUT gain ⑥ APGAIN=3.25V	6	8.3	11	dB
V aperture level Max.	G_{AP}Max.	㊱ DLY1 IN (30mV) →④ Y_L-Y_H OUT Output level ratio for ⑥ APGAIN=3.25V to 1.5V	8	11	−	dB
V aperture slice Mid.	V_{APS} Mid.	㊱ DLY1 IN (100mV) →④ Y_L-Y_H OUT Output level difference between ⑦ APSLICE=2V and 3V	85	120	155	mV
V aperture cutting input level	V_{APCUT}	㊱ DLY1 IN input level when the ④ Y_L-Y_H OUT output is cut ⑥ APGAIN=1.5V	225	260	295	mV
Chroma suppress Y output level Max.	V_{CSY} Max.	㊱ DLY1 IN (350mV) →⑩ CSYOUT ⑨ VCSGAIN=GND, ⑪ CSGAIN=1.8V	400	760	−	mV
Chroma suppress Y gain Min.	G_{CSY} Min.	㊱ DLY1 IN (350mV) →⑩ CSYOUT ⑨ VCSGAIN=GND Output level ratio for ⑪ CSGAIN=5V to 1.8V	−14.2	−12.0	−10.8	dB
Chroma suppress VAP level Max.	V_{CSVAP} Max.	㊱ DLY1 IN (50mV) →⑩ CSYOUT ⑪ CSGAIN=GND, ④ VCSGAIN=5V	740	920	−	mV
Chroma suppress VAP gain Min.	G_{CSVAPM} Min.	㊱ DLY1 IN (50mV) →⑩ CSYOUT ⑪ CSGAIN=GND Output level ratio for ⑨ VCSGAIN=5V to 1.8V	−14.2	−12.0	−9.3	dB
C_R gain	G_{CR}	㉞ DLC_1 IN→⑮ ROUT gain ㉒ RMTX=GND	3.6	5.3	7.0	dB
RMTX Y factor presetting	K_{RY}	㉞ DLC_1IN (100mV) →⑮ ROUT, ⑳ ID=5V ㉒ RMTX=GND output level set to V_1 ㊱ DLY IN (220mV) →⑮ ROUT, ⑳ ID=5V ㉑ RMTX=GND output level set to V_2 (V_2/V_1) ×1/8 is calculated.	0.094	0.12	0.131	V/V
C_B gain	G_{CB}	㉞ DLC_1IN→⑫ BOUT gain ⑳ ID=GND, ㉒ RMTX=GND	3.6	5.3	7.0	dB
BMTX Y factor presetting	K_{BY}	㉞ DLC_1 IN (100mV) →⑫ BOUT, ⑳ ID=GND ㉒ RMTX=GND output level set to V_1 ㊱ DLY_1 IN (220mV) →⑫ BOUT, ⑳ ID=GND ㉒ RMTX=GND output level set to V_2 (V_2/V_1) ×1/8 is calculated.	0.173	0.20	0.222	V/V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
BMTX C_R factor	K_{BCR}	㉞ DLC1IN (100mV) →⑫ BOUT, ⑳ ID=GND ㉒ RMTX=GND output level set to V_1 ㉞ DLC1IN (100mV) →⑫ BOUT, ⑳ ID=5V ㉒ RMTX=GND output level set to V_2 V_2/V_1	0.173	0.20	0.222	V/V
Y_1 gain	G_{Y1}	㊱ DLY1IN→⑬ GOUT gain ⑳ ID=5V, ㉒ RMTX=GND	6.6	8.3	10.0	dB
GMTX C_R factor	K_{GCR}	㊱ DLY1IN (220mV) →⑬ GOUT, ⑳ ID=5V ㉒ RMTX=GND output level set to V_1 ㉞ DLC1IN (100mV) →⑬ GOUT, ⑳ ID=5V ㉒ RMTX=GND output level set to V_2 $V_2/V_1 \times 8$	0.78	1.0	1.22	V/V
GMTX C_B factor	K_{GCB}	㊱ DLY1IN (220mV) →⑬ GOUT, ⑳ ID=5V ㉒ RMTX=GND output level set to V_1 ㉞ DLC1IN (100mV) →⑬ GOUT, ⑳ ID=GND ㉒ RMTX=GND output level set to V_2 $V_2/V_1 \times 8$	0.78	1.0	1.22	V/V
RMTX Y factor HI	K_{RYMI}	㉞ DLC1IN (100mV) →⑮ ROUT, ⑳ ID=5V ㉒ RMTX=GND output level set to V_1 ㊱ DLY1IN (220mV) ⑮ ROUT, ⑳ ID=5V ㉒ RMTX=1.8V output level set to V_2 $(V_2/V_1) \times 1/8$ is calculated.	0.192	0.225	0.253	V/V
BMTX Y factor LOW	K_{RYLO}	㉞ DLC1IN (100mV) →⑮ ROUT, ⑳ ID=5V ㉒ RMTX=GND output level set to V_1 ㊱ DLY1IN (220mV) →⑮ ROUT, ⑳ ID=5V ㉒ RMTX=3.9V output level set to V_2 $(V_2/V_1) \times 1/8$ is calculated.	0.042	0.056	0.070	V/V
BMTX Y factor HI	K_{BYMI}	㉞ DLC1IN (100mV) →⑫ BOUT, ⑳ ID=GMD ㉒ RMTX=GND output level set to V_1 ㊱ DLY1IN (220mV) →⑫ BOUT, ⑳ ID=GND ㉑ BMTX=1.8V output level set to V_2 $(V_2/V_1) \times 1/8$ is calculated.	0.337	0.380	0.413	V/V
RMTX Y factor LOW	K_{BYLO}	㉞ DLC1IN (100mV) →⑫ BOUT, ⑳ ID=GND ㉒ RMTX=GND output level set to V_1 ㊱ DLY1IN (220mV) →⑫ BOUT ⑳ ID=GND ㉑ BMTX=3.9V output level set to V_2 $(V_2/V_1) \times 1/8$ is calculated.	0.068	0.09	0.117	V/V
DC OUT DC	V_{CC}	⑭ DCOUT pin voltage	1.73	1.85	1.97	V
R, G, B OUT offset	V_{RGBO}	Potential difference between ⑮ ROUT/ ⑬ GOUT, ⑫ BOUT and ⑭ DCOUT	−10	0	10	mV
γ preset standard level	$V_{Y\,PRE}$	㊹ YIN (220mV) →㊻ Y γ OUT	365	410	455	mV

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Y preset curve	$G_{Y\,PPE}$	Ratio of ㊶ YIN (55mV) →㊻ Y Y OUT output level to ㊶ YIN (220mV) → ㊻ Y Y OUT output level	−8.2	−7.0	−5.8	dB
Y_HOUT DC	$V_{Y\,HOUT}$	⑤ Y_HOUT pin voltage	2.0	2.3	2.6	V
Y_H gain Min. (Y_HOUT)	G_{YH}Min1	㊽ Y Y1IN→⑤ Y_HOUT gain ① YGAIN=1.8V ③ AGCMIX=4V ㊼ OFFSET=GND	−	10	12.2	dB
Y_H gain Max. (Y_HOUT)	G_{YH}Max1	㊽ Y Y1IN→⑤ Y_HOUT gain ① YGAIN=5V ③ AGCMIX=4V ㊼ OFFSET=GND	20.8	23.0	−	dB
Y_L-Y_H OUT DC	V_{YL}OUT	Y_L-Y_H pin voltage	2.6	2.9	3.2	V
Y_H gain Min. (Y_L-Y_H OUT)	G_{YH}Min2	㊽ Y Y1IN→④ Y_L-Y_H OUT gain ① YGAIN=1.8V ③ AGCMIX=4V ㊼ OFFSET=GND	−	2.1	4.2	dB
Y_H gain Max. (Y_L-Y_H OUT)	G_{YH}Max2	㊽ Y Y1IN→④ Y_L-Y_H OUT gain ① YGAIN=5V ③ AGCMIX=4V ㊼ OFFSET=GND	12.8	15.0	−	dB
Y_L gain	G_{YL}	② Y_L IN→④ Y_L-Y_H OUT gain ③ AGCMIX=3V	4.3	6.0	7.7	dB

Electrical Characteristics Test Circuit

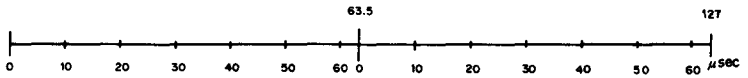
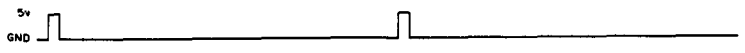
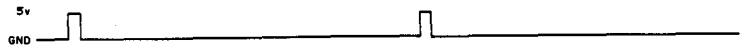
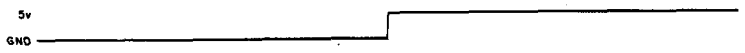
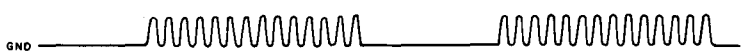
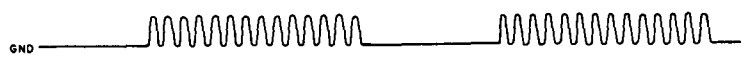
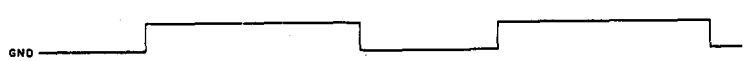
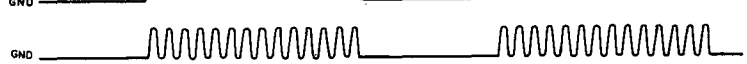
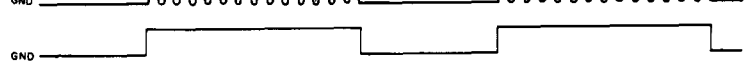
Standard setting conditions



Note)

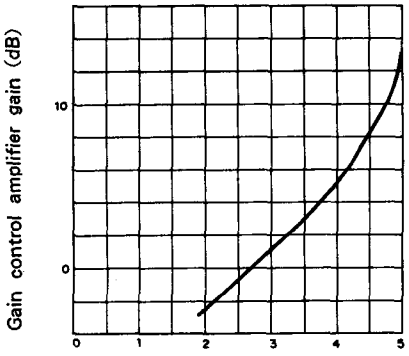
1. Conditions only that are different from standard setting conditions are described.
2. Adjust V_{C1}, V_{C2}, and V_{Y1} so that the signal levels will be equivalent between DLC_1IN and C_1OUT, DLC_2IN and between DLY_1IN and Y_1OUT.
3. Signal sources other than ID, CLP0, and CLP2 are not input in standard setting but set to GND.
4. If measurement conditions specify ID=5V and ID=GND, measure at the ID=5V timing and ID=GND timing.

Input Signal Timing Chart

Pin	Input signal
	
41 CLPO	
42 CLP2	
20 ID	
38 S_1 IN	
39 S_2IN	
36 DLY_1 IN	
35 DLY_2 IN	
34 DLC_1 IN	
33 DLC_2 IN	
44 YIN	
48 Y_{Y1} IN	

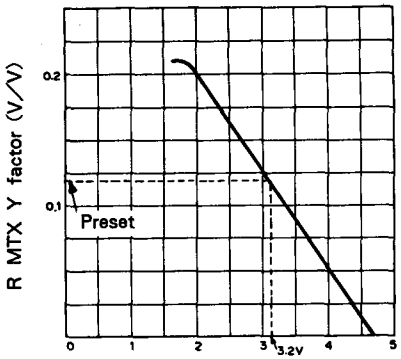
Note) 1. The signal level and frequency are listed in another table.
2. The sine wave intermittent signal is used for measurement of LPF characteristics

Delay line gain control amplifier characteristics



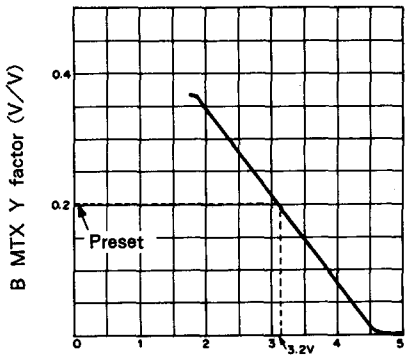
37, 32, 27 pins Y1, C1, C2GAIN pins (Y)

R MTX control characteristics (Y factor)



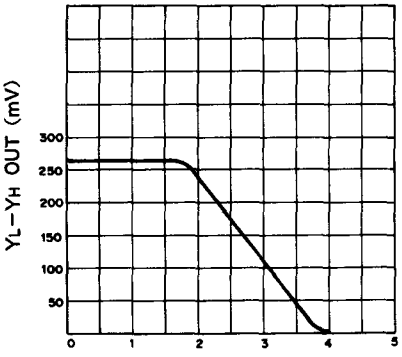
22 pin RMTX (V)

B MTX control characteristics (Y factor)



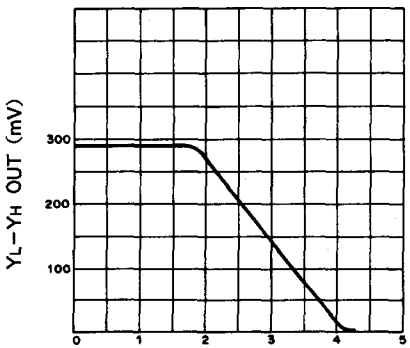
21 pin BMTX (V)

AP GAIN control characteristics



6 pin AP GAIN (V)

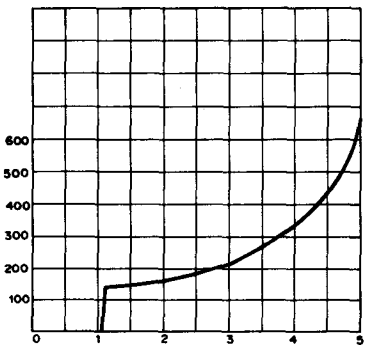
AP SLICE control characteristics



7 pin AP SLICE (V)

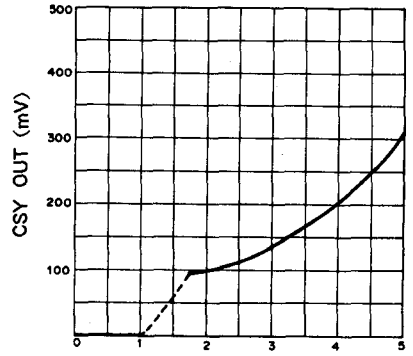
(6 pin AP GAIN=3.25V
Input pin 36 DLY1IN 100mV)

CSY GAIN control characteristics



11 pin CS GAIN (V)
(Input pin 36 DLY1IN=350mV)

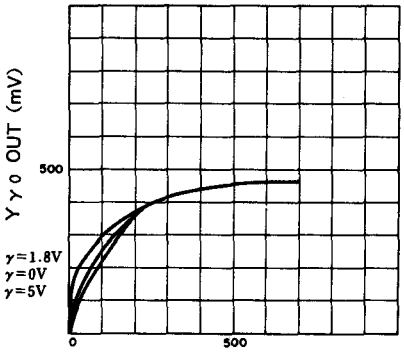
CSY VAP control characteristics



9 pin VCS GAIN pin (V)

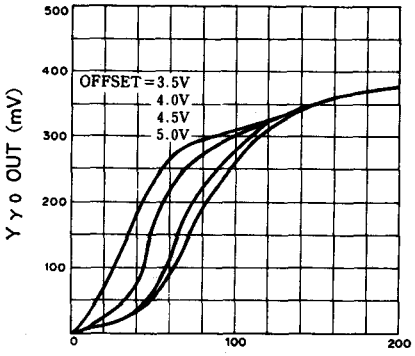
(Input pin 36 DLY1IN=50mV)

γ control characteristics



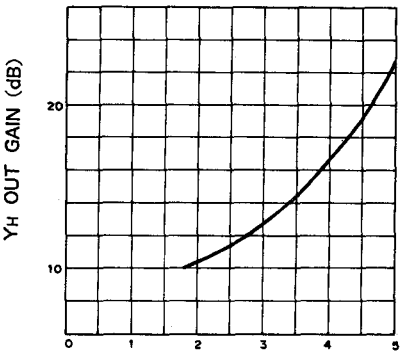
44 pin YIN input level (mV)

γ OFFSET control characteristics (γ = 1.8V)



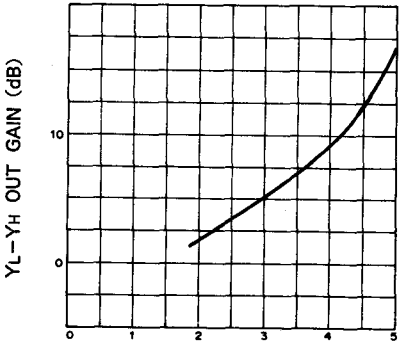
44 pin YIN input level (mV)

YH GAIN control characteristics



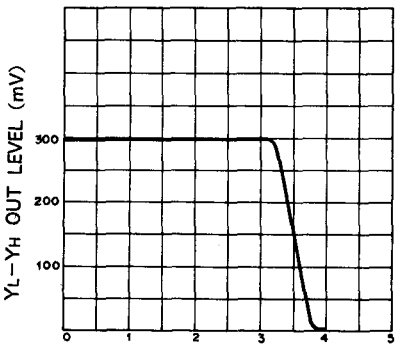
1 pin Y GAIN pin (V)

YM GAIN control characteristics



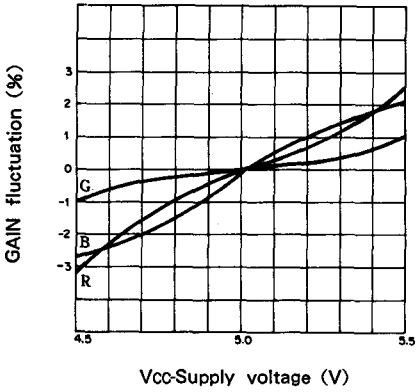
1 pin Y GAIN pin (V)

YL MIX control characteristics

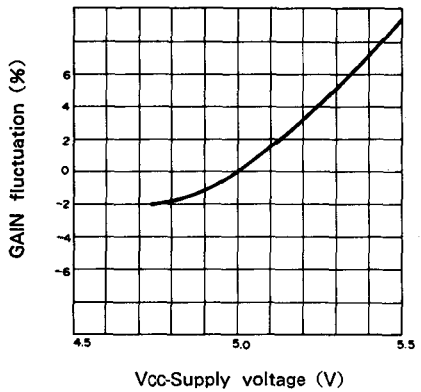


3 pin AGC MIX (V)

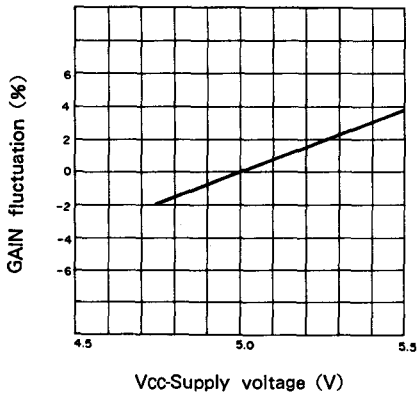
S1, S2, Y-R, G, B GAIN Vcc characteristics



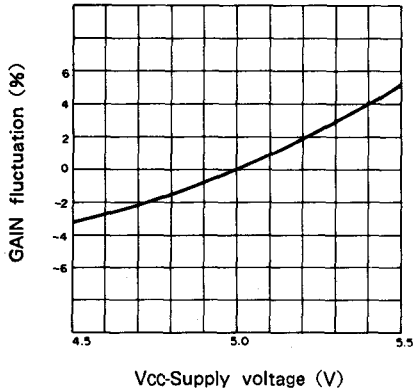
YIN – YH GAIN Vcc characteristics



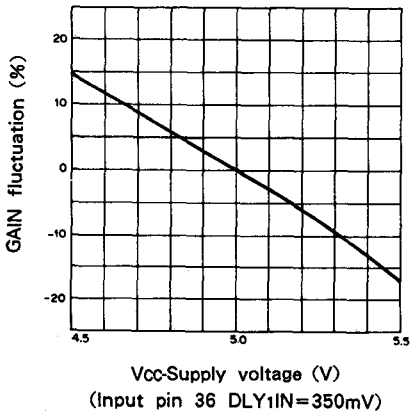
YIN – YL-YH GAIN Vcc characteristics



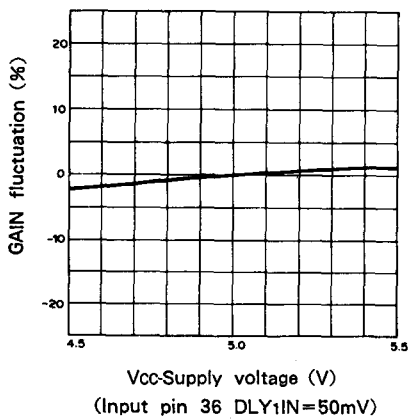
YIN – YL GAIN Vcc characteristics



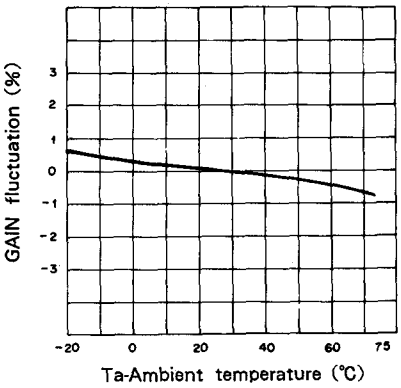
CSY GAIN Vcc characteristics



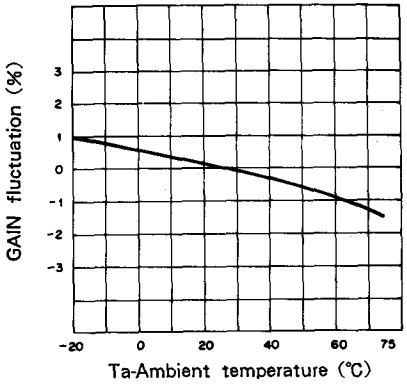
VCS GAIN Vcc characteristics



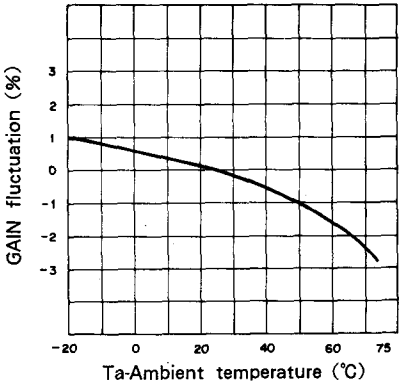
S_1, S_2 IN → C_0, Y_0 OUT Gain temperature characteristics



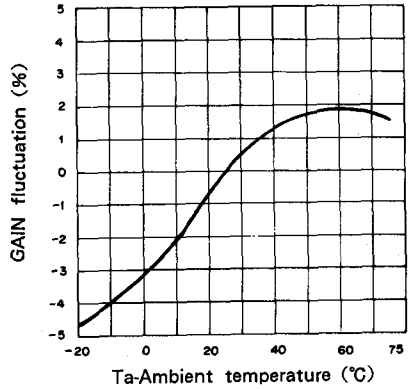
DLY_1, DLC_1 IN → Y_1, C_1 OUT gain temperature characteristics (0dB)



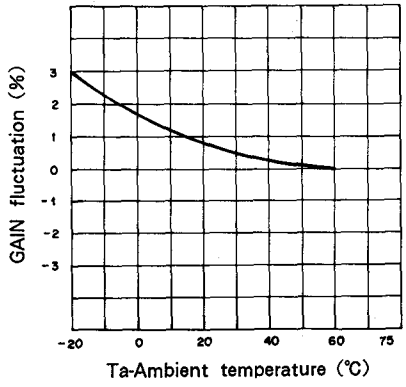
DLC_1 IN → R, B OUT gain temperature characteristics



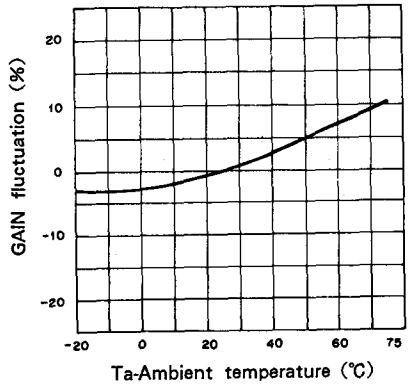
Y IN (220mV) → Y_Y OUT gain temperature characteristics



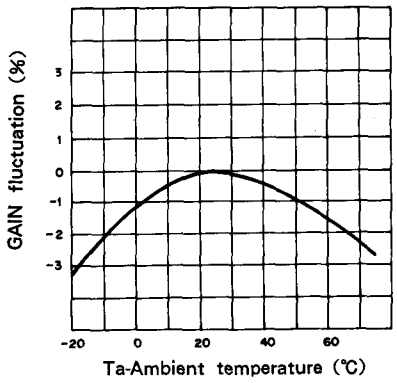
Y_{Y1} IN → Y_H OUT gain temperature characteristics



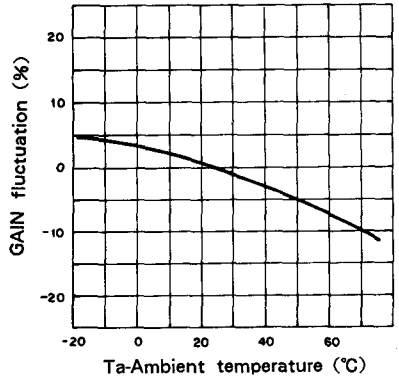
DLY_1 IN → Y_L - Y_H OUT aperture gain temperature characteristics



DLY1 IN (350mV) → YL - YH OUT CSY temperature characteristics.



DLY1 IN (50mV) → YL - YH OUT CSY VAP temperature characteristics.



Operation

CXA1151 is an IC that outputs RGB, YL - YH, YH, and CSY from the signal that sampled and held the complementary color checker coding imager.

1. S1 and S2 input → RGB OUT

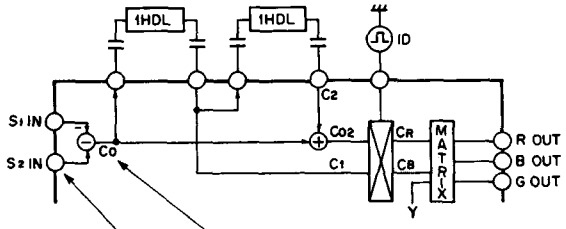


Table-1 Imager coding

Mg	G	Mg	G	0H
Ye	Cy	Ye	Cy	
G	Mg	G	Mg	1H
Ye	Cy	Ye	Cy	
Mg	G	Mg	G	2H
Ye	Cy	Ye	Cy	
S_2	S_1	S_2	S_1	

Table-2 Chroma signal

	0H(C_0)	1H(C_1)	2H(C_2)
C	2R−G	−(2B−G)	2R−G

Table-3 S1 and S2 signals

	0H	1H	2H
S_1	G+Cy	Mg+Cy	G+Cy
S_2	Mg+Ye	G+Ye	Mg+Ye

1) Imager
The coding imager shown in Table-1 is used.

2) S1 and S2 inputs
The signals that sampled and held the imager output are input. By using the imager shown in Table-1, field reading is performed to obtain signals shown in Table-3. G+Cy and G+Ye, or Mg+Ye and Mg+Cy are alternately input to S1 and S2 every hour.

3) Chroma signal
The chroma signal (C) is acquired from S_2 - S_1. As shown in Table-2, a signal that alternates 2R-G and 2B-G is obtained.

4) C_{02} and C_1 signals
To make the RGB signal in the matrix circuit, 2R-G and 2B-G are required at the same time. By using 1HDL, signal C_1 that 1 hour behind and signal C_2 that is 2 hours behind are created. By averaging C_0 and C_2 with the same period as 2B-G of C_1, 2R-G is created.

5) Multiplexing
2R-G and 2B-G are alternately sent every hour to C_1 and C_{02}, so 2R-G (C_R) and 2B-G (C_B) are separated by the ID pulse that inverts "L" to "H", or vice versa every 1 hour.

6) Matrix
RGB is made from C_R, C_B, and Y. The theoretical formulae shown below are applied.
$R = C_R + 0.12Y$
$B = -C_B + 0.20\ (Y - C_R)$
$G = Y - C_R + C_B$
Coefficients, 0.12 and 0.20, are adjustable. (RMTX and BMTX Pins)

7) RGB output
The RGB output is a clamped output. The clamped DC is output to the DC pin. From the R OUT, B OUT, and G OUT pins, the C_R, C_B, and Y signals to be fed to the matrix can be output.

2. Y IN, Y_L IN → Y_L - Y_H OUT
As Y_L that is output from Y_L - Y_H OUT, ② Y_L signal and ㊹ Y IN signal can be linearly switched with ③ AGC MIX pin of the MIX amplifier.

1) Y IN signal
$Y = Mg + G + Ye + Cy$ ((f_3) out of CXA1337), as the AGC output, is input.

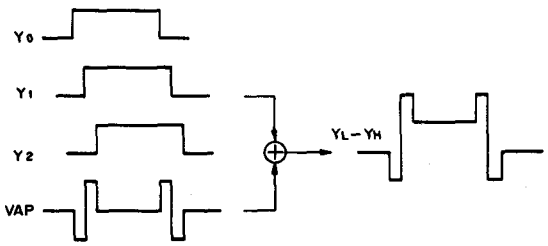
2) γ
The γ curve is adjustable, and presetting is available.

3) OFFSET
It is used in the negative mode. If GND is set, the output of the MIX amplifier comes out of Y_L - Y_H OUT. (For adjustment)

4) Y_L - Y_H OUT
By controlling the AGC MIX Pin, α (Y_L IN - Y IN) ($0 \leqq \alpha \leqq 1$) is output. The aperture signal is added and output.

3. V aperture signal
The V aperture signal is synthesized from $\frac{Y_0 + Y_2}{2} - Y_1$

The signal is made at a ratio of 1 : 1 between plus and minus.



After aperture signal VAP is synthesized, the signal whose level around noise is sliced and controlled by the aperture slicing circuit is added to the Y_L - Y_H signal.

The aperture signal is not output when the Y signal exceeds a reference level.

That reference level has been preset but it can be adjusted with ㉕ AP CUT Pin.

If ㉕ AP CUT is set to GND, the aperture signal is not output at all.

4. Chroma suppressing Y signal

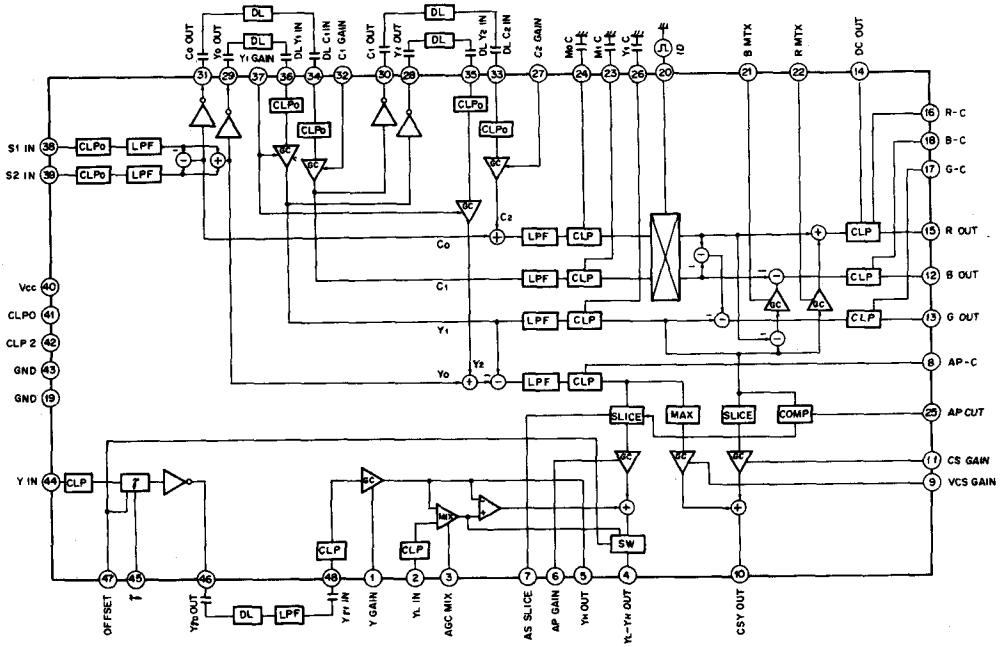
Depending on the Y signal level, a signal that suppresses the chroma signal is output.

The chroma suppressing Y (CSY) signal is made by mixing the following two signals :

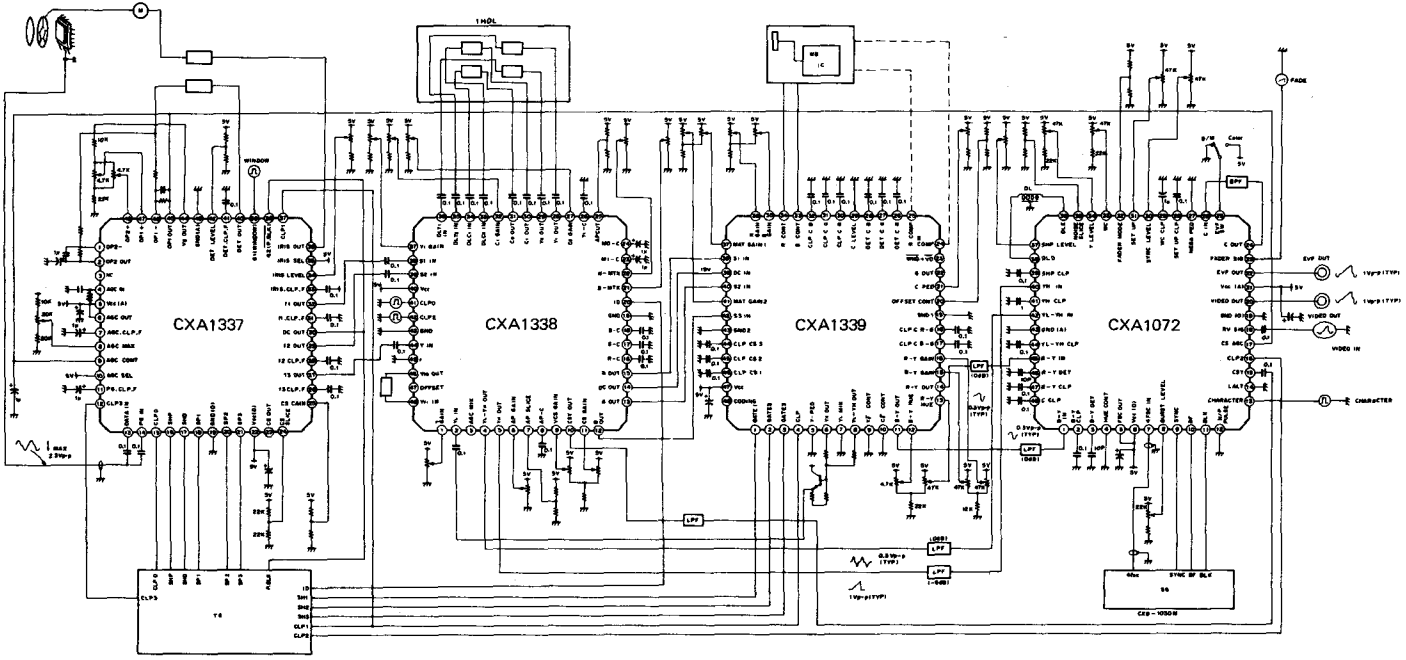
1) The amount of the Y signal exceeding a reference level (1.2 times of the reference signal) is output.

   The sliced amount is fixed. After slicing, the signal is gain-controlled and output.

2) The absolute value of the aperture signal is output as the CSY signal.



Application Circuit



- It is recommended to set the resistance with no value indicated to 50kΩ and below between Vcc and GND.
- Unspecified capacity unit is μF

SONY

CXA1391Q/R

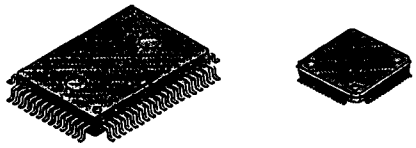
Processing IC for Complementary Color Mosaic CCD Camera

Description

The CXA1391Q/R is a bipolar IC developed for signal processing in complementary color mosaic CCD cameras.

CXA1391Q
64 pin QFP (Plastic)

CXA1391R
64 pin VQFP (Plastic)



Features

- Low power consumption (170mW)
- Number of delay lines used for signal processing can be selected according to the system requirements
- The LPF peripheral to 1H delay line is built in

Absolute Maximum Ratings

• Supply voltage	Vcc	7	V
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	690	mV
	(VQFP: Ta=25°C, without P.C.B)		

Recommended Operating Conditions

• Supply voltage	Vcc	4.75 to 5.25	V
• Ambient temperature	Topr	−20 to +75	°C

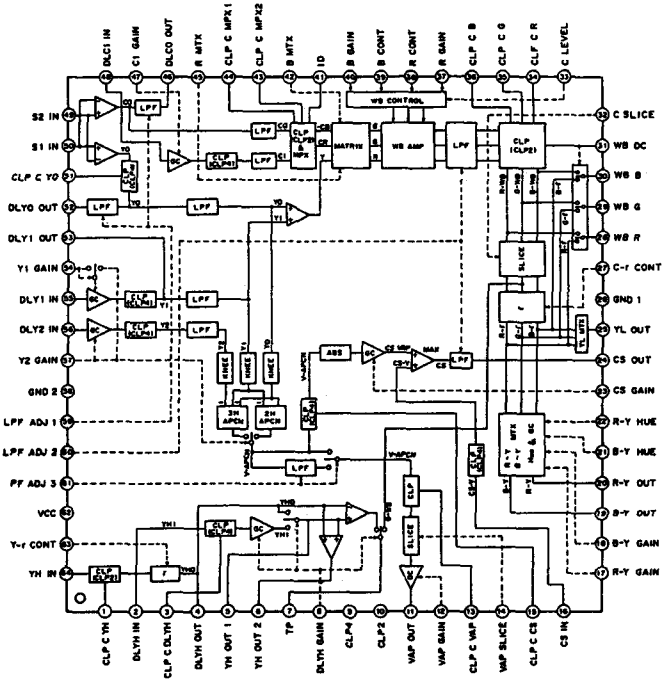
Structure

Bipolar silicon monolithic IC

Applications

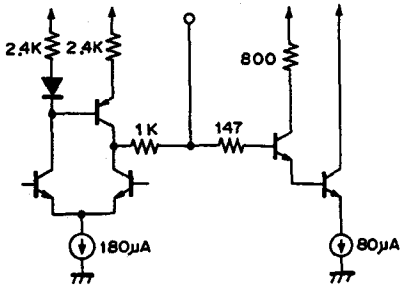
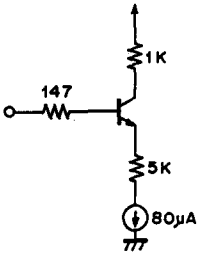
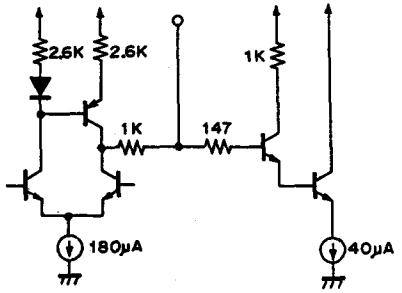
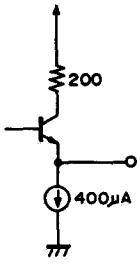
Complementary color mosaic CCD cameras

Block Diagram and Pin Configuration (Top View)

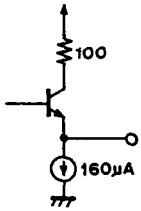
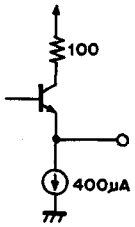
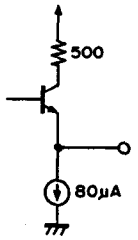
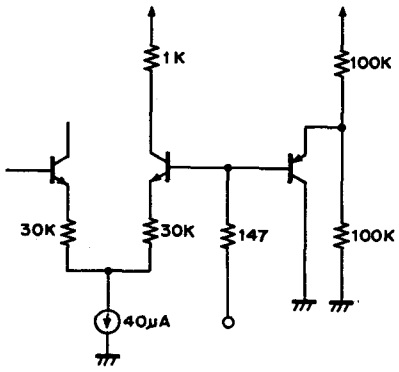


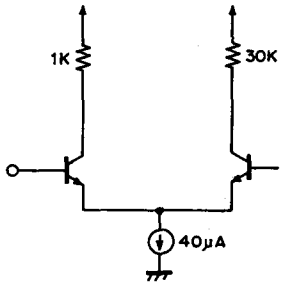
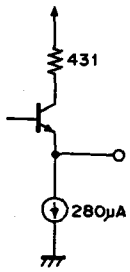
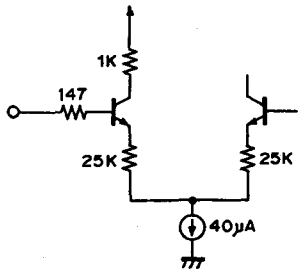
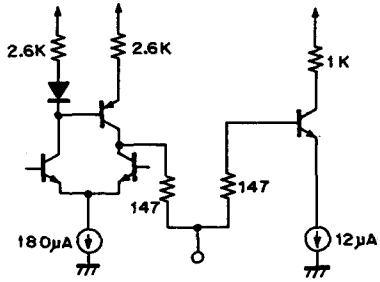
E89Z18 – ST

Pin Description

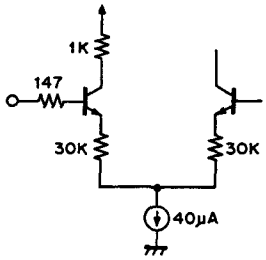
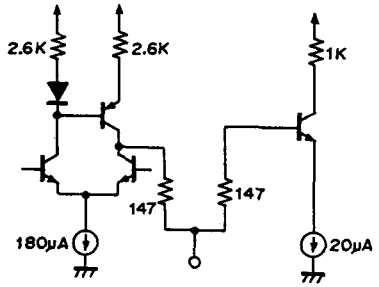
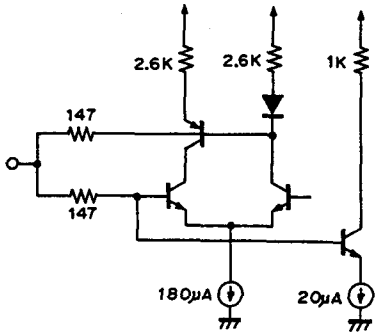
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	CLP C YH	3 to 3.5V		Capacitor connecting pin for YH clamp (Clamp at CLP2)
2	DL YH IN	3.65V		DL YH signal input pin (Input from 1H delay line) Sig: Typ. 200mV (Positive polarity)
3	CLP C DL YH	2.6 to 3.8V		Capacitor connecting pin for DL YH clamp (Clamp at CLP4)
4	DL YH OUT	2.7 to 3.1V		DL YH signal output pin (To 1H delay line) Sig: Typ. 400mV Max. 600mV (Negative polarity)

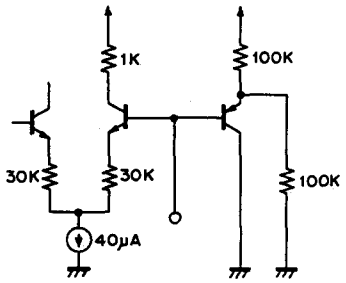
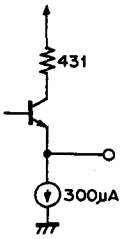
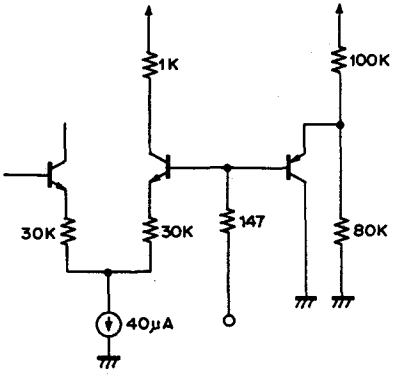
Note) Pin voltage for input and output pins indicate black level.

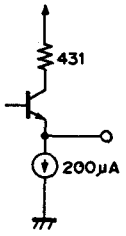
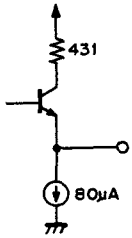
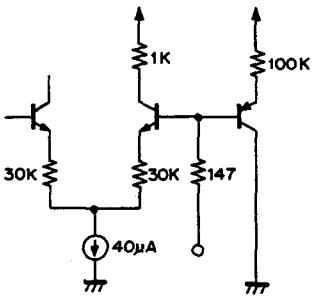
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
5	Y_H OUT1	1.9 to 2.3V		Y_{H1} signal output pin Sig: Typ. 1V Max. 1.5V (Positive polarity)
6	Y_H OUT2	1.9 to 2.3V		Y_{H2} signal output pin Sig: Typ. 1V Max. 1.5V (Positive polarity)
7	TP	2.6 to 3.0V (Y_H) 2.5 to 2.9V (G)		TP OUT (adjusting pin) 1H mode: Outputs Y_{H1}–Y_{H0} 0H mode: Outputs Gch C-slice OUT (Mode selection is executed through Pin 8)
8	DL Y_H GAIN	0V (0H Mode) 1.8 to 5V (1H Mode)		DL Y_H signal gain control pin (For 1H delay line gain compensation of Y_H) TP (Pin 7) mode selection 0H Mode: 0V 1H Mode: 1.8 to 5V
54	Y1 GAIN	0V: Common control by Pin 57 1.8 to 5V: Independent control		DLY_1 signal gain control pin (1H delay line gain compensation) 0V: DLY_1 signal gain control is executed in common with DLY_2 signal gain control. 1.8 to 5V: DLY_1 signal gain control is executed independently from DLY_2 signal gain control.

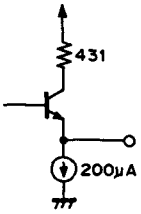
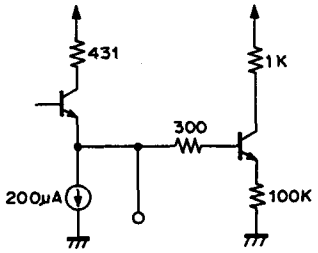
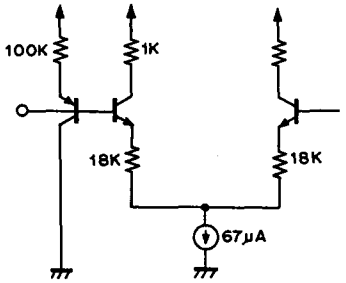
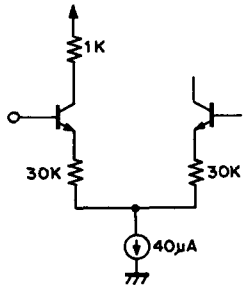
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
9	CLP4	5V 0		CLP4 pulse input pin (BLK clamp) (CMOS level input, V_{TH}=2.5V)
10	CLP2	5V 0		CLP2 pulse input pin (OPB clamp) (CMOS level input, V_{TH}=2.5V)
11	VAP OUT	2.6 to 3.0V		V-APCN signal output pin Note) Sig: Max. 1.2Vp-p
12	VAP GAIN	1.8 to 5V (Control)		V-APCN signal output level adjustment pin
13	CLP C VAP	3.4 to 3.8V		Capacitor connecting pin for VAP clamp (Clamp at CLP4)

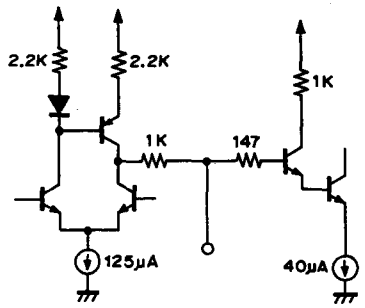
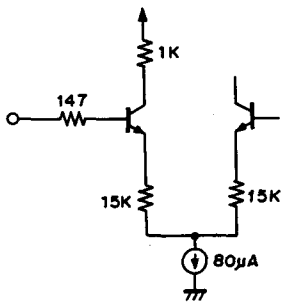
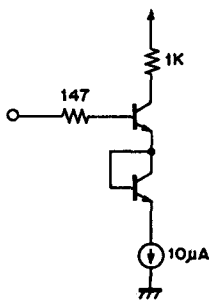
Note) V-APCN: Vertical Aperture Compensation

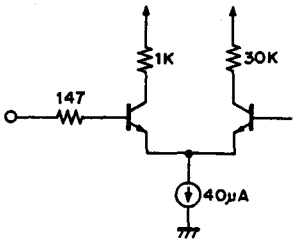
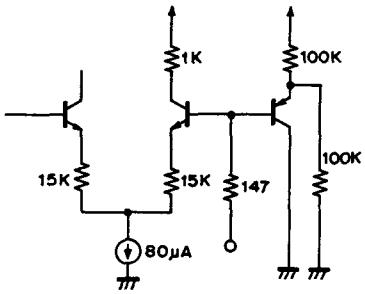
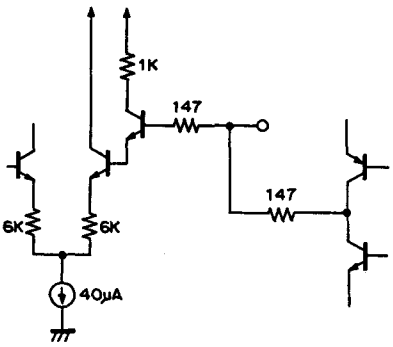
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
14	VAP SLICE	1.8 to 5V (Control)		V-APCN signal dark slice volume adjustment pin
15	CLP C CS	3.5 to 3.7V		Capacitor connecting pin for CS clamp (Clamp at CLP4)
16	CS IN	C-Couple input 2.9 to 3.3V		AGC CS signal input pin Sig: Max. 1V

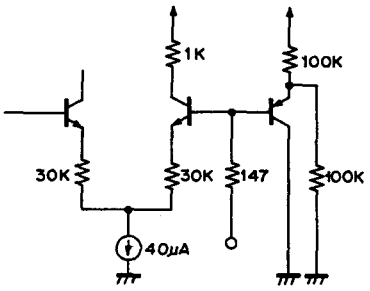
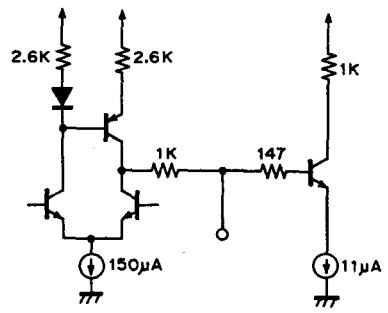
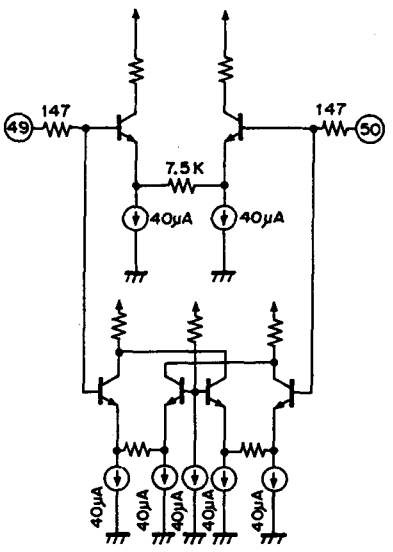
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
17	R – Y GAIN	0V: R–G output 1.8 to 5V: R–Y output		R–Y signal output level adjustment pin Pin 20 Mode select 0V: R–G output 1.8 to 5V: R–Y output
18	B – Y GAIN	0V: B–G output 1.8 to 5V: B–Y output		B–Y signal output level adjustment pin Pin 19 Mode select 0V: B–G output 1.8 to 5V: B–Y output
23	CS GAIN	1.8 to 5V (Control)		V-APCN CS signal gain control pin
19	B – Y OUT	2.75 to 3.15V (Hue OFF) 2.35 to 2.75V (Hue ON)		B–Y signal output pin Sig: Typ. 590mVp-p
20	R – Y OUT			R–Y signal output pin Sig: Typ. 800mVp-p
46	DLC_0 OUT	1.8 to 2.2V		DLC_0 signal output pin Sig: Typ. 200mVp-p Max. 600mVp-p (Positive polarity)
52	DLY_0 OUT	1.4 to 1.8V		DLY_0 signal output pin Sig: Typ. 200mVp-p Max. 600mVp-p (Positive polarity)
53	DLY_1 OUT	2.8 to 3.2V		DLY_1 signal output pin Sig: Typ. 200mVp-p Max. 600mVp-p (Positive polarity)
21	B – Y Hue	0V: Hue OFF		B–Y hue control pin
22	R – Y Hue	0V: Hue OFF		R–Y hue control pin

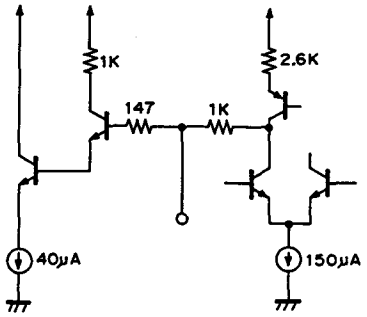
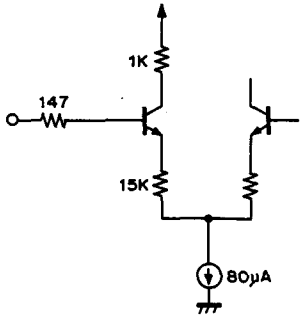
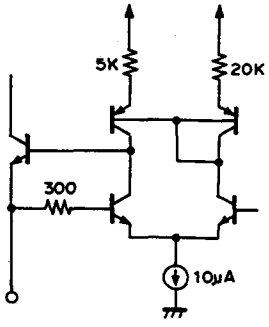
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
24	CS OUT	1.5 to 1.8V		CS signal output pin Sig: Max. 1V
25	Y_L OUT	1.9 to 2.3V		Y_L signal output pin
26	GND1			GND
27	C- γ CONT	0V: Typ. γ curve		Chroma (R.G.B) γ curve adjustment pin

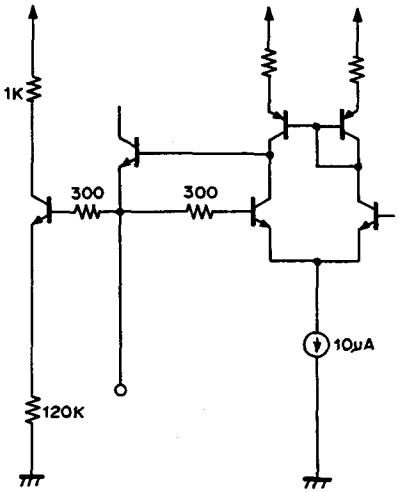
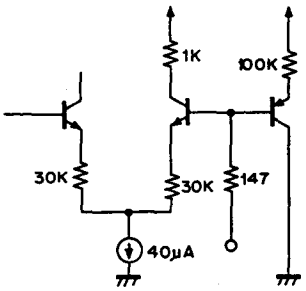
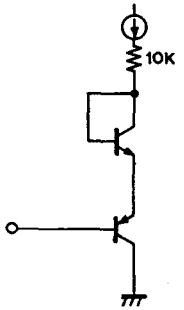
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
28	WB R	1.4 to 2V		R signal output pin WB Mode: Sig: Typ. 400mV γ Mode: Sig: Typ. 500mV
29	WB G	1.4 to 2V		G signal output pin WB Mode: Sig: Typ. 400mV γ Mode: Sig: Typ. 500mV
30	WB B	1.4 to 2V		B signal output pin WB Mode: Sig: Typ. 400mV γ Mode: Sig: Typ. 500mV
31	WB DC	1.4 to 2V		When used as output pin, it is an Auto WB DC output pin. Pin 28, 29 and 30 turn to WB mode. When connected to Vcc: Pins 28, 29 and 30 turn to γ mode.
32	C SLICE	0V: Slice OFF		Chroma (R.G.B) signals dark slice level adjustment pin
33	C LEVEL	1.8 to 5V (Control)		Chroma (R.G.B) gain control pin (Chroma modulation factor control for all 3 channels)
47	C_1 GAIN	1.8 to 5V (Control)		DL C_1 signal gain control pin (1H delay line gain compensation)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
34	CLP C R	3.0 to 3.6V		Capacitor connecting pin for R WB amplifier clamp (Clamp at CLP2)
35	CLP C G	3.0 to 3.6V		Capacitor connecting pin for G WB amplifier clamp (Clamp at CLP2)
36	CLP C B	3.0 to 3.6V		Capacitor connecting pin for B WB amplifier clamp (Clamp at CLP2)
37	R GAIN	1.8 to 5V (Control)		Rch WB amplifier gain control pin (Pre-WB)
40	B GAIN	1.8 to 5V (Control)		Bch WB amplifier gain control pin (Pre-WB)
38	R CONT	2.5 to 4.6V		Rch WB amplifier gain control pin
39	B CONT	2.5 to 4.6V		Bch WB amplifier gain control pin

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
41	ID	5V 0		ID pulse (color discrimination pulse) input pin (CMOS level V_{IH}=2.5V) ID=L $C_0 \rightarrow C_R$ $C_1 \rightarrow C_B$ ID=H $C_0 \rightarrow C_B$ $C_1 \rightarrow C_R$
42	B MTX	1.8 to 5V (Control) 0V (Preset)		B signal operations MTX coefficient adjustment pin (Coefficient 0.22) Refer to Note 2.
43	CLP C MPX2	2.7 to 3.1V		Capacitor connecting pin for MPX clamp (Clamp at CLP2)
44	CLP C MPX1	2.7 to 3.1V		Capacitor connecting pin for MPX clamp (Clamp at CLP2)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
45	R MTX	1.8 to 5V (Control) 0V (Preset)		R signal operations MTX coefficient adjustment pin (Coefficient 0.617) Refer to Note 2.
48	DLC1 IN	C-couple input 3.1 to 3.5V		DL C1 signal input pin Sig: Typ. 150mVp-p (Negative polarity)
55	DLY1 IN	C-couple input 3.6 to 4.0V		DL Y1 signal input pin Sig: Typ. 150mVp-p (Negative polarity)
56	DLY2 IN	C-couple input 3.6 to 4.0V		DL Y2 signal input pin Sig: Typ. 150mVp-p (Negative polarity)
49	S2 IN	1.9V		S2 signal input pin Sig: Typ. 500mV Max. 1500mV
50	S1 IN	1.9V		S1 signal input pin Sig: Typ. 500mV Max. 1500mV

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
51	CLP C Y_O	3.3 to 3.7V		Capacitor connecting pin for Y_O clamp (Clamp at CLP4)
57	Y_2 GAIN	1.8 to 5V (3H Mode) 0V (2H Mode)		DL Y_2 signal gain control pin (1H delay line gain compensation) V-APCON mode selection 0V: 2H Mode 1.8 to 5V: 3H Mode
58	GND2			GND
59	LPF Adj. 1	1.8 to 2.2V		Connecting pin of the external resistor that determines the characteristics of the LPF for 1H DL. (External resistor in the range of 15 to 27kΩ)
60	LPF Adj. 2	1.8 to 2.2V		Connecting pin of the external resistor that determines the characteristics of the chroma LPF (LPF for R, G, B, CS). (External resistor in the range of 15 to 62kΩ)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
61	LPF Adj. 3	1.8 to 2.2V		Connecting pin of the external resistor that determines the characteristics of the LPF for V-APCN. (External resistor in the range of 15 to 62kΩ) When connected to Vcc, the LPF for V-APCN turns OFF.
62	Vcc			Power supply 5V (Typ.)
63	Y- γ CONT	0V (Typ. γ curve) 1.8 to 5V (Control)		YH γ curve adjustment
64	YH IN	0.95V		YH signal input Sig: Typ. 220mV Max. 660mV

Electrical Characteristics

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption		**ID**		25	34.5	43	mA
S2 – S1 Amp Gain		**SSG**	Input: *S1 IN*= – 62.5mV, *S2 IN*=62.5mV Calculations: *DLC₀ OUT/S1 IN*	– 3	– 1.95	– 1	dB
DLC₁ gain control	Max.	**DLC₁H**	Input: *DLC₁IN*=100mV Conditions: *C₁Gain*=5V *C-level*=5V Calculations: *(WB-R/DLC₁IN)* – **CG** Note 2)	6	7	9	dB
	Min.	**DLC₁L**	Conditions: *C₁Gain*=0V (Others same as **DLC₁H**)	– 2	– 0.85	0	dB
S1+S2 Amp		**SAG**	Input: *S1 IN*=500mV Calculations: *DLY₀OUT/S1 IN*	– 15	– 14	– 13	dB
Chroma matrix (Gch) Note 3)	Gch Y	**GY**	Input: *S1 IN=S2 IN*=300mV Conditions: *C-level*=5V Calculations: *WB-G* (*ID*=H, L average)	80	100	120	mV
	C_R/Y	**GC$_R$**	Input: *S1 IN=S2 IN*=62.5mV Conditions: *C-level*=5V Calculations: *WB-G*/**GY** (*ID*=L)	0.9	1	1.1	—
	– C_B/Y	**GC$_B$**	*ID*=H (Others same as **GC$_R$**)	– 1.1	– 1	– 0.9	—
Chroma matrix (Rch) Note 3)	Rch C_R	**RC$_R$**	Input: *S1 IN*= – 62.5mV, *S2 IN*=62.5mV Conditions: *C-level*=5V Calculations: *WB-R* (*ID*=L)	70	85	100	mV
	Y (Preset)	**RYP**	Input: *S1 IN=S2 IN*=500mV Conditions: *C-level*=5V Calculations: *WB-R*/**RC$_R$** (*ID*=H)	0.15	0.168	0.186	—
	Y (Max.)	**RYH**	*RMTX*=5V (Others same as **RYP**)	0.22	0.25	0.27	—
	Y (Min.)	**RYL**	*RMTX*=1.8V (Others same as **RYP**)	0.11	0.125	0.14	—
Chroma matrix (Bch) Note 3)	Bch – C_B	**BC$_B$**	Input: *S1 IN*=62.5mV, *S2 IN*= – 62.5mV Conditions: *C-level*=5V Calculations: *WB-B* (*ID*=H)	80	100	120	mV
	Y (Preset)	**BYP**	Input: *S1 IN=S2 IN*=500mV Conditions: *C-level*=5V Calculations: *WB-B*/**BC$_B$** (*ID*=H)	0.2	0.22	0.24	—
	Y (Max.)	**BYH**	*BMTX*=5V (Others same as **BYP**)	0.31	0.34	0.37	—
	Y (Min.)	**BYL**	*BMTX*=1.8V (Others same as **BYP**)	0.13	0.15	0.17	—

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
WB GAIN	RCONT Max.	**RCH**	Input : *DLC₁IN*= − 200mV Conditions : *C-level*=5V *RCONT*=4.6V (*ID*=H) Calculations : *WB-R*/**WB-RTyp.** Note 4) **WB-R Typ.** is the tested output of *WB-R* when RCONT is set to 4V (Other inputs, conditions same as **RCH**).	7.5	8.2	8.5	dB
	RCONT Min.	**RCL**	Test : *RCONT*=2.5V (Others same as **RCH**)	− 8.4	− 7.9	− 7.4	dB
	BCONT Max.	**BCH**	Input : *DLC₁IN*=150mV Conditions : *C-level*=5V *BCONT*=4.6V (*ID*=L) Calculations : *WB-B*/**WB-BTyp.** Note 4) **WB-B Typ.** is the tested output of *WB-B* when BCONT is set to 4V (Other inputs, conditions same as **BCH**).	7.5	8.2	8.5	dB
	BCONT Min.	**BCL**	Test : *BCONT*=2.5V (Others same as **BCH**)	− 8.4	− 7.9	− 7.4	dB
	RGAIN Max.	**RGH**	Input : *DLC₁IN*= − 200mV Conditions : *RCONT*=2.5V *RGAIN*=5V *C-level*=5V (*ID*=H) Calculations : *WB-R*/**WB-RMin.** **WB-R Min.** is the tested *WB-R*, when tested under the same conditions as **RCL**.	8.6	9.2	—	dB
	BGAIN Max.	**BGH**	Input : *DLC₁IN*=150mV Conditions : *BCONT*=2.5V *BGAIN*=5V *C-level*=5V (*ID*=L) Calculations : *WB-B*/**WB-BMin.** **WB-B Min.** is the tested *WB-B*, when tested under the same conditions as **BCL**.	11.4	12.2	—	dB

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Bch color difference matrix Note 5)	R – G OUT/ WB-B	**BMBY**	Input : *S1IN*=200mV *S2IN*=160mV *DLC1IN*=220mV Conditions : *C-γ CONT=WB DC= C-Slice=C-level*=5V *RCONT*=2.5V *BCONT*=4.6V (*ID*=L) Calculations : *B – Y OUT/WB-B*	0.4	0.44	0.48	—
	R – Y OUT/ WB-B	**BMRY**	Conditions : *R – Y GAIN*=1.8V Calculations : *R – Y OUT/WB-B* (Others same as **BMBY**)	– 0.24	– 0.21	– 0.17	—
	B – Y GAIN Max.	**BMG**	Conditions : *BCONT*=4V 1. *B–Y OUT* is tested when *B–Y gain*=0V and taken as **A**. (Other conditions are the same as **BMBY**) 2. *B–Y OUT* is tested when *B–Y gain*=5V and taken as **B**. (Other conditions are the same as **BMBY**) Calculations : **B/A**	3.0	3.3	—	—
	B – Y Hue Max.	**BMHH**	Conditions : *B – Y HUE*=1.8V (Others same as **BMBY**) Calculations : *R – Y OUT*/**B – Y Typ.** **B–Y Typ.** is the value of the tested *B–Y OUT* when *B–Y hue*=0V (Other conditions are the same as **BMBY**). Note 6)	0.58	0.68	—	—
	B – Y Hue Min.	**BMHL**	*B – Y HUE*=5V (Others same as **BMHH**)	—	– 0.67	– 0.58	—
Gch color difference matrix Note 5)	R – Y/R – G	**GMR**	Input : *S1IN*=830mV *S2IN*=660mV *DLC1IN*= – 230mV Conditions : *WB-DC=C-level*=5V *RCONT=BCONT*=2.5V 1. *R–Y OUT* is tested when *R–Y gain*=0V and taken as **A**. 2. *R–Y OUT* is tested when *R–Y gain*=1.8V and taken as **B**. Calculations : **B/A**	0.81	0.85	0.89	—
	B – Y/B – G	**GMB**	Input : (The same as **GMR**) Conditions : 1. B–Y OUT is tested when B–Y gain=0V and taken as A. 2. B–Y OUT is tested when R–Y gain=1.8V and taken as B. (Others same as **GMR**) Calculations : **B/A**	0.63	0.66	0.7	—

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
C-Slice	Typ. − Min.	**CSLL**	Input : *DLY1IN*= − 400mV Conditions : *C-level*=5V *Y1GAIN*=1.8V *C-Slice*=1.8V (*ID*=H) Calculations : **C-SliceTyp.** -*TP* **C-Slice Typ.** is the *TP* output of *C-Slice*=0V.	0	5	15	mV
	Typ. − Max.	**CSLH**	Conditions : *C-Slice*=5V (Others same as **CSLL**)	95	120	145	mV
Gch γ curve	C- γ CONT=0V Gch-WB=400mV	**γ Typ.**	Input : *DLY1IN*= − 200mV *S1IN=S2IN*=500mV Conditions : *Y1GAIN*=1.8V *C-level* is varied and adjusted to obtain 400mV at *WB-G*. After that *C-level* is fixed during test. *WB-DC* is set to OPEN during *C-level* adjusted and set to 5V during test. Calculations : *WB-G* is tested.	450	500	550	mV
	C- γ CONT=0V Gch-WB=800mV	**γ L8**	Input : *DLY1IN*= − 400mV *S1IN=S2IN*=1000mV Conditions: Same as **γ Typ.** Calculations: *WB-G*/ **γ Typ.**	1.13	1.2	1.25	—
	C- γ CONT=0V Gch-WB=100mV	**γ L1**	Input : *DLY1IN*= − 50mV *S1IN=S2IN*=125mV (Others same as **γ L8**)	0.36	0.4	0.44	—
	C- γ CONT=1.8V Gch-WB=400mV	**γ M4**	Input : *DLY1IN*= − 200mV *S1IN=S2IN*=500mV Conditions: *C γ CONT*=1.8V Calculations: *WB-G*/ **γ Typ.**	0.9	1	1.1	—
	C- γ CONT=1.8V Gch-WB=800mV	**γ M8**	Input : *DLY1IN*= − 400mV *S1IN=S2IN*=1000mV (Others same as **γ M4**)	1.13	1.2	1.25	—
	C- γ CONT=1.8V Gch-WB=100mV	**γ M1**	Input : *DLY1IN*= − 50mV *S1IN=S2IN*=125mV (Others same as **γ M4**)	0.45	0.5	0.55	—
	C- γ CONT=5V Gch-WB=400mV	**γ H4**	Input: *DLY1IN*= − 200mV *S1IN=S2IN*=500mV Conditions: *C γ CONT*=1.8V Calculations: *WB-G*/ **γ Typ.**	0.9	1	1.1	—
	C- γ CONT=5V Gch-WB=800mV	**γ H8**	Input: *DLY1IN*= − 400mV *S1IN=S2IN*=1000mV (Others same as **γ H4**)	1.13	1.2	1.25	—
	C- γ CONT=5V Gch-WB=100mV	**γ H1**	Input: *DLY1IN*= − 50mV *S1IN=S2IN*=125mV (Others same as **γ H4**)	0.26	0.3	0.35	—

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Y γ	Y γ 1.0 (Typ.)	**Y γ T**	Input: *YHIN*=220mV Calculations: *DLYHOUT*	− 440	− 400	− 360	mV
	Y γ 2.0/ Y γ 1.0	**Y γ 2.0**	Input: *YHIN*=440mV Calculations: *DLYHOUT*/**Y γ T**	1.23	1.37	1.51	—
	Y γ 0.5/ Y γ 1.0	**Y γ 0.5**	Input: *YHIN*=110mV Calculations: *DLYHOUT*/**Y γ T**	0.59	0.66	0.73	—
	Y γ 0.5 (Max.)/ Y γ 1.0	**Y γ H**	Input: *YHIN*=110mV Conditions: *Y γ CONT*=1.8V Calculations: *DLYHOUT*/**Y γ T**	0.64	0.71	0.78	—
	Y γ 0.5 (Min.)/ Y γ 1.0	**Y γ L**	Input: *YHIN*=110mV Conditions: *Y γ CONT*=5V Calculations: *DLYHOUT*/**Y γ T**	0.54	0.6	0.66	—
TP	TP (YH)	**TPY**	Input: *YHIN*=220mV Conditions: *DLYHGAIN*=1.8V Calculations: *TP*/*DLYHOUT*	− 5	− 4	− 3	dB
	TP (DLY*H*)	**TPDY**	Input: *DLYHIN*=**Y γ T** × 0.7 Conditions: Same as **TPY** Calculations: *TP*/ − *DLYHOUT* Note 7)	− 5	− 4	− 3	dB
	TP (GWBS)	**TPG**	Input: *S1IN*=*S2IN*=500mV *DLY1IN*=200mV Conditions: *Y1GAIN*=1.8V Calculations: *TP*/*WB-G*	− 2	0	2	dB
YH AMP	Min. Gain	**YLG**	Input: *YHIN*=220mV *DLYHIN*= − [**Y γ T** × − 3.5dB] Conditions: *DLYHGAIN*=1.8V Calculations: *TP* is tested to check that the signal level is below 0mV in relation to black level. Note 8)	—	—	3.5	dB
	Max. Gain	**YHG**	Input: *YHIN*=220mV *DLYHIN*= − [**Y γ T** × − 12dB] Conditions: *DLYHGAIN*=5V Calculations: *TP*TP is tested to check that the signal level is over 0mV in relation to black level. Note 8)	12	—	—	dB
Chroma level Max./Min.		**GCL**	Input: *DLC1IN*=200mV Conditions: 1. WB-G is tested when C-level=5V and taken as GC-level Min. 2. WB-G is tested when C-level=1.8V and taken as GC-level Max. (Both 1 and 2 test at ID-H.) Calculations: **GC-level Max./GC-level Min.**	1.55	1.65	1.75	—
WB DC		**WDDC**	Test: *WB-DC*	1.4	1.6	2	V

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Y_L Note 5)	Y_LOUT/ R Y OUT	Y_LR	Input: *S1IN*=150mV *S2IN*=450mV Conditions: *C- Y CONT=WB* *DC=C-Slice=* *C-level*=5V *RCONT*=4.6V *BCONT*=2.5V *BGAIN*=1.8V (*ID*=L) Calculations: *Y_LOUT/WB-R*	0.27	0.3	0.34	—
	Y_LOUT/ B Y OUT	Y_LB	Input: *S1IN*=200mV *S2IN*=160mV *DLC_1IN*=220mV Conditions: *C- Y CONT=WB* *DC=C-Slice=* *C-level*=5V *RCONT*=2.5V *BCONT*=4.6V(*ID*=L) Calculations: *Y_LOUT/WB-B*	0.08	0.1	0.12	—
	Y_LOUT/ G Y OUT	Y_LG	Input: *S1IN*=830mV *S2IN*=660mV *DLC_1IN*= − 230mV Conditions: *WB-DC=C-level*=5V *RCONT=BCONT*=2.5V Calculations: *Y_LOUT/WB-G*	0.54	0.6	0.66	—
Y_HOUT1 (OH mode)		YH1Z	Input: *Y_HIN*=220mV Calculations: *Y_HOUT1* is tested.	900	1000	1100	mV
Y_HOUT1 1H/0H		YH1O	Input: *DLY_HIN*= − (Y Y T × − 4dB) Conditions: *DLY_HGAIN*=1.8V Calculations: *Y_HOUT1/*YH1Z Note 8)	− 1	0	1	dB
Y_HOUT2 (0H)/Y_HOUT1		YH2Z	Input: *Y_HIN*=220mV Calculations: *Y_HOUT2/*YH1Z	− 1	0	1	dB
Y_HOUT2 (1H)/Y_HOUT1		YH2O	Input: *Y_HIN*=220mV Conditions: *DLY_HGAIN*=1.8V Calculations: *Y_HOUT2/*Y_HOUT2Typ. Y_HOUT2Typ. is *Y_HOUT2* output tested at YH2Z.	− 6.5	− 6	− 5.5	dB
VAP Typ. Note 9)		VAPT	Input: *S1IN=S2IN*=125mV Conditions: *VAP GAIN*=1.8V *VAP Slice*=1.8V *Y_2 GAIN*=1.8V Calculations: *VAP OUT* is tested.	− 250	− 200	− 150	mV
VAP Slice Note 9)		VS	Input: *S1IN=S2IN*=1000mV Conditions: *Y_2 GAIN*=1.8V 1. VAP OUT is tested when VAP Slice=1.8V and taken as SMin. 2. VAP OUT is tested when VAP Slice=5V and taken as SMax. Calculations: SMax. − SMin. Note 10)	256	320	384	mV

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
DLY_1 gain Note 11)	Min.	**DY_1L**	Input: *S1IN=S2IN*=500mV *DLY_1IN*= − 200mV Conditions: *VAP GAIN=VAP Slice=Y_1GAIN*=1.8V Calculations: *VAP-OUT* is tested to check that the signal level is over 0mV in relation to black level.	—	—	0	dB
	Max.	**DY_1H**	Input: *S1IN=S2IN*=500mV *DLY_1IN*= − 110mV Conditions: *VAP GAIN=VAP Slice*=1.8V *Y_1GAIN*=5V Calculations: *VAP-OUT* is tested to check that the signal level is below 0mV in relation to black level.	5	—	—	dB
DLY_2 gain Note 11)	Min.	**DY_2L**	Input: *S1IN=S2IN*= − 167mV *DLY_2IN*= − 66.7mV Conditions: *VAP GAIN=VAP Slice=$Y_1GAIN=Y_2GAIN$*=1.8V Calculations: *VAP-OUT* is tested to check that the signal level is over 0mV in relation to black level.	—	—	0	dB
	Max.	**DY_2H**	Input: *S1IN=S2IN*= − 167mV *DLY_2IN*= − 37.5mV Conditions: *Y_2GAIN*=5V (Others same as **DY_2L**) Calculations: *VAP-OUT* is tested to check that the signal level is below 0mV in relation to black level.	5	—	—	dB
CS Note 12)	VCS Typ.	**VCST**	Input: *S1IN=S2IN*=167mV Conditions: *$Y_1GAIN=Y_2GAIN$*=1.8V *CS GAIN*=5V Calculations: CS OUT is tested.	90	120	150	mV
	VCS Min.	**VCSL**	Conditions: *CS GAIN*=0V (Others same as **VCST**) Calculations: *CS OUT*/**VCST**	—	0	0.05	—
	VCS Max.	**VCSH**	Conditions: *CS GAIN*=1.8V (Others same as **VCSL**)	4.4	—	—	—
	CS Typ.	**CST**	Input: *CS-IN*=500mV Calculations: *CS-OUT* is tested.	440	465	490	mV

Note 1) For pins without specific instructions regarding input, feed the DC value shown on the Test Circuit. Calculations are mentioned utilizing the pin name or the electrical characteristics symbols. Otherwise, for exceptional notations explanatory notes, are given with every case.

Note 2) In this item, the gain of DLC_1 amplifier exclusively is calculated. **CG** is the gain of the system from *DLC_1 IN* to *WB-R* from which DLC_1 GC amplifier gain has been excluded.
— **CG** calculating method —
In the actual calculation, the system on C_0 side is utilized.
Input: *S1IN*=–62.5mV *S2IN*=62.5mV
Condition: Same as **DLC_1H**
Calculations: **CG**=20log (*WB-R/DLC_0OUT*)

Note 3) Chroma matrix operations
$R = 2\ [C_R + \alpha Y]$ α : Control with **RMTX** (Preset 0.167)
$G = Y - (C_R + C_B)$
$B = 2\ [C_B + \beta (Y - C)]$ β : Control with **BMTX** (Preset 0.22)

Note 4) With the typical gain taken when *R CONT* is at 4V, compare with the gain during Max. and Min. The same for *B CONT*.

Note 5) Adjustment and testing is performed so that signals are output only for each of R, G, B channels respectively.

Note 6) Comparison with *B–Y OUT* when *R–Y HUE*=0V (HUE OFF).
The same for *B–Y HUE*.

Note 7) The compensation of difference in gain of Y_{H0} andY_{H1} is as follows.
1) At DLY_H GAIN=1.8V, DLY_H amplifier gain is 3dB.
2) Test DLY_H OUT (tested at YrT) when Y_H IN=220mV signal is input.
3) The difference in gain between Y_{H0} and Y_{H1} is compensated by inputting the signal as –3dB to DLY_H IN.

Note 8) The amplifier input is varied and the gain confirmed.

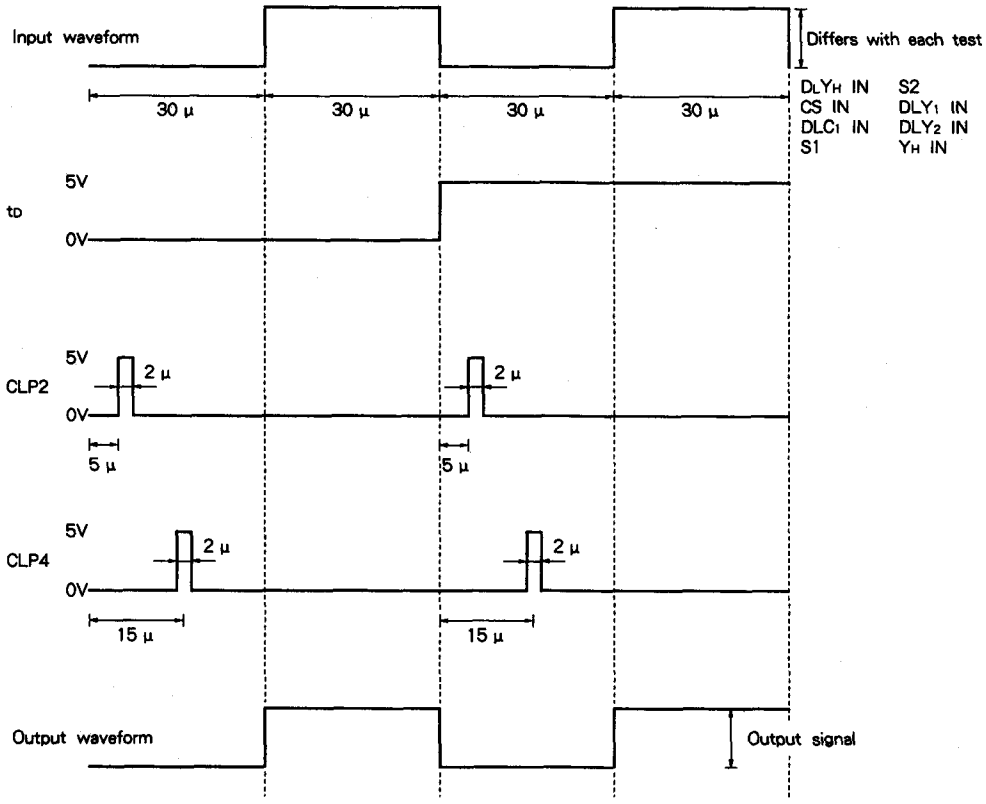
Note 9) VAP (Vertical Aperture Compensation)

Note 10) Dark slice variable volume. (Output level difference between the value slice volume at Max. and slice volume at Min.)

Note 11) Utilizing V-APCN 2H mode, DLY_1 amplifier exclusive gain is obtained through operations. However, as the amplifier gain cannot be tested directly, only the upper and lower limits of the gain control are checked according to the following method.
(a) Lower limit check
S1 IN=S2 IN=500mV (At that time KNEE circuit input turns to 200mV)
DLY_1 IN=–200mV (For others refer to the conditions chart)
In this condition, if we have *VAP OUT* $\geq$ 0, this indicates that DLY_1 amplifier is below 0dB.
(b) Upper limit check
S1 IN=S2 IN=500mV
DLY_1 IN=–110mV (in (a) the –5dB of –200mV)
In this condition, if we have *VAP OUT* $\leq$ 0, this indicates that DLY_1 amplifier is above 5dB.

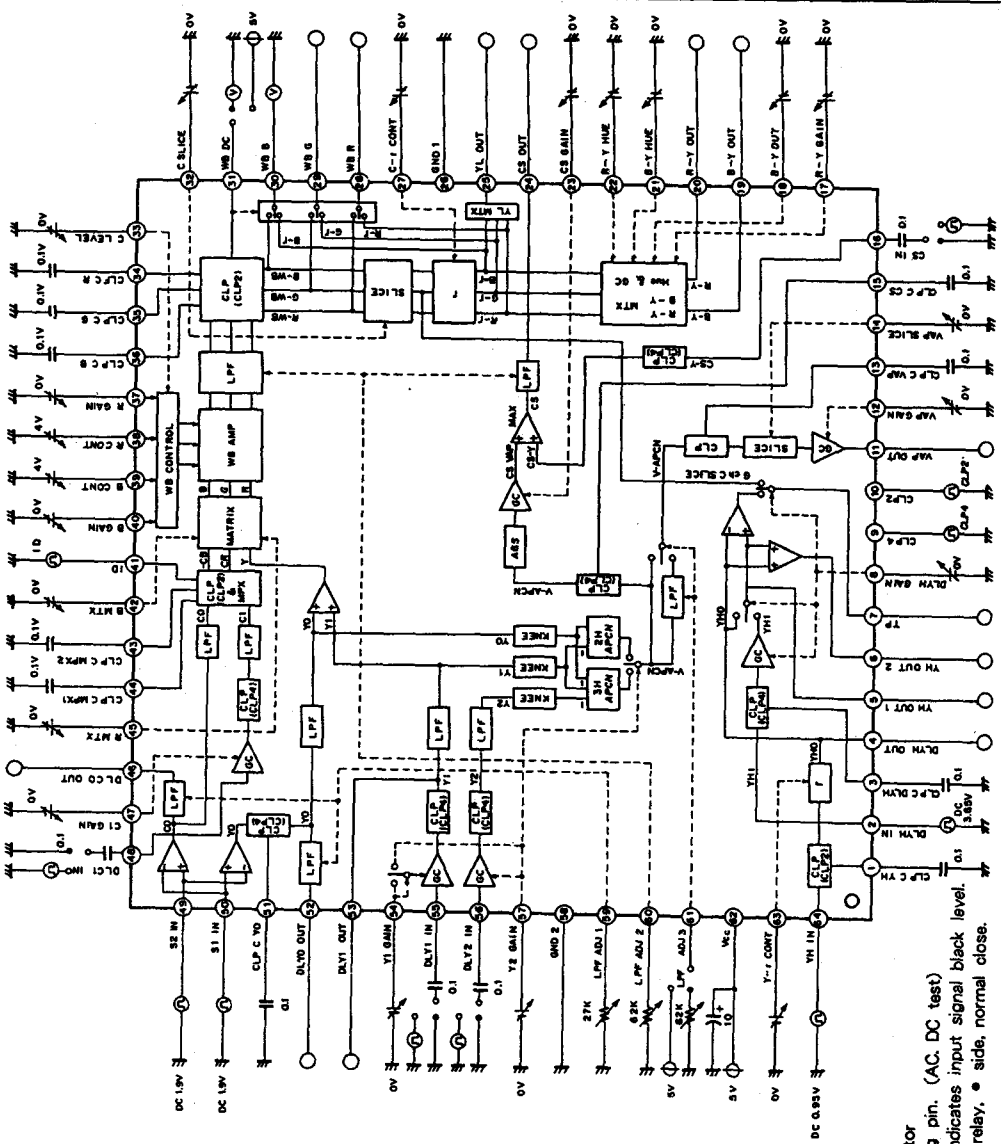
Note 12) CS (Chroma Suppress)

Timing Chart for Testing



DLYH OUT	B – Y OUT	WB_G
YH OUT1	R – Y OUT	WB_B
YH OUT2	CS OUT	DLC0 OUT
TP	YL OUT	DLY0 OUT
VAP_OUT	WB_R	DLY1 OUT

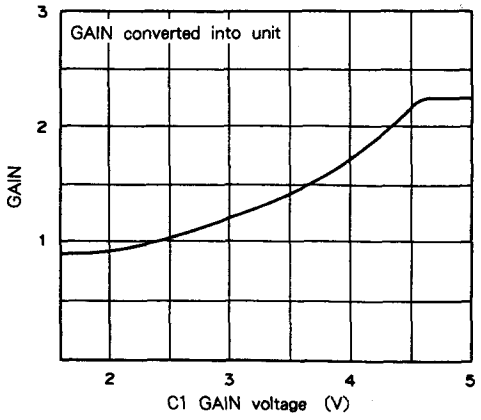
Test Circuit (Typ. setting)



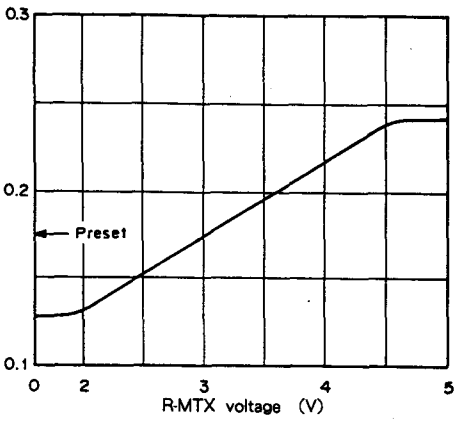
Note 1) µF is unit of capacitor
Note 2) —o indicates testing pin. (AC. DC test)
Note 3) Input pin DC value indicates input signal black level.
Note 4) —o/— indicate relay, • side, normal close.

Standard Control Characteristics (Vcc=5V, Ta=25℃)

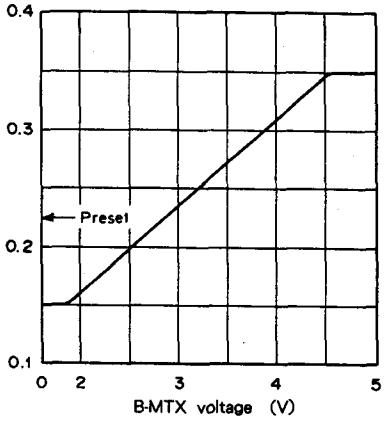
C1 GAIN control characteristics



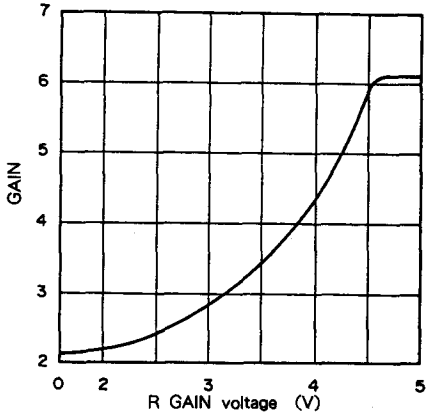
R-MTX coefficient



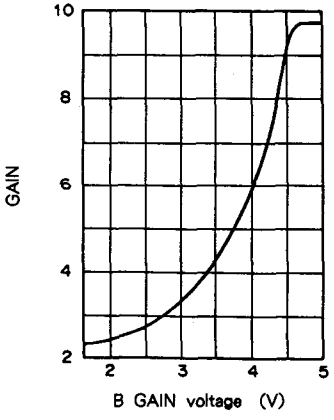
B-MTX coefficient



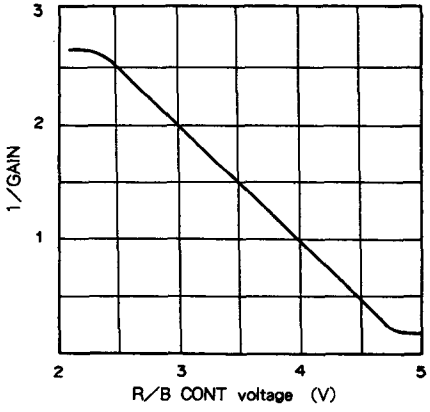
R GAIN control characteristics



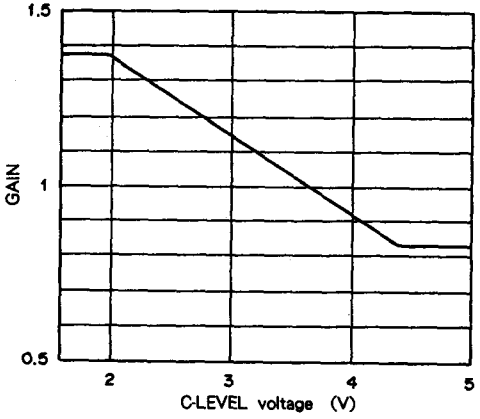
B GAIN control characteristics



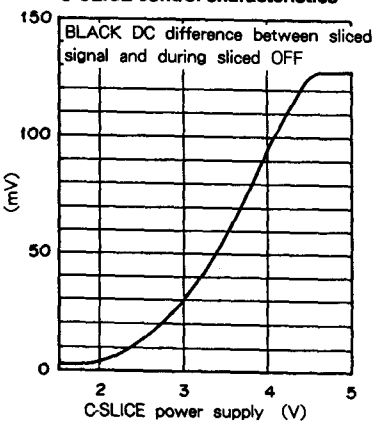
R/B CONT control characteristics



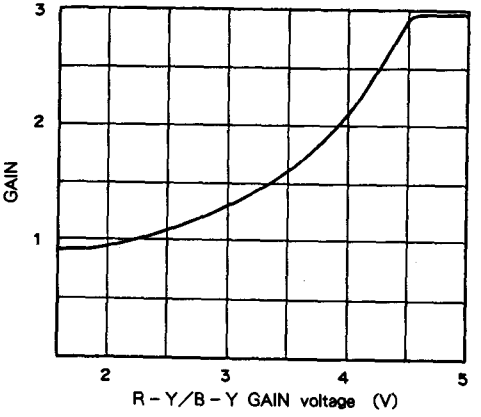
C-SLICE control characteristics



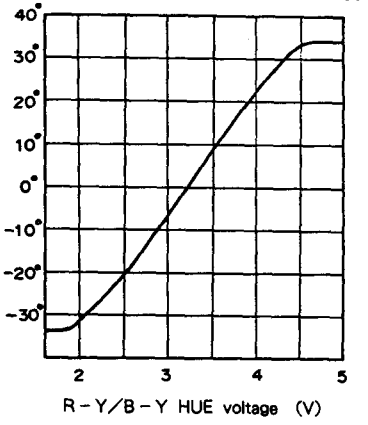
C-SLICE control characteristics



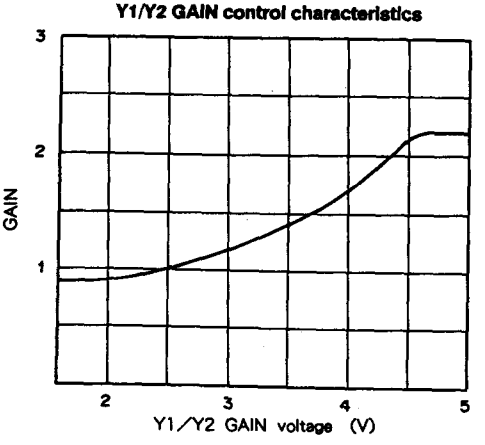
R – Y/B – Y GAIN control characteristics



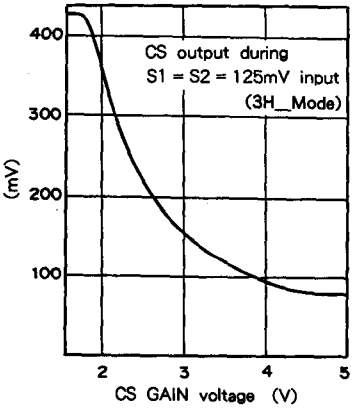
R – Y/B – Y HUE control characteristics



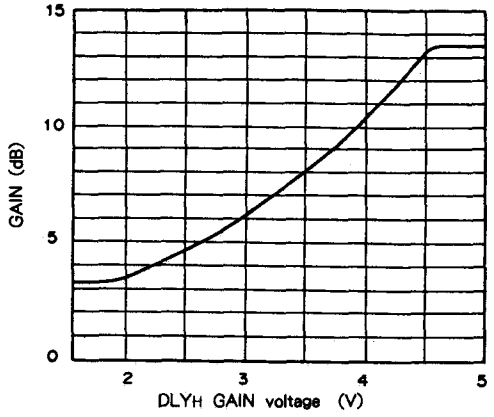
Y1/Y2 GAIN control characteristics



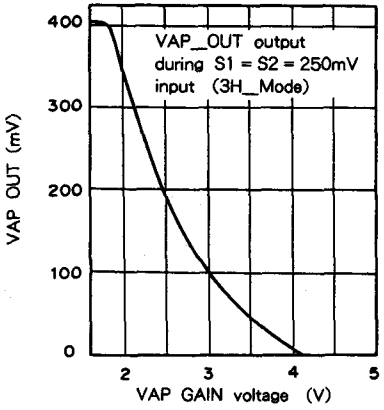
CS GAIN control characteristics



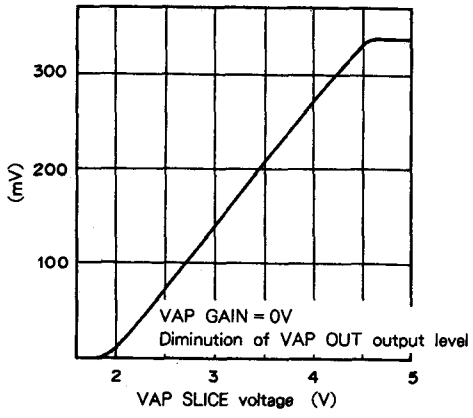
DLYH GAIN control characteristics



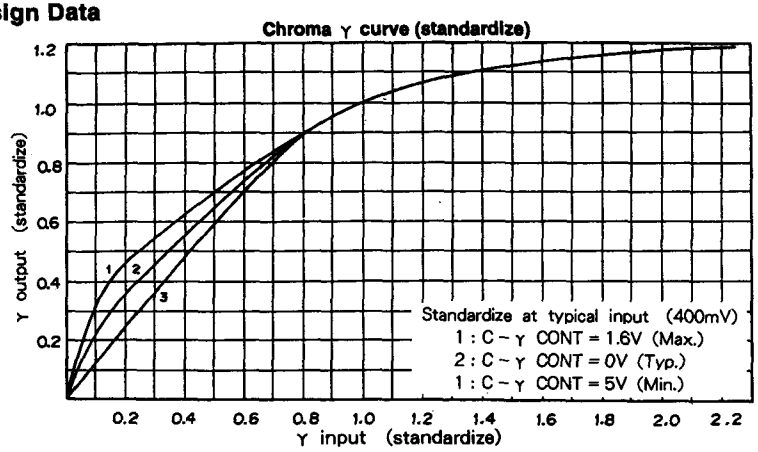
VAP control characteristics

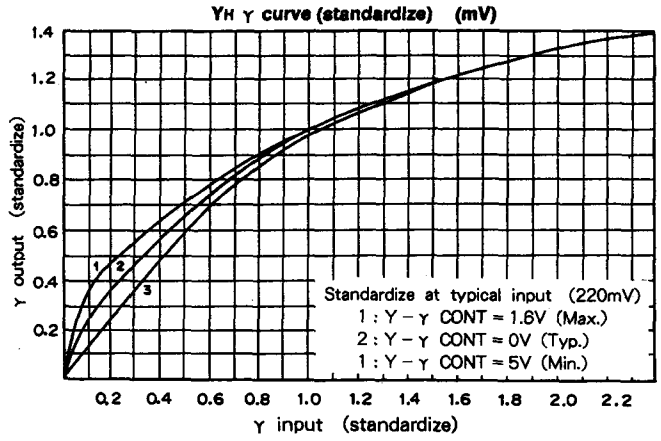


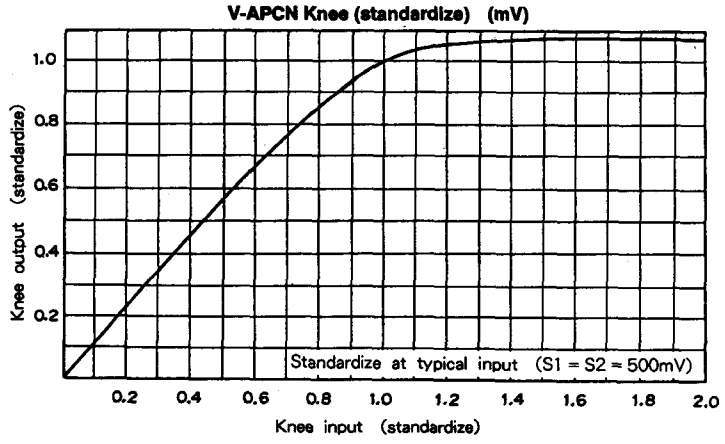
VAP SLICE control characteristics



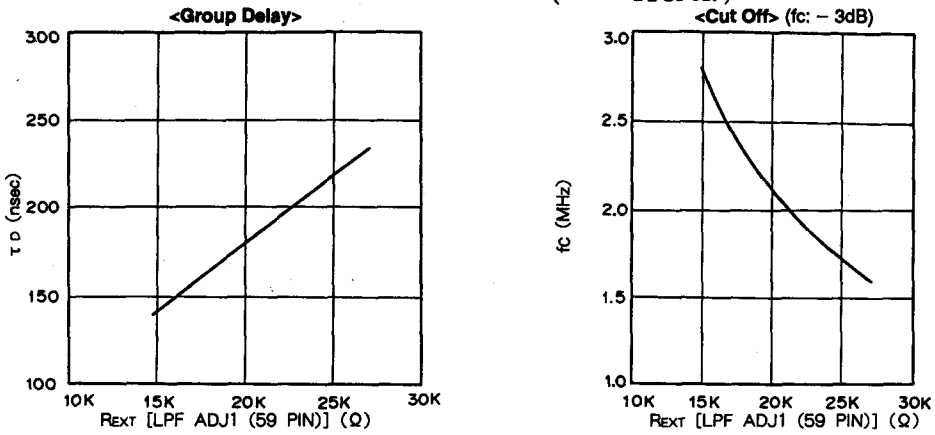
Standard Design Data



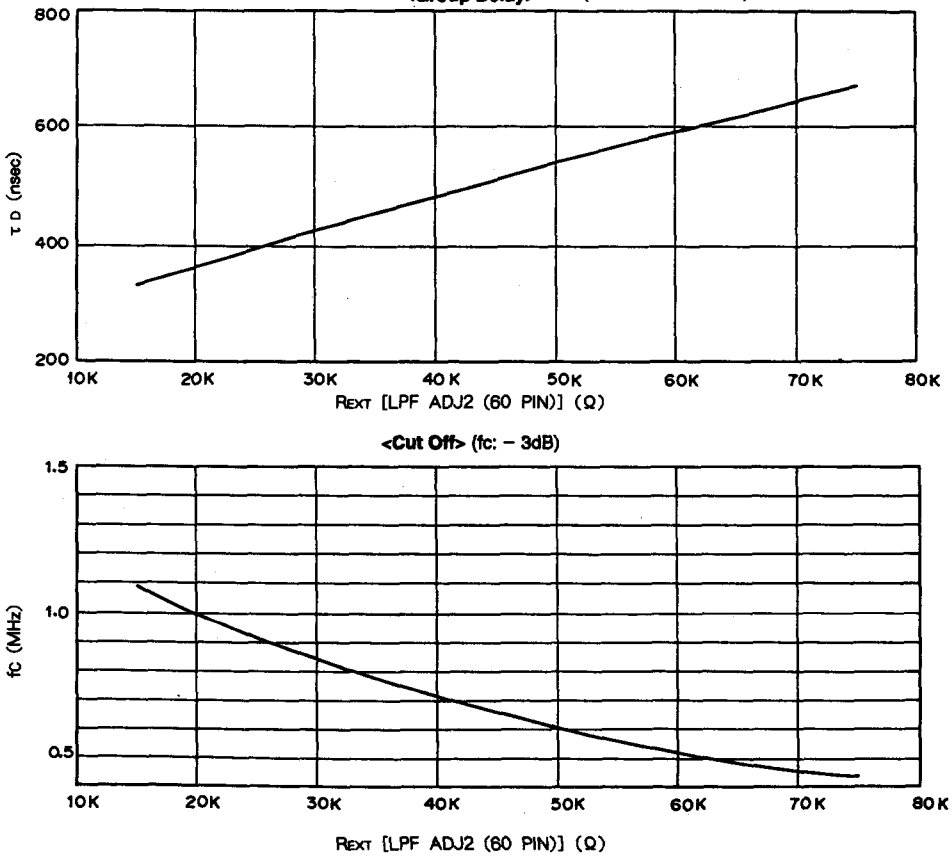




Pre-Filter Adjust characteristics (S1, S2 → DL Y0 out / DL C0 out)

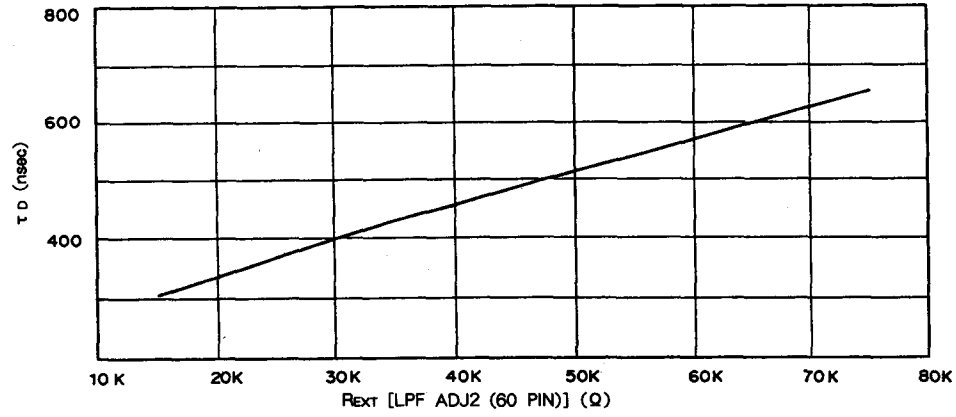


Chroma Adjust characteristics (S1, S2 → R – Y out / B – Y out)

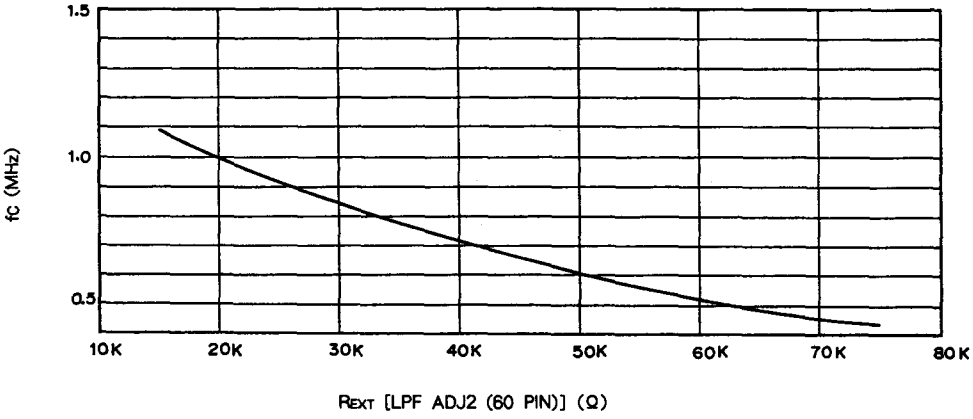


CS-VAP Adjust characteristics (S1, S2→CS OUT)

<Group Delay>



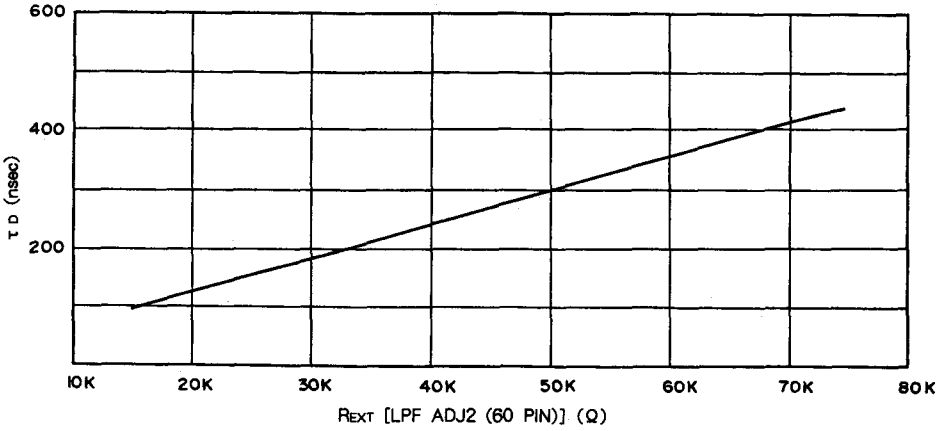
<Cut Off> (fc: − 3dB)



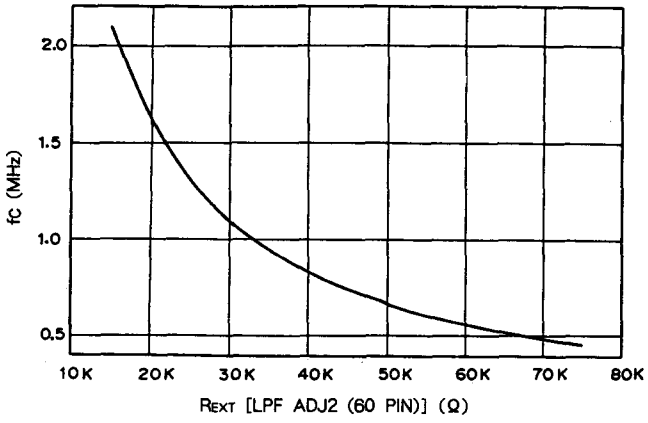
CS-Y LPF Adjust characteristics

(CS IN → CS OUT)

<Group Delay>



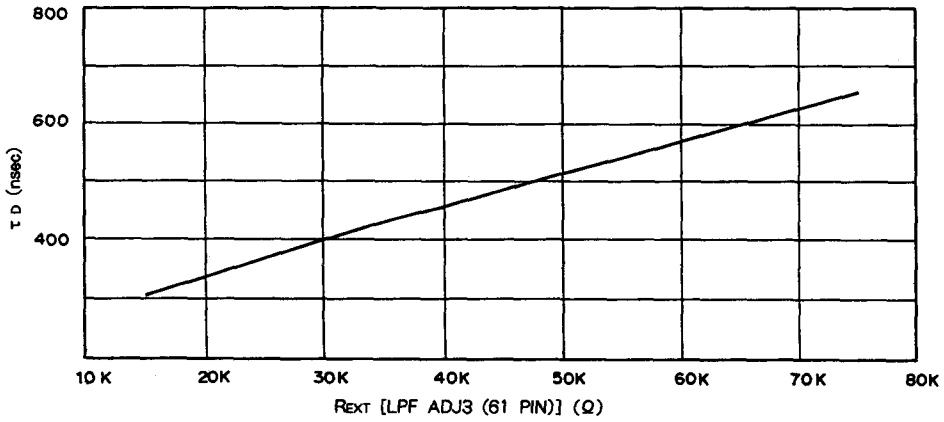
<Cut Off> (fc: − 3dB)



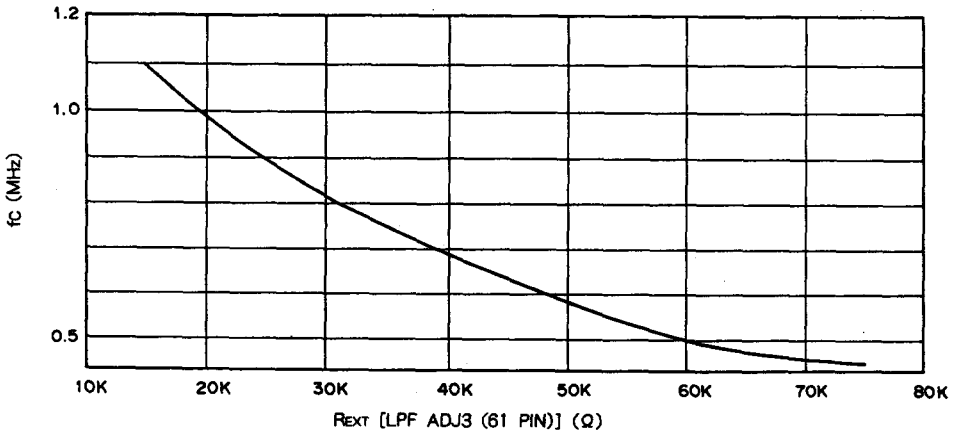
VAP LPF Adjust characteristics

VAP LPF Adjust characteristics (S1, S2→VAP OUT)

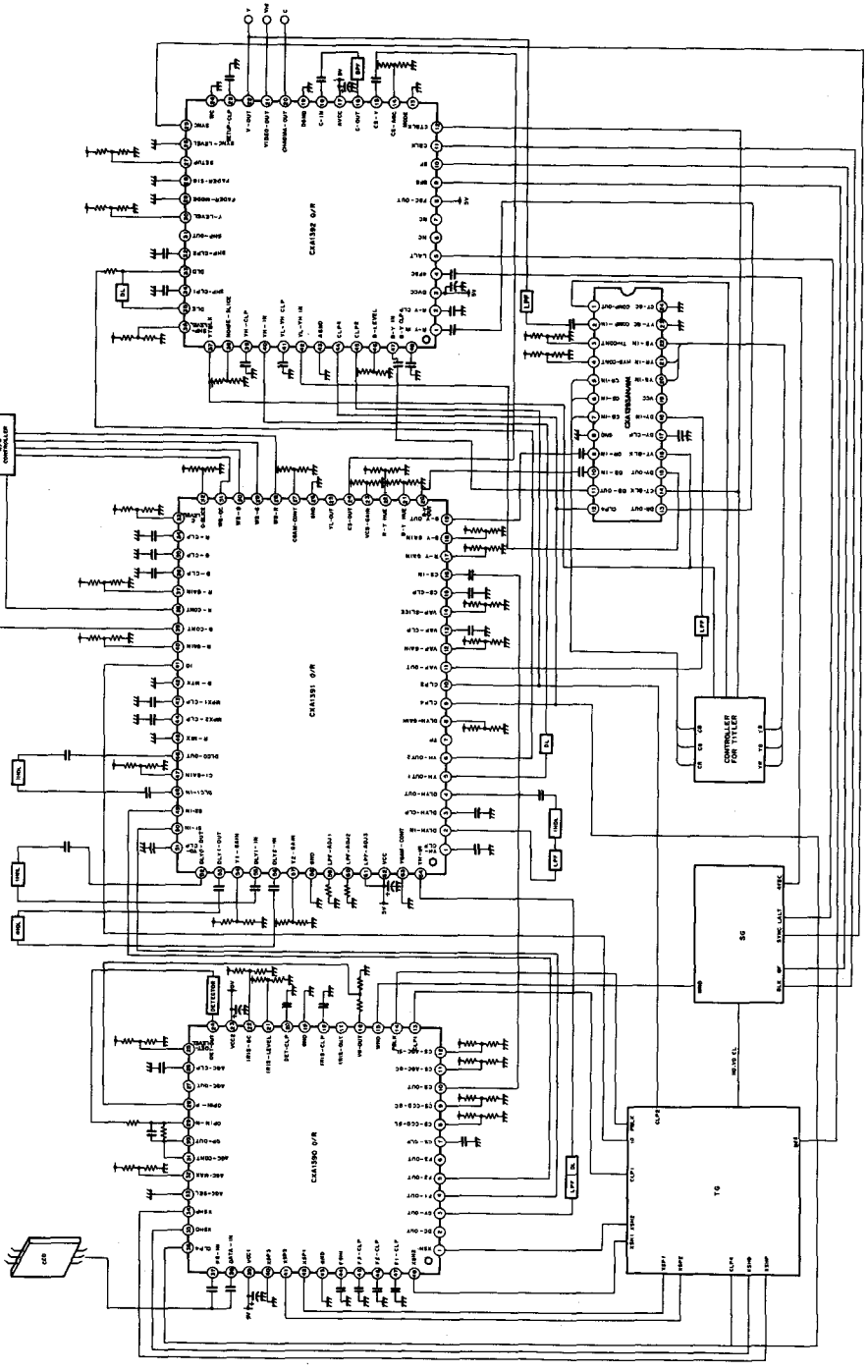
<Group Delay>



<Cut Off> (fc: – 3dB)



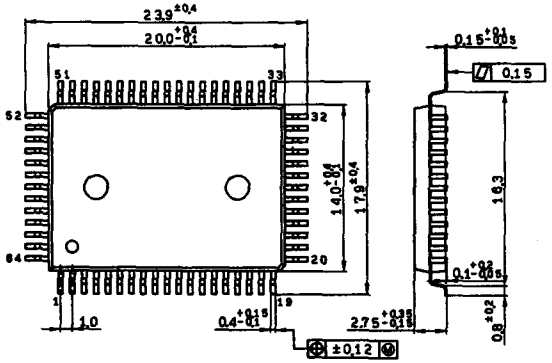
CXA1390 Series System Diagram



Package Outline Unit: mm

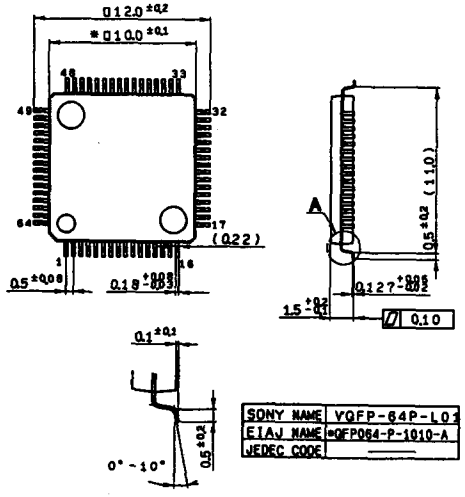
CXA1391Q

64pin QFP (Plastic) 1.5g



CXA1391R

64pin VQFP (Plastic) 0.3g



Detailed diagram of A

Note) Dimensions marked with * does not include resin residue.

SONY

CXA1339Q-Z/R

CCD Camera Processor

Description

CXA1339Q-Z and CXA1339R are processor ICs for CCD color cameras. These execute color coding, white balance, γ compensation, HUE control and other signal processing to color separated input signals. γ compensated R-Y, B-Y and YH, YL-YH signals are also shaped.

CXA1339Q-Z
48 pin QFP (Plastic)

CXA1339R
48 pin VQFP (Plastic)

Features

- The built-in color coding circuit makes it compatible with both types of CCD color filters, complementary color or primary color.
- Realizes high resolution through the adoption of YL-YH, and YH's Y signal processing.
- Compatible with negative/positive inversion.
- White balance is compatible with both automatic and one push button.
- Control pins have preset function.

Absolute Maximum Ratings (Ta=25°C)

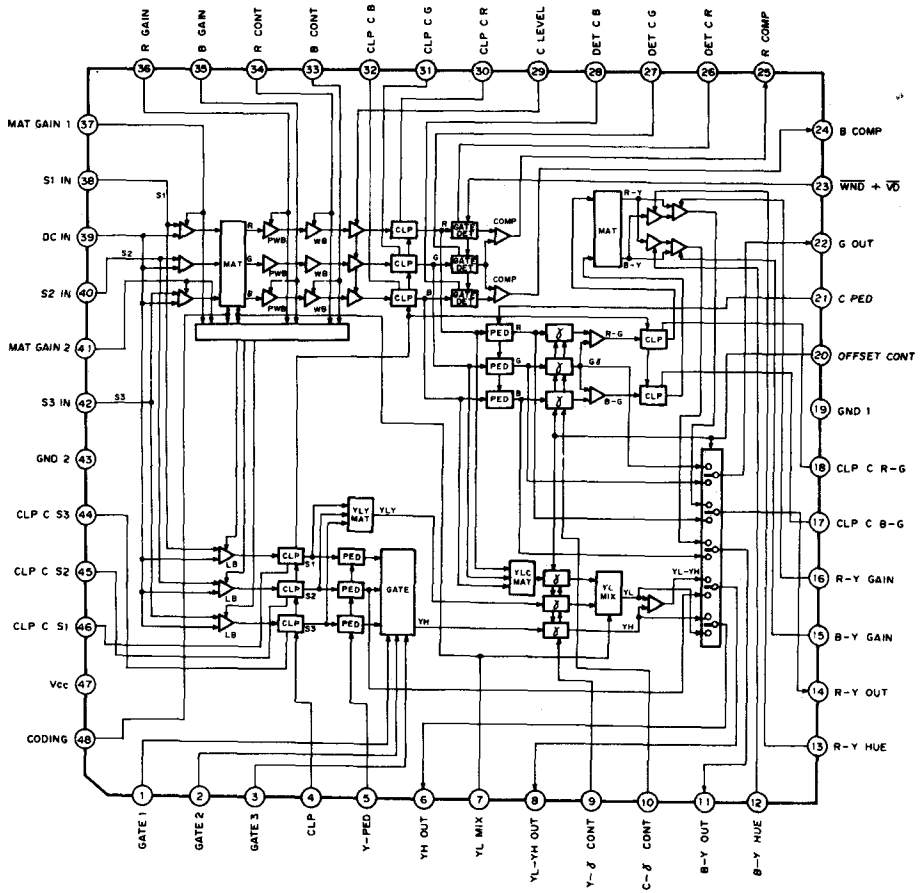
• Supply voltage	Vcc	7	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−65 to +150	°C
• Allowable power dissipation	PD	600	mW

Recommended Operating Condition

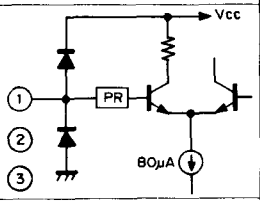
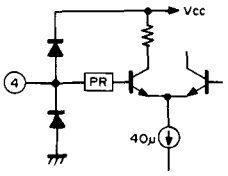
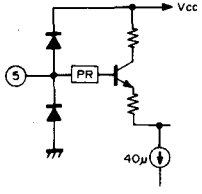
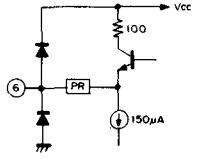
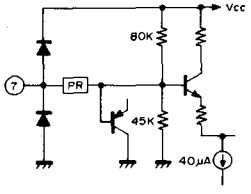
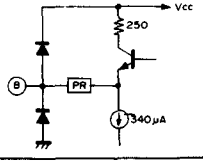
• Supply voltage	Vcc	5±0.25	V

E90112 – ST

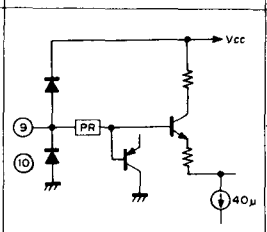
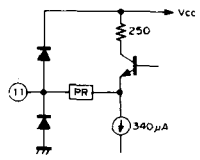
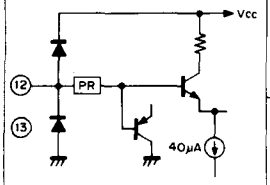
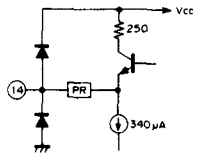
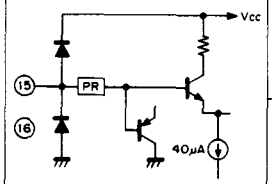
Block Diagram



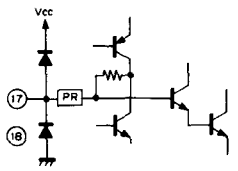
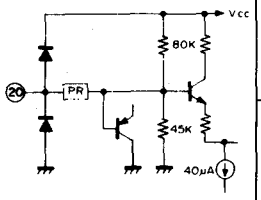
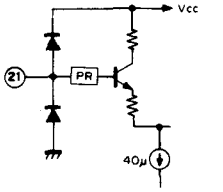
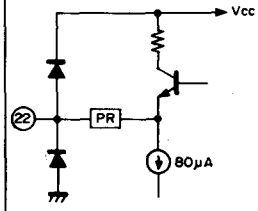
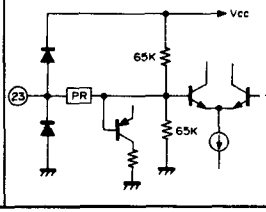
Pin Description

No.	Symbol	Equivalent circuit	Voltage	Description
1 2 3	GATE 1 GATE 2 GATE 3		3.1 to 5V* HI LEVEL 0 to 1.9V* LO LEVEL	With the gate pulse input of YH GATE, when GATE 1 turns to HI, YH=S1 when GATE 2 turns to HI, YH=S2. when GATE 3 turns to HI, YH=S3. It is active at HI.
4	CLP		3.1 to 5V* HI LEVEL 0 to 1.9V* LO LEVEL	This is the clamp pulse input pin for signals R, G, B, S1, S2, S3, R-G and B-G. It is active at HI.
5	Y PED		1.6 to 5V*	This is the Y signal dark slice level control pin.
			0 to 0.4V*	Preset mode pin (Y-PED OFF).
6	YH OUT		2.5V	When pin 20>1.6V YH output is on and when pin 20 <0.4V YL output is on.
7	YL MIX		1.6 to 5V*	This is the YLY and YLC MIX RATIO control pin. Color coding in complementary mode.
			0 to 0.4V*	Color coding in primary color mode. MIX ratio of YLY and YLC is YL 100% MAT GAIN 1 and 2 reach the same gain as S2 channel.
8	YL-YH OUT		3.0V	YL-YH output output when pin 20>1.6V.YTP output when pin 20<0.4V.

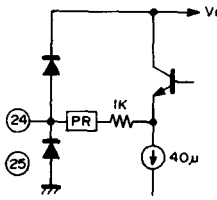
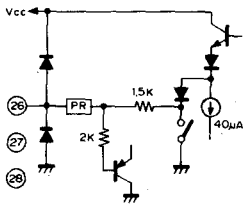
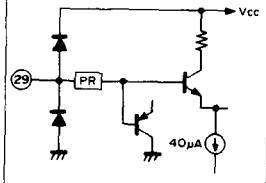
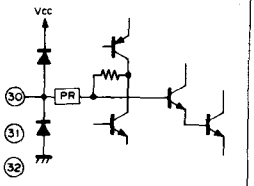
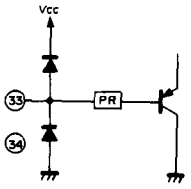
***Note)** External voltage applied

No.	.Symbol	Equivalent circuit	Voltage	Description
9 10	Y-γ CONT C-γ CONT		1.6 to 5V*	Y signal, chroma signal γ control.
			0 to 0.4V*	Preset mode (Typ. γ curve)
11	B-Y OUT		3.0V	When pin 20>1.6V B-Y output. When pin 20<0.4V B output.
12 13	B-Y HUE R-Y HUE		1.6 to 5V*	HUE control of B-Y, R-Y
			0 to 0.4V*	Preset mode (HUE OFF)
14	R-Y OUT		3.0V	When pin 20>1.6V R-Y output. When pin 20<0.4V R output.
15 16	B-Y GAIN R-Y GAIN		1.6 to 5V*	Gain control of B-Y, R-Y.
			0 to 0.4V*	Preset mode. Pin 14 R-G output. Pin 11, B-G output.

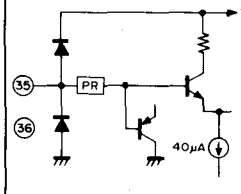
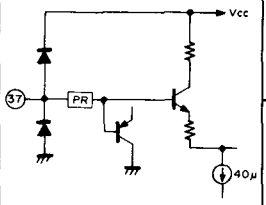
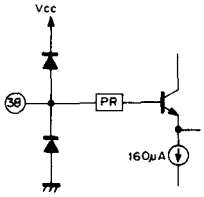
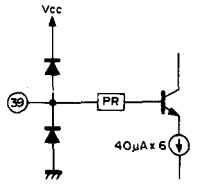
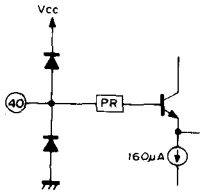
***Note)** External voltage applied

No.	Symbol	Equivalent circuit	Voltage	Description
17 18	CLP C B-G CLP C R-G		——	Capacitor connecting pin for B-G, R-G signal clamp.
19	GND1		GND*	GND pin for other than YH GATE part.
20	OFFSET CONT		1.6 to 5V*	Offset control during negative, positive inversion function. (For both Y and chroma systems)
			0 to 0.4V*	Output of pins 6, 8, 11, 14 and 22 changes.
21	C-PED		1.6 to 5V*	Dark slice level control of chroma signal.
			0 to 0.4V*	Preset mode (C-PED OFF)
22	G OUT		3.0V	When pin 20>1.6V Gγ output. When pin 20<0.4V G output.
23	$\overline{WND}+\overline{VD}$		2.5V 4.1 to 5V* WINDOW ON 0 to 0.9V* RESET ON	Pulse input pin for one push white balance system.

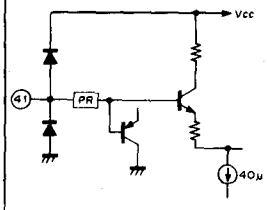
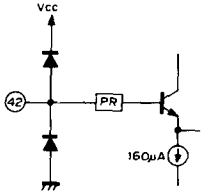
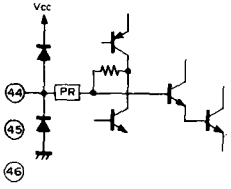
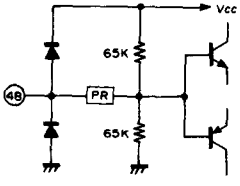
***Note)** External voltage applied

No.	Symbol	Equivalent circuit	Voltage	Description
24 25	B COMP R COMP		V_H>4V V_L<1V	Comparator output V_H is the output when B<G and R<G. V_L is the output when B>G and R>G.
26 27 28	DET C R DET C G DET C B		——	Connecting of capacitor for R, G, B signals peak detection.
29	C LEVEL		1.6 to 5V*	Chroma level control.
			0 to 0.4V*	Preset mode (0 dB for primary color mode, 6 dB for complementary color mode)
30 31 32	CLP C R CLP C G CLP C B		——	Connecting pin of capacitor for R, G, B signals clamp.
33 34	B CONT R CONT		0.4 to 2.5V*	White balance control.

***Note)** External voltage applied

No.	Symbol	Equivalent circuit	Voltage	Description
35 36	B GAIN R GAIN		1.6 to 5V*	Prewhite balance control.
			0 to 0.4V*	Preset mode (same gain as G channel)
37	MAT GAIN 1		1.6 to 5V*	Control of matrix amplifier 1.
			0 to 0.4V*	Preset mode (same gain as S2 channel)
38	S1 IN		—	For S1 signal input.
39	DC IN		1.9V*	Differential input vs S1 to S3 input.
40	S2 IN		—	For S2 signal input.

***Note)** External voltage applied

No.	Symbol	Equivalent circuit	Voltage	Description
41	MAT GAIN 2		1.6 to 5V*	Control of matrix amplifier 2.
			0 to 0.4V*	Preset mode (same gain as S2 channel)
42	S3 IN		—	For S3 signal input.
43	GND2		GND*	GND pin of YH GATE part.
44 45 46	CLP C S3 CLP C S2 CLP C S1		—	Capacitor connecting pin for S1, S2, and S3 signals clamp.
47	Vcc		5V*	Supply pin.
48	CODING		—	Mode control for color coding, effective only in complementary color mode (YL MIX>1.6V). Compatible codings are as follows.
			4.6 to 5V*	W, Ye, Cy mode
			2.5V	Ye, G, Cy mode
			0 to 0.4V*	W, Ye, G mode

***Note)** External voltage applied

Electrical Characteristics

Vcc=5V, Ta=25°C

No.	Item		Symbol	Input level (mV) S1	S2	S3	Pin conditions that differ from Electrical test circuit		Conditions formula of typical value	Test pin	Min.	Typ.	Max.	Unit	*	Test explanation, Remarks
1	Consumption current		Icc							47	20	33	46	mA		
2	White balance amplifier output level	Primary color mode G level	GM1		500					22	300	400	500	mV		Test of matching between channel and output level when the output signal is set to Pin 22: G out Pin 14: R out Pin 11: B out by means of the output switch SW.
3		Primary color mode R.G matching	RM1	500					14 Pin OUT/GM1	14	−2.2	0	2.2	dB		
4		Primary color mode B.G matching	BM1			500			11 Pin OUT/GM1	11	−2.2	0	2.2	dB		
5		W.Ye.G mode G level	GM2			250	YL MIX=OPEN CODING=0V			22	300	400	500	mV		
6		W.Ye.G mode R.G matching	RM2	250					14 Pin OUT/GM2	14	−2.2	0	2.2	dB		
7		W.Ye.G mode B.G matching	BM2		250				11 Pin OUT/GM2	11	−2.2	0	2.2	dB		
8		Ye.G.Cy mode G level	GM3			250	YL MIX=OPEN			22	300	400	500	mV		
9		Ye.G.Cy mode B.G matching	BM3	250					11 Pin OUT/GM3	11	−2.2	0	2.2	dB		
10		Ye.G.Cy mode R.G matching	RM3		250				14 Pin OUT/GM3	14	−2.2	0	2.2	dB		
11		W.Ye.Cy mode R level	RM4		250		YL MIX=OPEN CODING=5V			14	300	400	500	mV		
12		W.Ye.Cy mode B.R matching	BM4		250				11 Pin OUT/RM4	11	−2.2	0	2.2	dB		
13		W.Ye.Cy mode G1.R matching	GM4	250					22 Pin OUT/RM4	22	−2.2	0	2.2	dB		
14		W.Ye.Cy mode G2.R matching	GM5			250			22 Pin OUT/RM4	22	−2.2	0	2.2	dB		
15	MAT GAIN1	MIN GAIN	M1 MIN	250			YL MIX =OPEN CODING =0V	MAT GAIN1 =1.6V	14 Pin OUT/ RM2 14 Pin OUT	14			−1.4	dB		Ratio with output level when MAT GAIN1, 2 in preset mode at MAT GAIN 1 and 2 variable range test.
16		MAX GAIN	M1 MAX	250				MAT GAIN1 =5V	14 Pin OUT/ RM2 14 Pin OUT	14	2.5			dB		
17	MAT GAIN2	MIN GAIN	M2 MIN			250		MAT GAIN2 =1.6V	22 Pin OUT/GM2	22			−1.4	dB		
18		MAX GAIN	M2 MAX			250		MAT GAIN2 =5V	22 Pin OUT/GM2	22	2.5			dB		

V_{CC}=5V, Ta=25°C

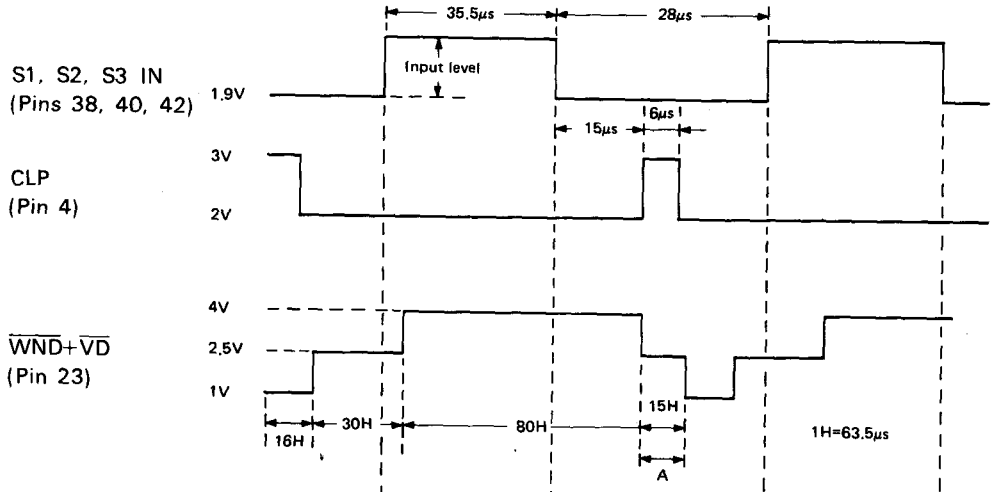
No.		Item	Symbol	Input level (mV) S1	S2	S3	Pin conditions that differ from Electrical test circuit	Conditions formula of typical value	Test pin	Min.	Typ.	Max.	Unit	Test explanation, Remarks
19	R GAIN	MIN GAIN	RGA MIN	500			R GAIN=5V	14 Pin OUT/RM1 14 Pin OUT	14			−1.4	dB	Ratio with output level when R, B GAIN in preset mode at R, B GAIN variable range test.
20		MAX GAIN	RGA MAX	167			R GAIN=1.6V	3×(14 Pin OUT/RM1 14 Pin OUT)	14	9.0			dB	
21	B GAIN	MIN GAIN	BGA MIN			500	B GAIN=5V	11 Pin OUT/BM1 11 Pin OUT	11			−1.4	dB	
22		MAX GAIN	BGA MAX			167	B GAIN=1.6V	3×(11 Pin OUT/BM1 11 Pin OUT)	11	9.0			dB	
23	R CONT	GAIN Linearity 0.4 Times	RC04	1250			R CONT=2.5V	14 Pin OUT/RM1 14 Pin OUT	14	−0.8	0	0.8	dB	Test of linearity of control voltage vs 1/GAIN for R, B CONT refer to diagram 3.
24		GAIN Linearity 2.5 Times	RC025	200			R CONT=0.4V	14 Pin OUT/RM1 14 Pin OUT	14	−0.8	0	0.8	dB	
25	B CONT	GAIN Linearity 0.4 Times	BC04			1250	B CONT=2.5V	11 Pin OUT/BM1 11 Pin OUT	11	−0.8	0	0.8	dB	
26		GAIN Linearity 2.5 Times	BC025			200	B CONT=0.4V	11 Pin OUT/BM1 11 Pin OUT	11	−0.8	0	0.8	dB	
27	C LEVEL	MIN GAIN	CG MIN		1000		C LEVEL=1.6V	0.5×(22 Pin OUT/GM1)	22			−4.8	dB	Ratio with output level when C LEVEL in preset mode at C LEVEL variable range test.
28		MAX GAIN	CG MAX		200		C LEVEL=5V	2.5×(22 Pin OUT/GM1)	22	4.8			dB	
29	Comparator output voltage	R COMP LO LEVEL	R COMP1				Input signal where with $\overline{WND}+\overline{VD}$ pulse ON we have R>G and B>G.		25			1.0	V	Test concerns DC output level equipment to the A portion of the $\overline{WND}+\overline{VD}$ input waveform diagram.
30		B COMP LO LEVEL	B COMP1						24			1.0	V	
31		R COMP HI LEVEL	R COMP2				Input signal where with $\overline{WND}+\overline{VD}$ pulse ON we have R<G and B<G.		25	4.0			V	
32		B COMP HI LEVEL	B COMP2						24	4.0			V	
33		Y PED Amount	YP1		500		Y PED=5V	Y PED=0V When 8 Pin OUT−8 Pin OUT	8	100			mV	Amount of dark slice in Y S2 channel.
34		C PED Amount	CPG		500		C PED=5V	GM1−22 Pin OUT	22	80			mV	Amount of dark slice in chroma type G channel.
35	Cγ reference curve	500 mV at input	CγG1		500		OFFSET CONT= OPEN		22	650	800	950	mV	
36		200 mV at input	CγG2		200			22 Pin OUT/CγG1	22	0.48	0.58	0.68		γ I/O characteristics where CγG2 is the ratio with CγG1.

V_{CC}=5V, Ta=25°C

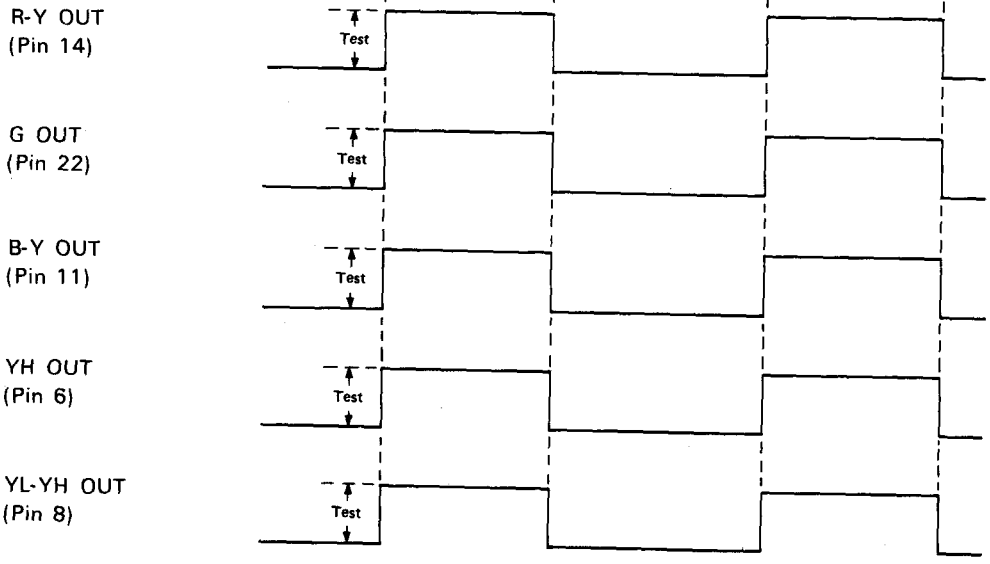
No.	Item	Symbol	Input level (mV) S1	S2	S3	Pin conditions that differ from Electrical test circuit		Conditions formula of typical value	Test pin	Min.	Typ.	Max.	Unit	Test explanation, Remarks
37	YH-Y reference curve 500 mV at input	YHγ1		500		OFFSET CONT =OPEN		6 Pin OUT/YHγ1	6	780	1015	1250	mV	Ratio between YHγ2 and YHγ1 at γ I/O characteristics
38	200 mV at input	YHγ2		200					6	0.48	0.58	0.68	-	
39	YH OUT DC	YHDC				OFFSET CONT =OPEN			6	2.1	2.5	2.9	V	Output pin DC level
40	YL-YH OUT DC	YLHDC							8	2.6	3.0	3.4	V	
41	R-Y GAIN MIN GAIN	RY2	200			OFFSET CONT= OPEN	R-Y GAIN =1.6V	14 Pin OUT/R-Y GAIN=0V When 14 Pin OUT	14			-1.8	dB	Ratio between R-Y, B-Y GAIN variable range test.
42	MAX GAIN	RY3	200				R-Y GAIN =5V	14 Pin OUT/R-Y GAIN=0V When 14 Pin OUT	14	7			dB	
43	B-Y GAIN MIN GAIN	BY2			200	OFFSET CONT= OPEN	B-Y GAIN =1.6V	11 Pin OUT/B-Y GAIN=0V When 11 Pin OUT	11			-1.8	dB	
44	MAX GAIN	BY3			200		B-Y GAIN =5V	11 Pin OUT/B-Y GAIN=0V When 11 Pin OUT	11	7			dB	
45	R-Y HUE MAX	RHU1	500			OFFSET CONT= OPEN	B-Y HUE =5V	$-\tan^{-1}\left\{\frac{11\text{ Pin OUT}}{14\text{ Pin OUT}}\right\}$	11	22			°	Angle with R-Y axis taken as reference at rotation angle variable range test using R-Y HUE.
46	MIN	RHU2	500				B-Y HUE =1.6V	$-\tan^{-1}\left\{\frac{11\text{ Pin OUT}}{14\text{ Pin OUT}}\right\}$	11			-22	°	
47	B-Y HUE MAX	BHU1			500	OFFSET CONT= OPEN	R-Y HUE =5V	$\tan^{-1}\left\{\frac{11\text{ Pin OUT}}{14\text{ Pin OUT}}\right\}$	14	22			°	Angle with B-Y axis taken as reference at rotation angle variable range test using R-Y HUE.
48	MIN	BHU2			500		R-Y HUE =1.6V	$\tan^{-1}\left\{\frac{11\text{ Pin OUT}}{14\text{ Pin OUT}}\right\}$	14			-22	°	
49	R-Y OUT DC	RYDC				OFFSET CONT= OPEN	R-Y GAIN=5V		14	2.6	3.0	3.4	V	Output pin DC level.
50	B-Y OUT DC	BYDC					B-Y GAIN=5V		11	2.6	3.0	3.4	V	

Test Circuit I/O Waveform

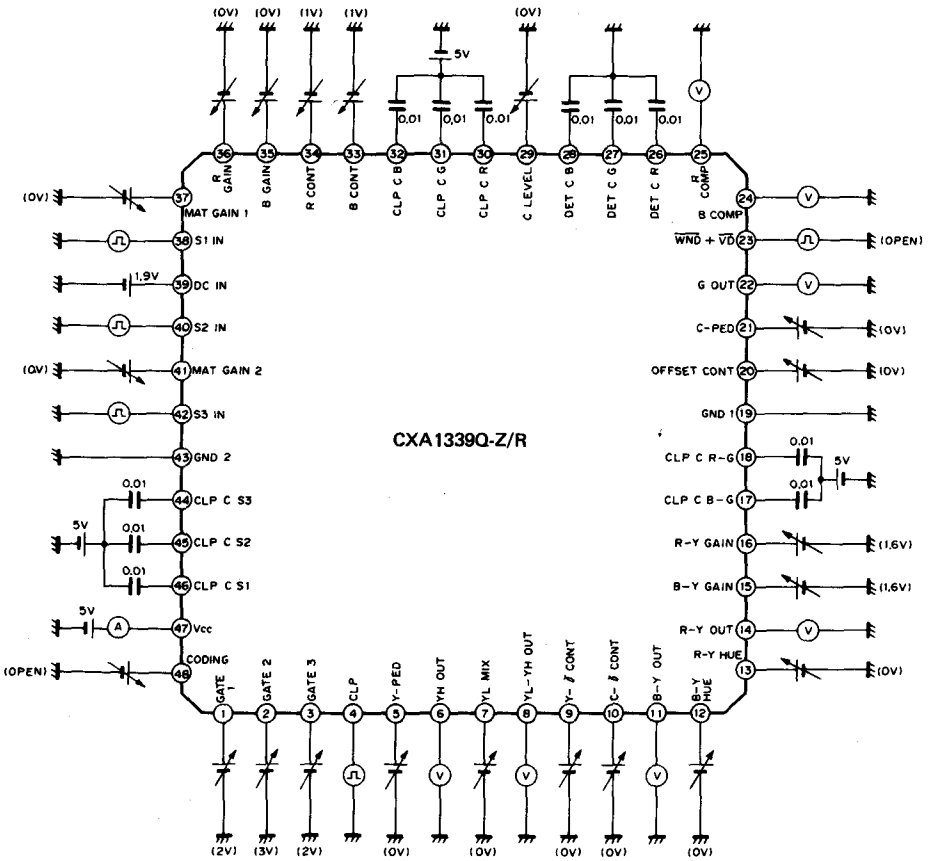
Input waveform



Output waveform



Electrical Characteristics Test Circuit



Note) 1. Capacitor capacity unit μF.
2. In brackets voltage in places not specifies in the descriptions of Electrical characteristics.
3. V indicates test pin. (AC, DC voltage test)

Operation

Color coding

Compatible with the combination of the 4 following color filters. Set through the applicatin of voltage to CODING (Pin 48) and YL MIX (Pin 7). The necessary conditions for the selection of each coding are as follows.

Filter color coding	CODING (Pin 48)	YL MIX (Pin 7)
R.G.B	–	GND
W.Ye.Cy	Vcc	Higher than 1.6V
Ye.G.Cy	OPEN	Higher than 1.6V
W.Ye.G	GND	Higher than 1.6V

W:White, Ye:Yellow, Cy:Cyan

Note) R.G.B modes are selected with YL MIX only and have no relation with the CODING voltage.

Preset mode

By grounding a pin that has the preset function, the control setting by that pin stands at a specified value. This is indicated in the following table.

No.	Symbol	Preset mode
5	Y-PED	Becomes Y-PED OFF.
7	YL MIX	Color coding at R.G.B, YL YLC 100%, MAT GAIN 1 and 2 reaches same gain as S2 channel.
9	Y-γ CONT	Becomes typical Y-γ curve. (See Fig. 11)
10	C-γ CONT	Becomes typical C-γ curve. (See Fig. 10)
12	B-Y HUE	Becomes B-Y HUE OFF.
13	R-Y HUE	Becomes R-Y HUE OFF.
15	B-Y GAIN	B-Y OUT (Pin 11) output becomes B-G.
16	R-Y GAIN	R-Y OUT (Pin 14) output becomes R-G.
20	OFFSET CONT	Pins 6, 8, 11, 14 and 22 of output SWs are switched.
21	C-PED	Becomes C-PED OFF.
29	C LEVEL	C LEVEL AMP gain becomes 0 dB at R.G.B modes. In other modes 6 dB.
35	B GAIN	B GAIN AMP gain becomes same as G channel.
36	R GAIN	R GAIN AMP gain becomes same as G channel.
37	MAT GAIN 1	MAT GAIN 1's gain becomes same as S2 channel.
41	MAT GAIN 2	MAT GAIN 2's gain becomes same as S2 channel.

Output switching SW

By grounding OFFSET CONT (pin 20) output SW of pins, 6, 8, 11, 14 and 22 and output signal becomes as follows.

No.	OFFSET CONT>1.6V output	OFFSET CONT<0.4V output
6	YH	YL
8	YL-YH	YTP (signal that has passed through PED of Y S2 channel)
11	B-Y	B (B signal before entry γ)
14	R-Y	R (R signal before entry γ)
22	G signal with γ applied	G (G signal before entry γ)

White balance control

1) Gain control

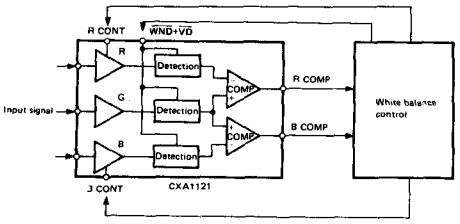
There are 2 types, R GAIN (Pin 36) and B GAIN (Pin 35) for precontrol and R CONT (Pin 34) and B CONT (Pin 33).

Also for R CONT, B CONT. The control voltage and the white balance amplifier gain reverse figures have a ratio relation. It is ideal as the control pin for auto white balance.

2) One push white balance (close loop white balance)

- An example is shown at right

R.G.B signals that have passed through white balance are PEAK detected and output as comparison signals R and G, B and G by means of the comparator. From the comparison signal, GAIN control is executed and by requesting R CONT B CONT to become R=B=G, white balance is completed.



- Detection part operation

$\overline{WND}+\overline{VD}$ (Pin 23) the operation of the detection part by means of external voltage application is as follows.

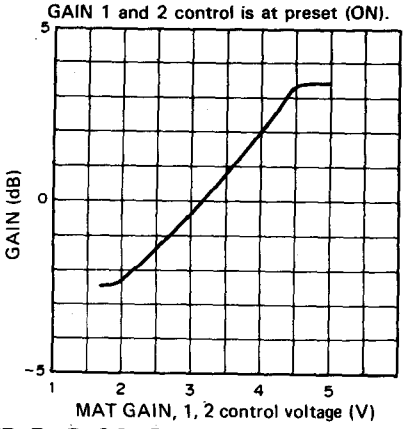
$\overline{WDN}+\overline{VD}$>4.1V: Detects input signal.

$\overline{WND}+\overline{VD}$=2.5V: Just before getting set to 2.5V, detection data is held.

$\overline{WND}+\overline{VD}$<0.9V: Detection data is reset.

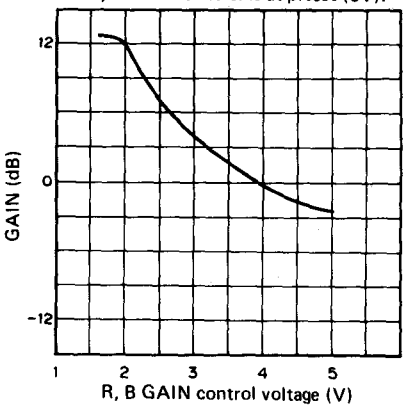
MAT GAIN 1, 2 control characteristics

Output is assumed to be 0 dB when MAT GAIN 1 and 2 control is at preset (ON).



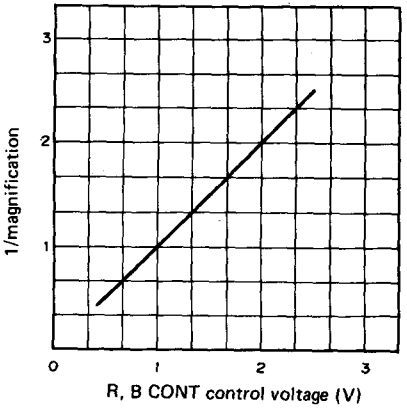
WB R, B GAIN control characteristics

Output is assumed to be 0dB when R, B GAIN control is at preset (0V).



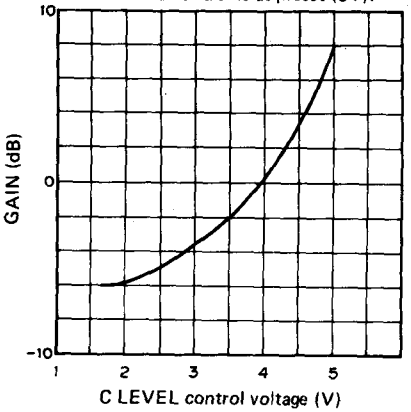
WB R, B CONT control characteristics

Output is assumed to be 1 when, R, B CONT control is at 1V.



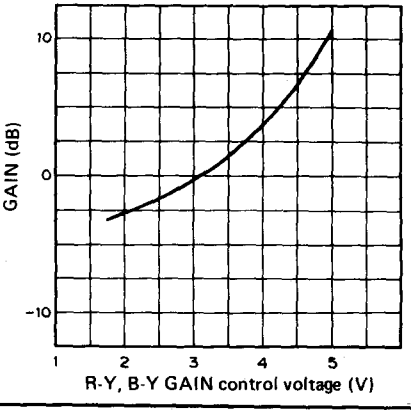
C LEVEL control characteristics

Output is assumed to be 0dB when C LEVEL control is at preset (0V).

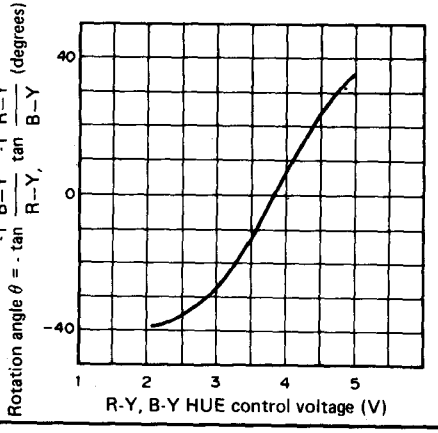


R-Y, B-Y GAIN control characteristics

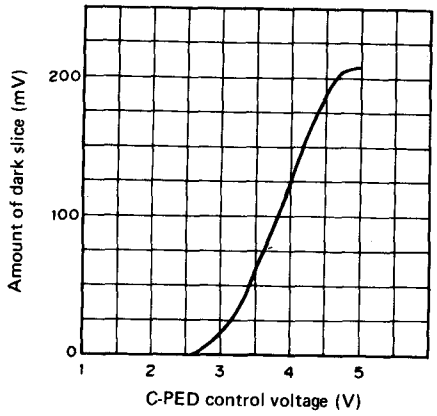
Output is assumed to be 0dB when R-Y, B-Y GAIN control is at preset (0V).



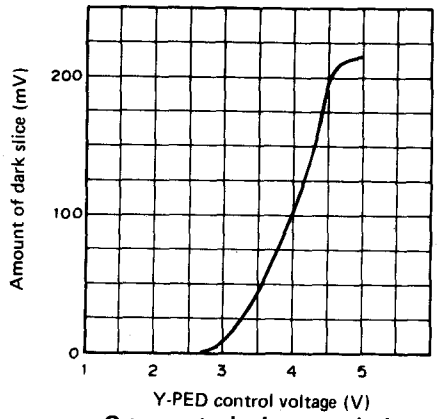
R-Y, B-Y HUE control characteristics



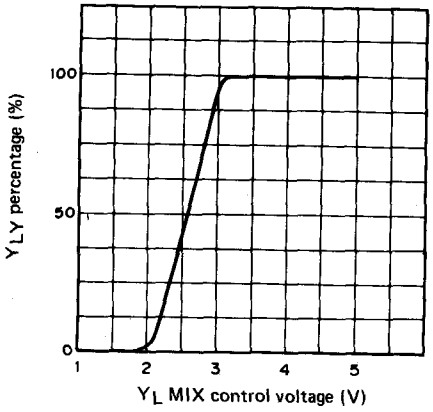
C-PED control characteristics



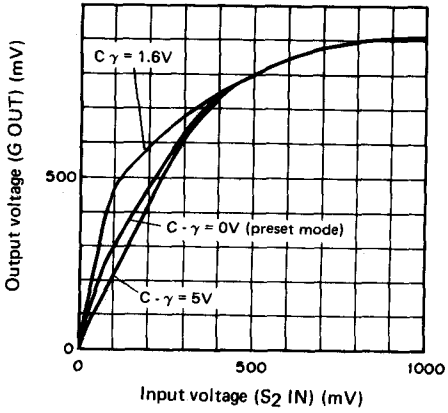
Y-PED control characteristics



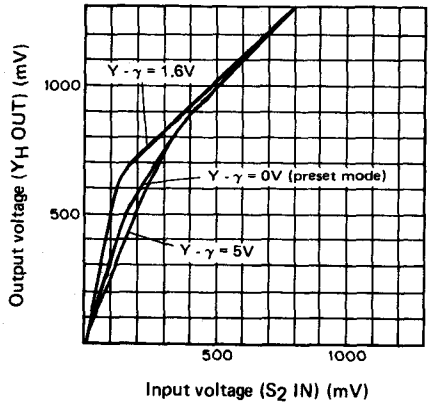
YL MIX control characteristics



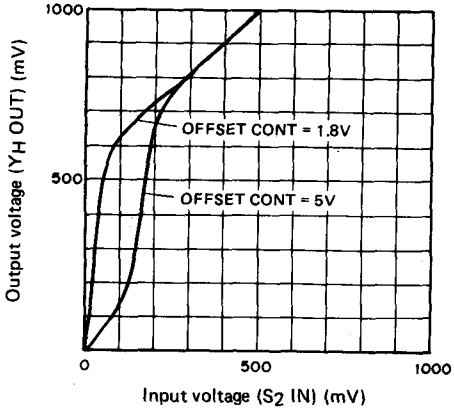
C-γ control characteristics



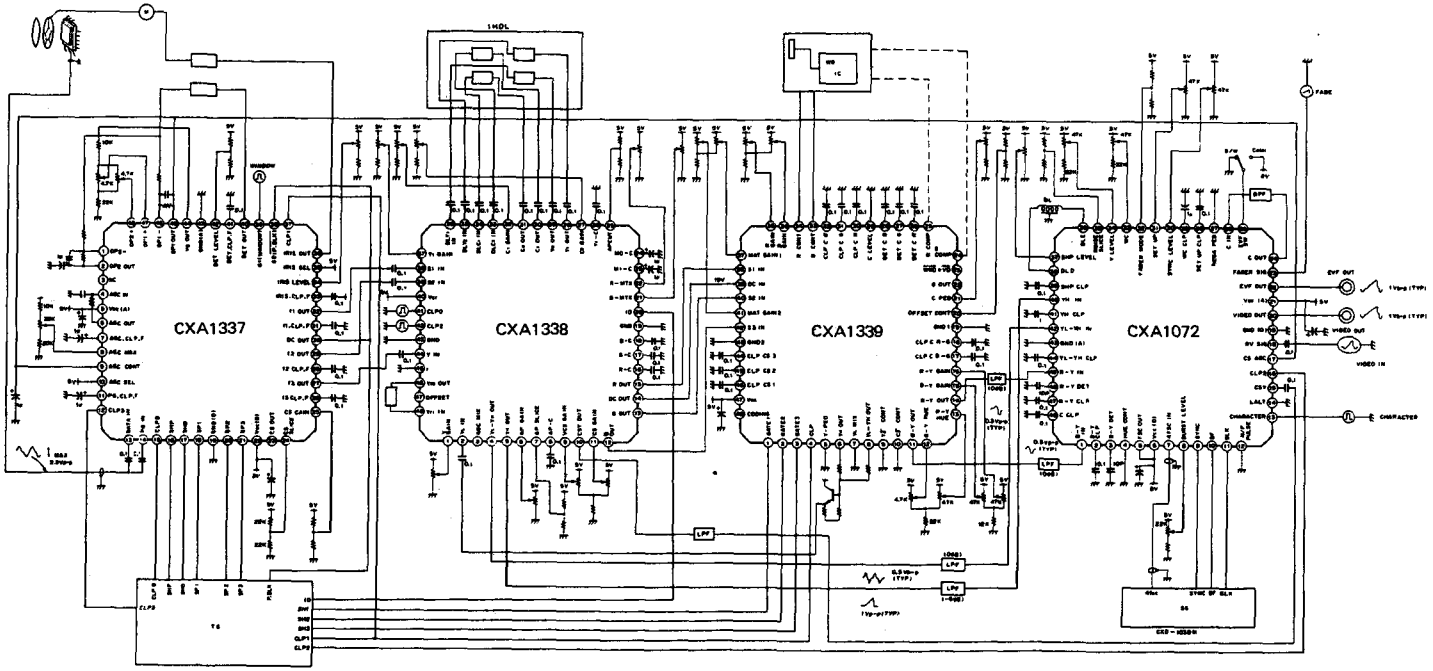
YH-γ OFFSET control characteristics



YH-γ control characteristics



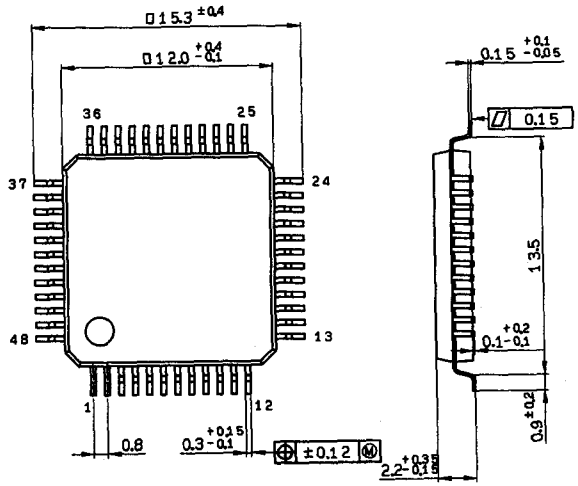
768H Complementary Color Mosaic CCD Camera System Diagram



- It is recommended to set the resistance with no value indicated to 50 kΩ and below between Vcc–GND.
- Unspecified capacity unit is μF.

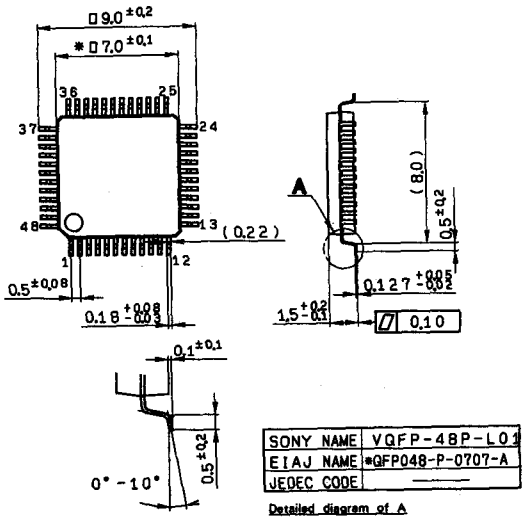
Package Outline Unit : mm

CXA1339Q-Z 48 pin QFP (Plastic)



SONY NAME	QFP-48P-L04
EIAJ NAME	*QFP048-P-1212-B
JEDEC CODE	———

CXA1339R 48 pin VQFP (Plastic)



SONY NAME	VQFP-48P-L01
EIAJ NAME	*QFP048-P-0707-A
JEDEC CODE	———

Detailed diagram of A

Note) Dimensions marked with * do not include resin residue.

SONY

CXA1072Q-Z/R

Camera Signal Processing

Description

CXA1072Q-Z and CXA1072R are encoder ICs for CCD color cameras.
Luminance and color difference signals are input to be output as composite video signals.
Combined use with system for CCD color cameras.

Features

- Built-in auto carrier balance (carrier balance adjustment unnecessary).
- Compatible with both NTSC/PAL.
- Compatible with Negative/Positive.
- Low consumption (200 mW) (150 mW in B/W mode)
- Low noise

Structure

Bipolar silicon monolithic IC.

Application

CCD color camera

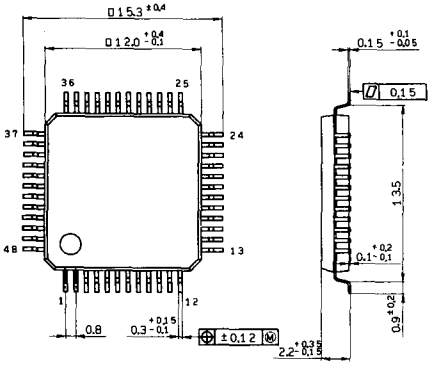
Function

- Set-up level control
- White clip level control
- White fader/black fader
- View finder output
- Character signal (superimpose)
- Sub carrier modulation
- Burst level control
- PAL mode
- Sub carrier output
- Sharpness level control
- Negative mode
- Return video input
- Auto carrier balance
- HUE control
- Sync level control
- Chroma suppress Y, chroma suppress AGC

Package Outline

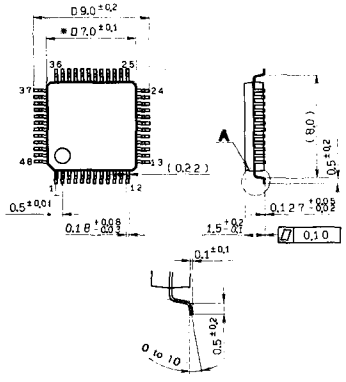
Unit: mm

48 pin QFP (Plastic)



QFP-48P-L04

48 pin VQFP (Plastic)



VQFP-48P-L01

Absolute Maximum Ratings (Ta=25°C)

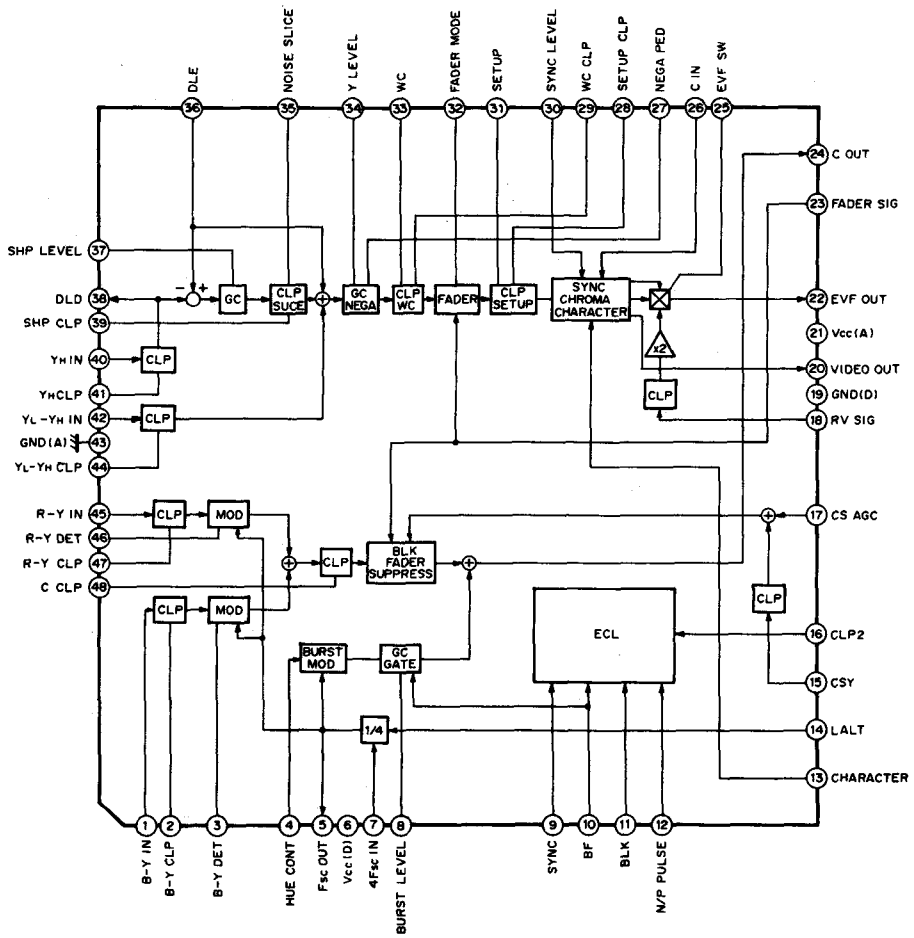
• Supply voltage	Vcc	7	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	600	mW

Recommended Operating Condition

• Supply voltage	Vcc	4.75 to 5.25	V

70813A-ST

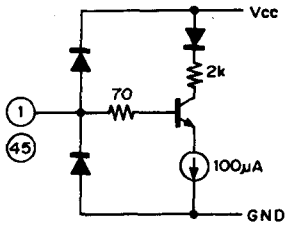
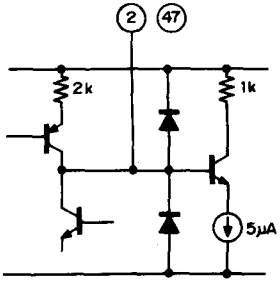
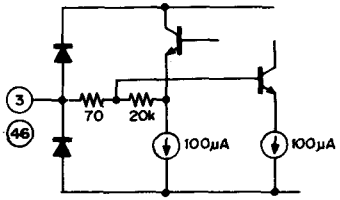
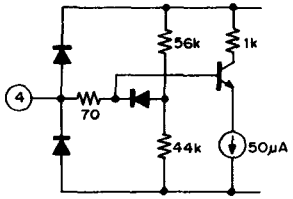
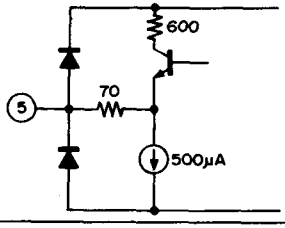
Block Diagram and Pin Configuration

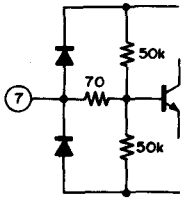
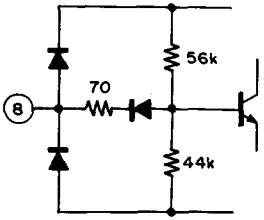
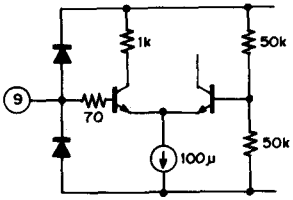
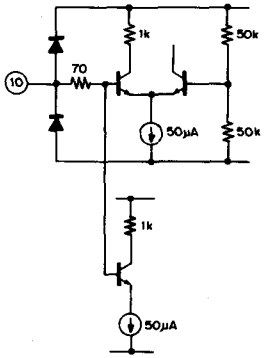


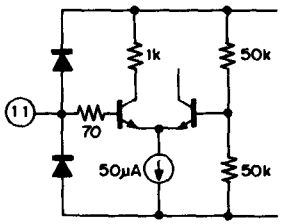
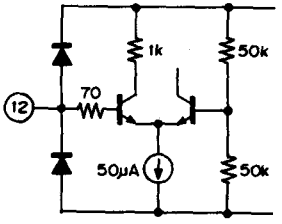
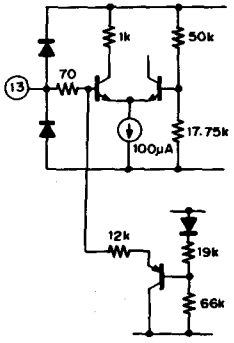
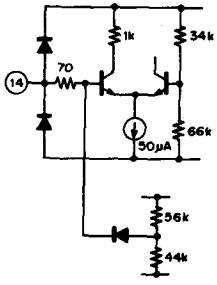
Abbreviations

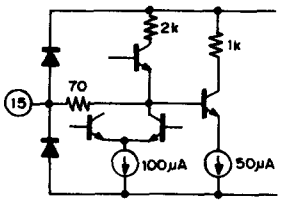
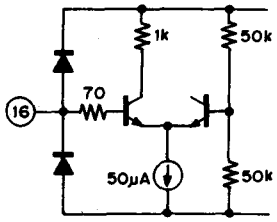
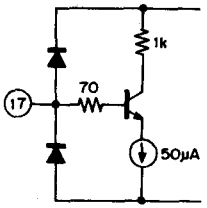
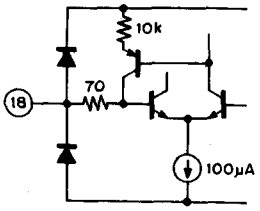
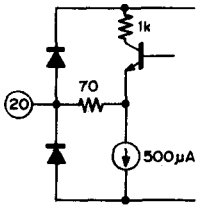
CLP	Clamp	RV	Return Video
DET	Detecter	EVF	Electric View Finder
CONT	Control	CIN	Chroma Input
BF	Burst Frag	PED	Pedestal
BLK	Blanking	WC	White Clip
N/P	Nega/Posi	DLD	Delay Line Drive
LALT	Line Alternate	DLE	Delay Line End
CSY	Chroma Suppres Y	SHP	Sharpness

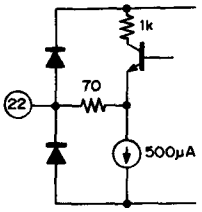
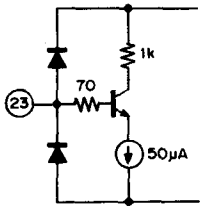
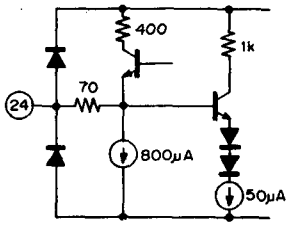
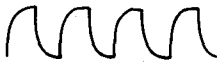
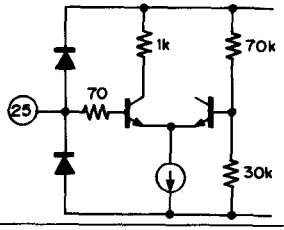
Pin Description and Equivalent Circuit

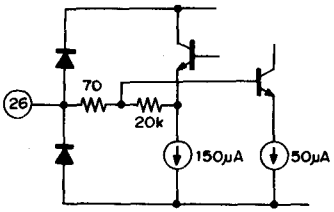
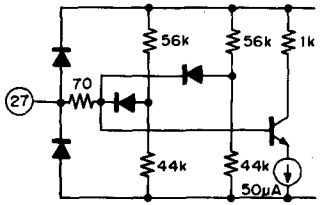
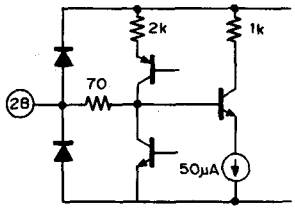
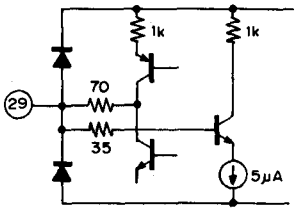
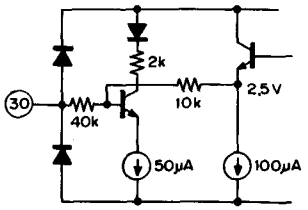
No.	Symbol	Voltage	Equivalent circuit	Description
1 45	B-Y IN R-Y IN	3.0V (External) 3.0V (External)		Color difference signal input pin.
2 47	B-Y CLP R-Y CLP	3.0V 3.0V		Connecting pin to the color signal input CLP capacitor.
3 46	B-Y DET R-Y DET	3.5V 3.5V		Connecting pin to the capacitor for auto carrier balance.
4	HUE CONT	0V (External)		HUE control pin 0V..... HUE OFF 2.5V to 5V..... Control
5	FSC OUT	Low-2.9V Hi-3.6V		Sub carrier output pin

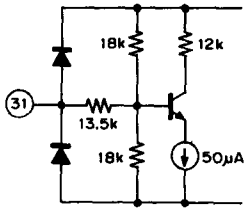
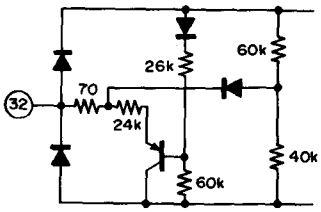
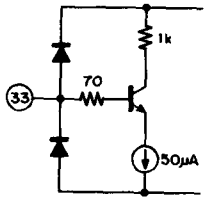
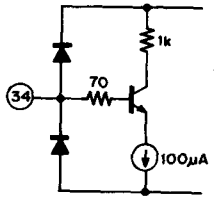
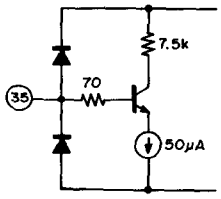
No.	Symbol	Voltage	Equivalent circuit	Description
6	Vcc (D)	5V		Digital circuit supply.
7	4FSC IN	2.5V (When open)		Pin that inputs signals with a frequency 4 times that of the sub carrier
8	BURST LEVEL	3.7V (External)		Burst level control pin Ground when using for analog burst.
9	SYNC	Pulse input		Sync pulse input pin ⊓ Negative polarity Low: 0 to 2V Hi: 3 to 5V
10	BF	Pulse input		Burst pulse input pin ⊓ Negative polarity Input 2.5 to 3.5V signal during analog burst usage. ⌐¬ 3.5V 2.5V

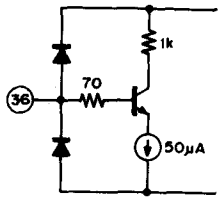
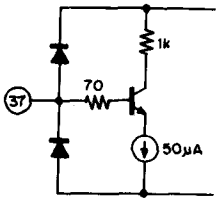
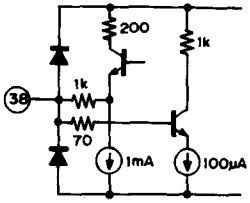
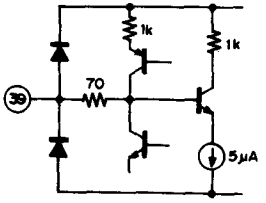
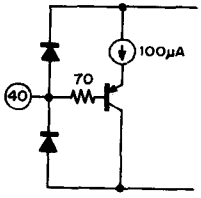
No.	Symbol	Voltage	Equivalent circuit	Description
11	BLK	Pulse input		Blanking pulse input pin Negative polarity Low: 0 to 2V Hi: 3 to 5V
12	N/P PULSE	Pulse input		Pulse input pin in negative mode. At high level negative pedestal. Low: 0 to 2V Hi: 3 to 5V
13	CHARACTER	Pulse input		Character pulse input pin 2.5V 2.0 Input 2.5V to 3.5V signal during analog burst usage.
14	LALT	Pulse input		Line alternate pulse input pin NTSC mode: GND PAL mode: 2H period pulse Low: 2.2 to 2.8V Hi: 3.8 to 5V

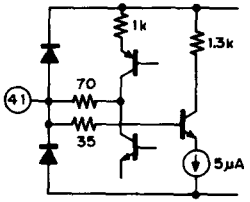
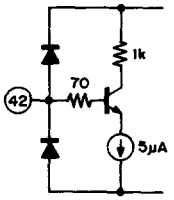
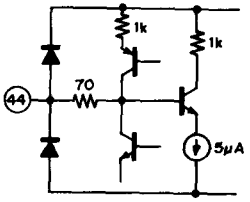
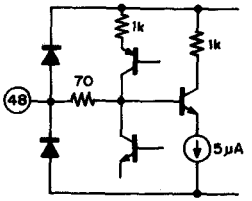
No.	Symbol	Voltage	Equivalent circuit	Description
15	CSY	2.85V		Chroma suppress Y signal input pin
16	CLP2	Pulse input		Clamp pulse input pin ⊓ Positive polarity Low: 0 to 2V Hi: 3 to 5V
17	CS AGC	GND (External)		Chroma suppress AGC signal. Input pin
18	RV SIG	2V		Return video signal input pin
19	GND (D)	0V		
20	VIDEO OUT	2.1V		Video output pin

No.	Symbol	Voltage	Equivalent circuit	Description
21	Vcc (A)	5V		Analog circuit supply
22	EVF OUT	2.1V		View finder output pin
23	FADER SIG	GND (External)		Fader signal input pin
24	C OUT	2.6V		Chroma signal ouput pin  *Short waveform is output. In B/W mode by turning the pin to Vcc power saving is possible.*
25	EVF SW	5V (External)		EVF output select pin 0V..... Return Video 1.5 to 3.5V..... Color mode 5V..... B/W mode

No.	Symbol	Voltage	Equivalent circuit	Description
26	C IN	2.5V		Chroma signal mixed input pin
27	NEGA PED	0V (External)		NEGA/POSI modes select pin 0V..... POSI 2 to 5V..... Nega pedestal Level control
28	SETUP CLP	2.7V		SETUP CLP capacitor connecting pin
29	WC CLP	2.8V		WC CLP capacitor connecting pin
30	SYNC LEVEL	2.5V		Sync level control pin

No.	Symbol	Voltage	Equivalent circuit	Description
31	SETUP	2.5V (External)		Set-up level control pin Video output pin
32	FADER MODE	0V (Exteranl)		Fader mode select pin 0 to 2V . . . . . Black fader 2 to 3.7V . . . . . White fader White level control
33	WC	3.5V (External)		White clip level control pin
34	Y LEVEL	3.2V (External)		White signal level control pin
35	NOISE SLICE	3V (External)		Noise slice level control pin

No.	Symbol	Voltage	Equivalent circuit	Description
36	DLE	3.4V		Delay line connecting pin for sharpness signal formation.
37	SHP LEVEL	3.5V		Sharpness level control pin Chroma signal mixed input pin
38	DLD	3.4V		Delay line connecting pin for sharpness signal formation.
39	SHP CLP	2.5V		Sharpness clamp capacitor connecting pin
40	Y_H IN	1.2V (External)		Y_H signal input pin

No.	Symbol	Voltage	Equivalent circuit	Description
41	Y_H CLP	2.1V		Y_H clamp capacitor connecting pin
42	Y_L-Y_H IN	3.0V (External)		Y_L-Y_H signal input pin
43	GND (A)	0V		
44	Y_L-Y_H CLP	3V		Y_L-Y_H clamp capacitor connecting pin
48	CHROMA CLP	3.9V		CHROMA clamp capacitor connecting pin

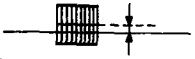
Electrical Characteristics

V=5V, Ta=25°C

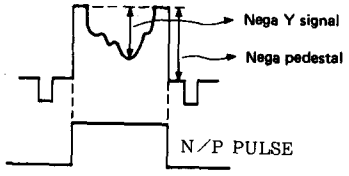
No.	Item	Symbol	Condition	Test point	Min.	Typ.	Max.	Unit
1	Supply current (color)	Icc	Current that flows into Vcc1, Vcc2	Vcc1, Vcc2	31	40	53	mA
2	Supply current (B/W)	Icc (B/W)	Current that flows into Vcc1,Vcc2	Vcc1, Vcc2	22	30	40	mA
3	Y_H level MIN.	Y MIN	Y LEVEL=5V, Y_H IN=500 mV	VIDEO OUT	230	320	410	mV
4	Y_H level MAX.	Y MAX	Y LEVEL=2V, Y_H IN=250 mV	VIDEO OUT	410	770	1240	mV
5	Y_H level MAX/MIN Y_H CLP 2.1V	Y CONT	No.3 and No.4 ratio		8	13	17	dB
6	Y_L-Y_H/Y_H gain difference	Y_L-Y_H	Y_L-Y_H IN=250 mV (I/O gain difference with Y_H IN=500 mV)	VIDEO OUT	−1.1	0	1.1	dB
7	EVF OUT/VIDEO OUT gain difference	EVF	Y_H IN=500 mV (I/O gain difference with the results obtained from VIDEO OUT test)	EVF OUT	−1.1	0	1.1	dB
8	White clip MAX	WC MAX	Y_H IN=500 mV Y LEVEL=2V, WC=5V	VIDEO OUT	870	1140	1430	mV
9	White clip MIN	WC MIN	Y_H IN=500 mV Y LEVEL=2V, WC=2V	VIDEO OUT	440	540	660	mV
10*1	Nega pedestal MAX	NPED MAX	NEGA PULSE input, NEGA PED=5V WC=5V, BLK=5V	VIDEO OUT	880	1030	1220	mV
11	Nega pedestal MIN	NPED MIN	NEGA PULSE input, NEGA PED=2V W/C=5V, BLK=5V	VIDEO OUT	240	330	460	mV
12	Nega Y_H/Posi Y_H gain difference	NEGA Y	NEGA PULSE input, NEGA PED=3.4V Y_H IN=250 mV (I/O gain difference with IN=500 mV in posi mode)	VIDEO OUT	−1.1	0	1.1	dB

No.	Item	Symbol	Condition	Test point	Min.	Typ.	Max.	Unit
13	Sharpness upper side level	SHP UP	Y_H IN=−20 mV Y_L-Y_H IN=250 mV SET UP=5V, NOISE SLICE=3.0V SHP LEVEL=3.5V SW2 ON	VIDEO OUT	30	84	140	mV
14	Sharpness up down ratio	SHP LOW	Y_H IN=20 mV Y_L-Y_H IN=250 mV SET UP=5V, NOISE SLICE=3.0V SHP LEVEL=3.5V, SW2 ON (Ratio of sharpness upper side level vs. sharpness lower side level)	VIDEO OUT	1.5	2.0	2.5	V/V
15	Nega sharpness upper side level	N SHP UP	Y_H IN=20 mV NEGA PULSE input SET UP=5V, NOISE SLICE=3.0V SHP LEVEL=3.5V, SW2 ON	VIDEO OUT	30	84	140	mV
16	Nega sharpness up down ratio	N SHP LOW	Y_H In=−20 mV NEGA PULSE input SET UP=5V, NOISE SLICE=3.0V SHP LEVEL=3.5V SW2 ON	VIDEO OUT	1.5	2.0	2.7	V/V
17	White fader	W FADE	BLK input, FADER SIG=3.5V FADER MODE=2.5V	VIDEO OUT	260	350	440	mV
18	SETUP MAX	SETUP MAX	BLK input, FADER SIG=3.5V SET UP=5V	VIDEO OUT	165	140	185	mV
19	SYNC MAX	SYNC MAX	SYNC input, BLK=0V FADER SIG=3.5V SYNC LEVEL=5V	VIDEO OUT	360	430	520	mV
20	SYNC MIN	SYNC MIN	SYNC input, BLK=0V FADER SIG=3.5V SYNC LEVEL=0V	VIDEO OUT	100	170	250	mV

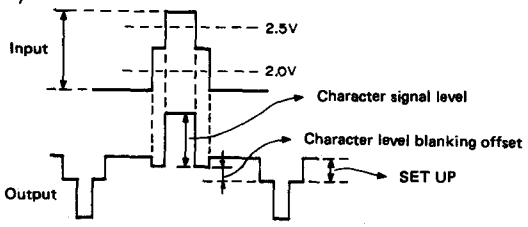
No.	Item	Symbol	Condition	Test point	Min.	Typ.	Max.	Unit
21	SYNC EVF (B/W)— V OUT Difference	SYNC (B/W)	SYNC input, BLK=0V FADER SIG=3.5V SYNC LEVEL=OPEN Ratio with B-Y level No.33	EVF OUT	−70	0	70	mV
22	SYNC EVF (Color)— V OUT Difference	SYNC (COL)	SYNC input, BLK=0V FADER SIG=3.5V, EVF SW=2.5V SYNC LEVEL=OPEN (Difference with the VIDEO OUT Sync under the same conditions)	EVF OUT	−70	0	70	mV
23	Character blanking level offset (V-OUT)	CHA OFF	BLK input, CHARACTER=2.25V	VIDEO OUT	3	100	170	mV
24	Character blanking level offset (EVF B/W)	CHA OFF (B/W)	BLK input, CHARACTER=2.25V	EVF OUT	3	100	170	mV
25	Character blanking level offset (EVF COL)	CHA OFF (COL)	BLK input, CHARACTER=2.25V EVF SW=2.5V	EVF OUT	20	100	190	mV
26*2	Character level (V-OUT)	CHA	BLK input, CHARACTER=3.2V	VIDEO OUT	475	520	595	mV
27	Character level (EVF B/W)	CHA (B/W)	BLK input, CHARACTER=3.2V (Ratio vs. VIDEO OUT character level)	EVF OUT	−1.1	0	1.1	dB
28	Character level (EVF COL)	CHA (COL)	BLK input, CHARACTER=3.2V EVF SW=2.5V (Ratio vs. VIDEO OUT character level)	EVF OUT	−1.1	0	1.1	dB

No.	Item	Condition	Test point	Min.	Typ.	Max.	Unit
29	Return video gain	EVF SW=0V RV SIG IN=350 mV	EVF OUT	4.5	6	7.5	dB
30	FSC OUT amplitude	SW4 ON	FSC OUT	610	710	810	mV
31	Carrier balance 3.58 MHz	B-Y IN, R-Y IN=2.1V and 3.9V	BPF OUT	—	1.3	3.5	mVp-p
32	Carrier balance 500 kHz	4FSC IN=2 MHz B-Y IN, R-Y IN=2.1V and 3.9V	BPF OUT	—	1.2	3.5	mVp-p
33	B-Y level	B-Y IN=300 mV	BPF OUT	400	470	550	mVp-p
34	R-Y level	R-Y IN=300 mV	BPF OUT	400	470	550	mVp-p
35	CHROMA TOTAL GAIN	B-Y IN=300 mV SW3 ON	VIDEO OUT	1.9		2.8	V/V
36	CHROMA GAIN EVF/ V-OUT ratio	B-Y IN=300 mV SW3 ON, EVF SW=2.5V	VIDEO OUT EVF OUT	−1.1	0	1.1	dB
37	CHROMA D-Range	B-Y IN=900 mV	BPF OUT	990	1130	1260	mVp-p
38	CS AGC MAX	B-Y IN=300 mV CS AGC=3.5V (Ratio with B-Y level No.33)	BPF OUT	40	50	60	%
39	BURST MAX	BF=0V, BLK=0V BURST LEVEL=5V	BPF OUT	310	390	480	mVp-p
40	BURST MIN	BF=0V, BLK=0V BURST LEVEL=2.5V	BPF OUT	88	110	132	mVp-p
41	BURST PAL Hi/Low	BF=0V, BLK=0V Ratio LALT=5 when LALT=2.5V	BPF OUT	−3	0	5	%
42	BURST linear MAX	BF=0V, BLK=0V BURST LEVEL=0V	BPF OUT	340	450	560	mVp-p
43	BURST level blanking offset	BF input, BLK=0V 	C OUT	−55	0	55	mV
44	CHROMA BLK level offset	BLK input, BF=5V	C OUT	−55	0	55	mV

*1)

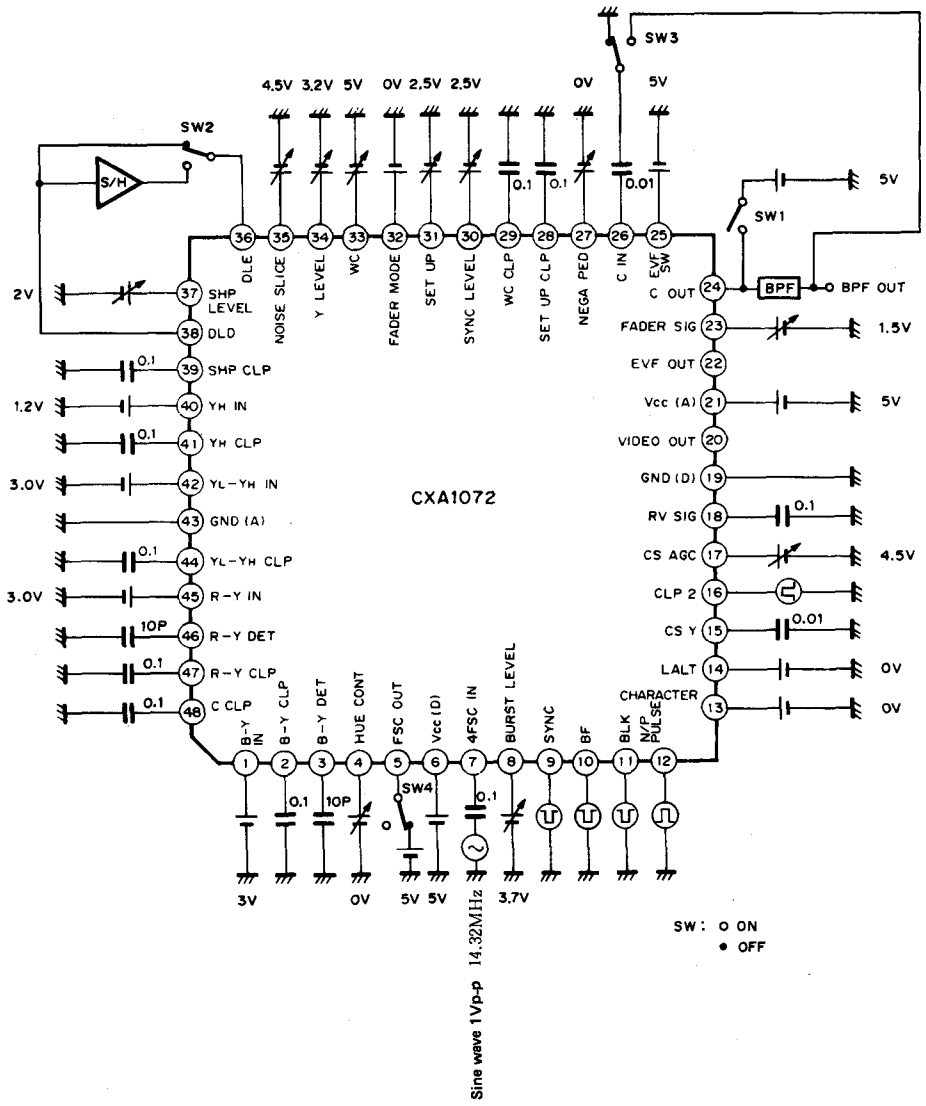


*2)



Test Circuit

(Typical Setting)



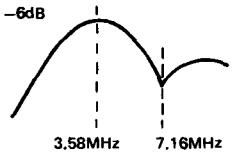
Note) Above conditions are given as the typical setting. The individual conditions of each item are indicated in the chart.

Test Conditions

1. BPF

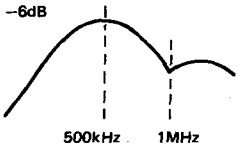
(1) 3.58 MHz BPF

The BPF where with an input of a 3.58 MHz sine wave the output becomes 1/2.



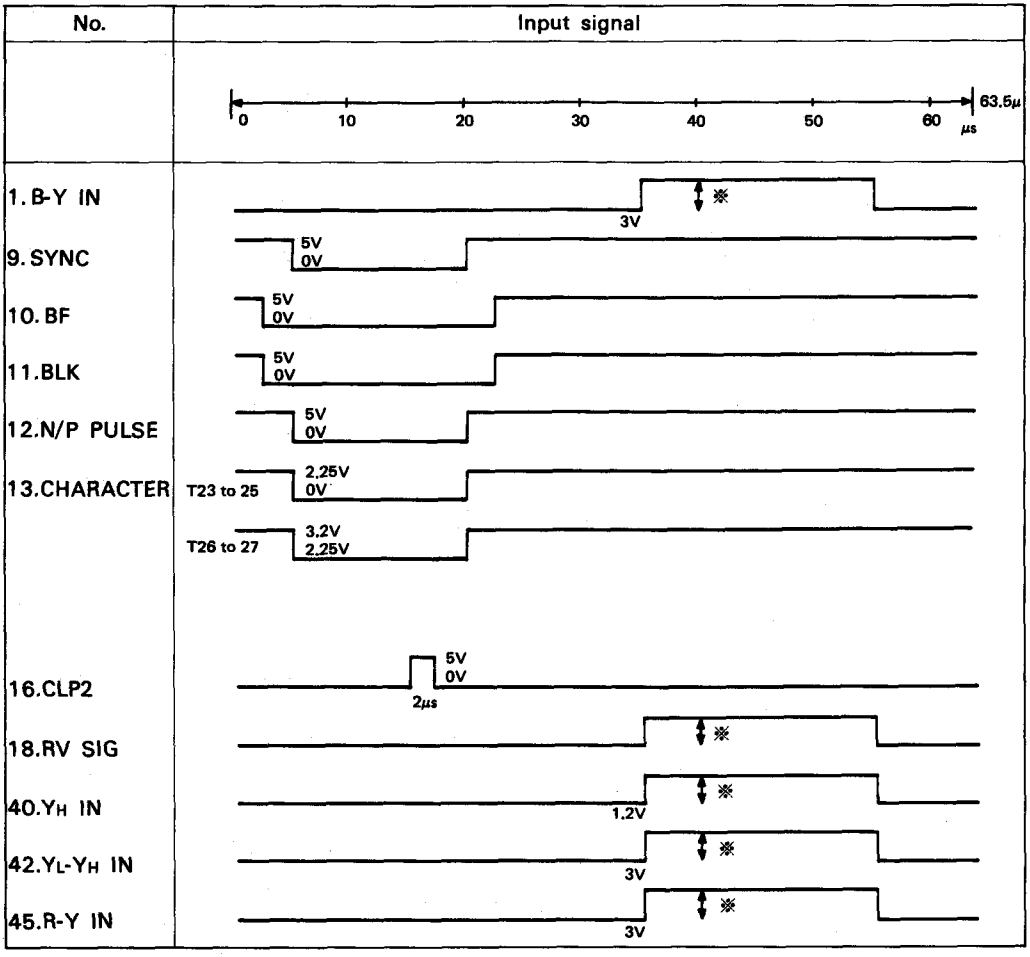
(2) 500 kHz BPF

The BPF where with an input of a 500 kHz sine wave the output becomes 1/2.



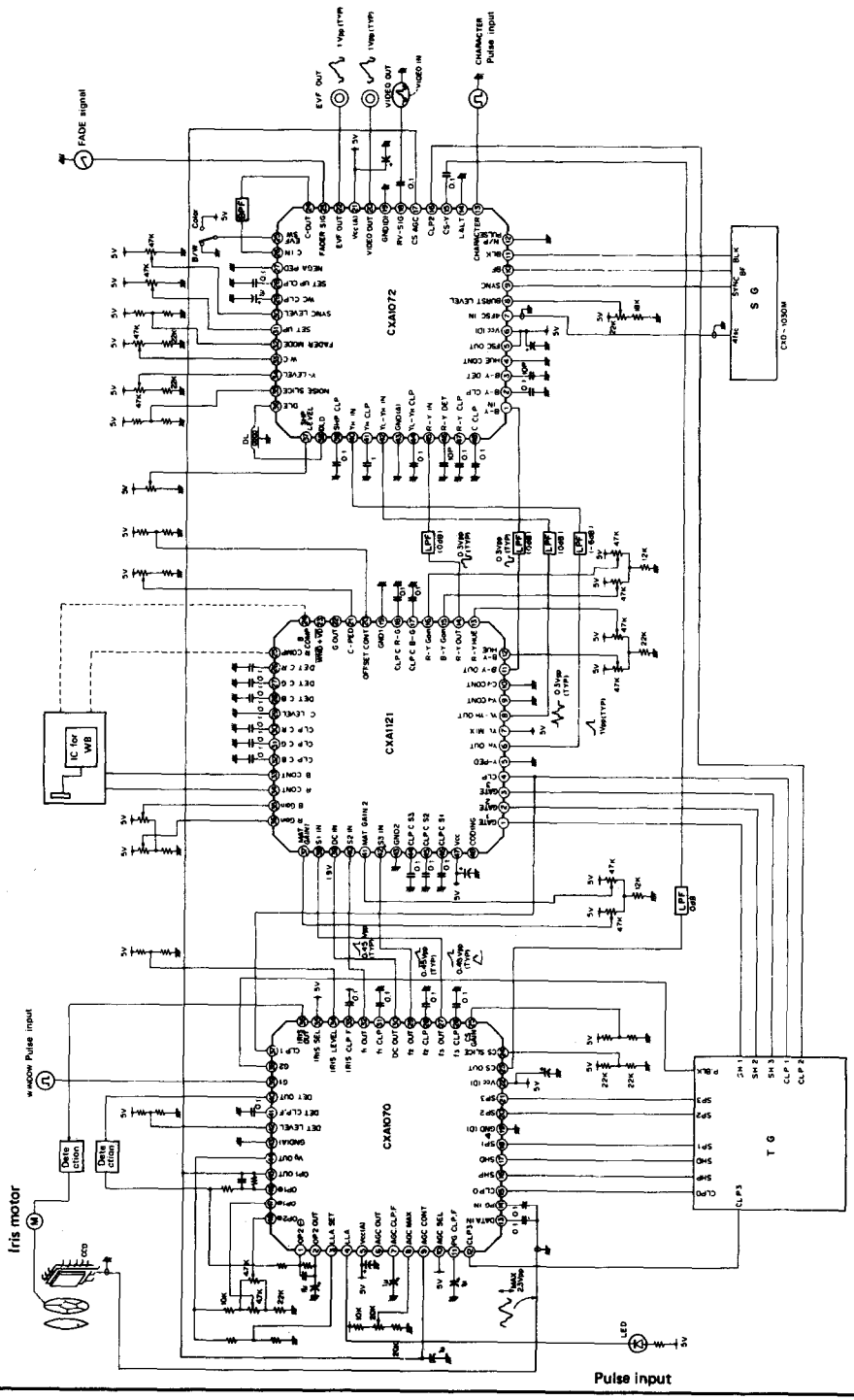
2. *Pins shown with an input signal timing chart are indicated in the test circuit as* ⊣⊢ . However there is also a test where the signal is input.

Input Signal Timing Chart



Note) Level is indicated in the conditions shown in the chart.

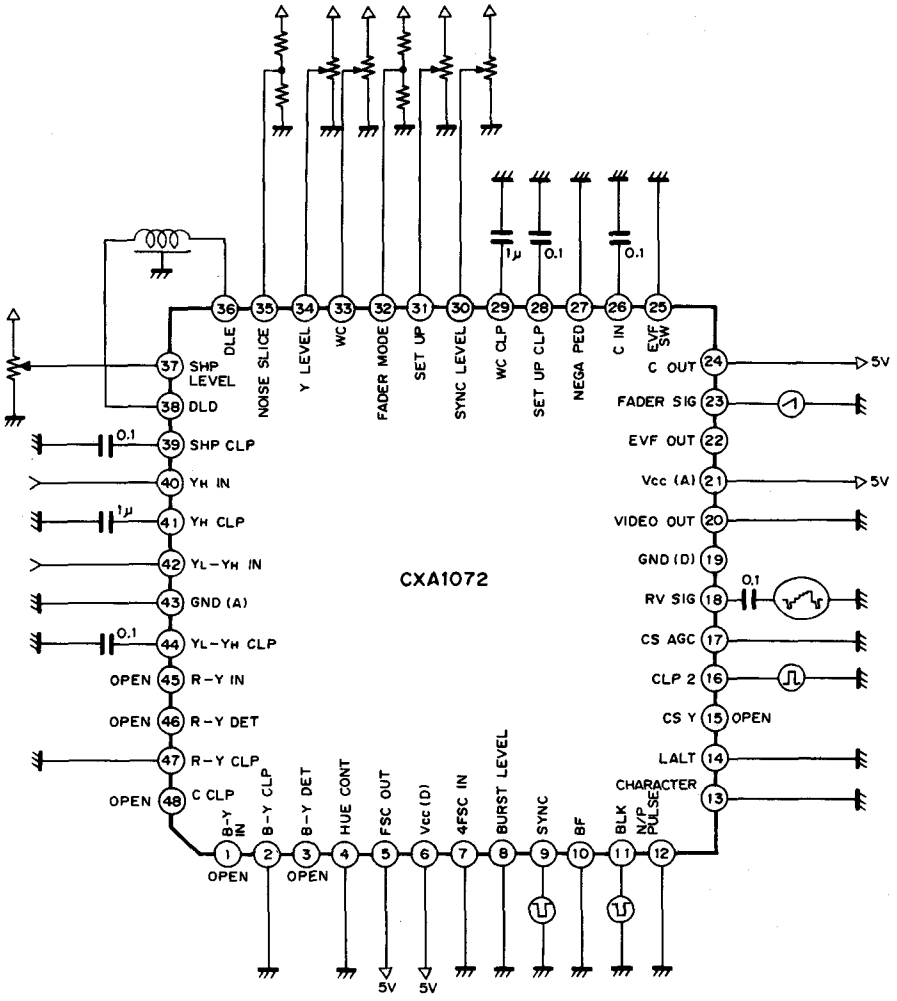
768H Color Compensation Stripe CCD Camera System Diagram



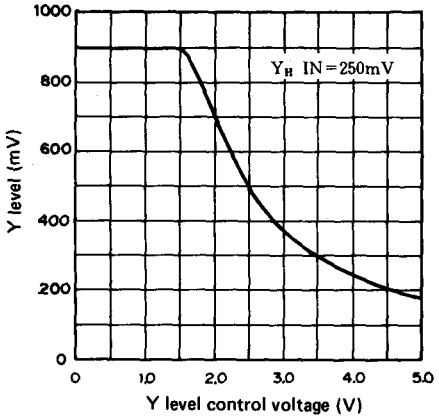
Note) 1. Resistances without value should better be set below 50 kΩ between Vcc and GND.
2. The unit of unspecified capacitance should be μF.

Application Circuit

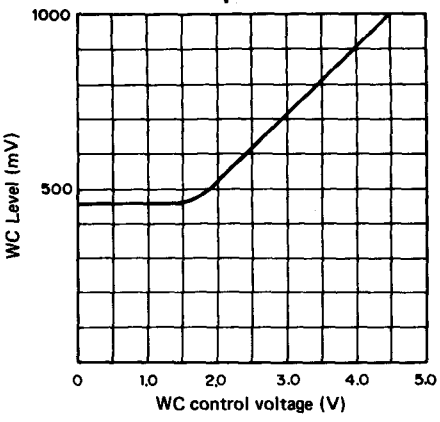
(During Black and White Mode)



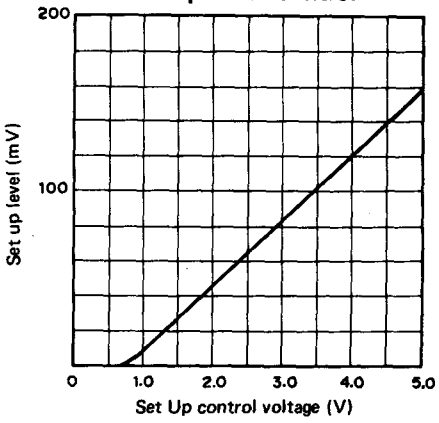
Y-levle control



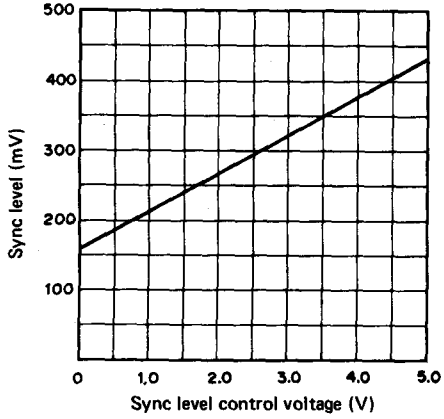
White clip level control



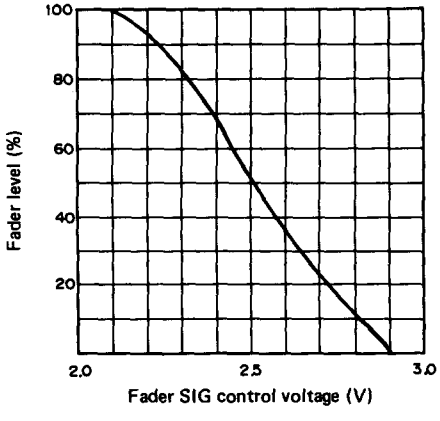
Set-up level control



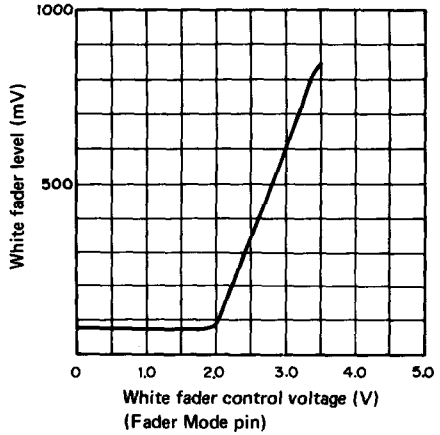
Sync level control



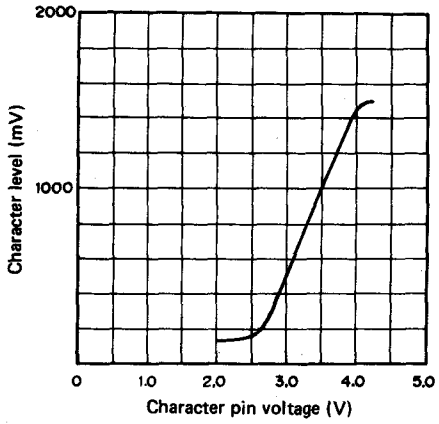
Fader level control



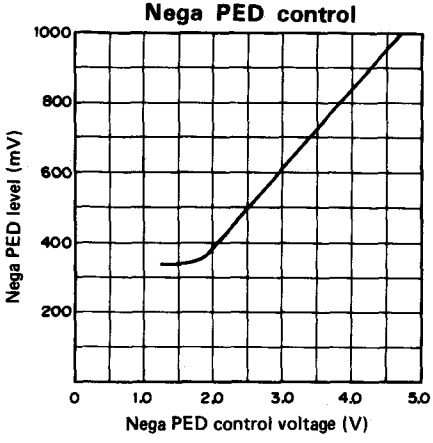
White fader level control



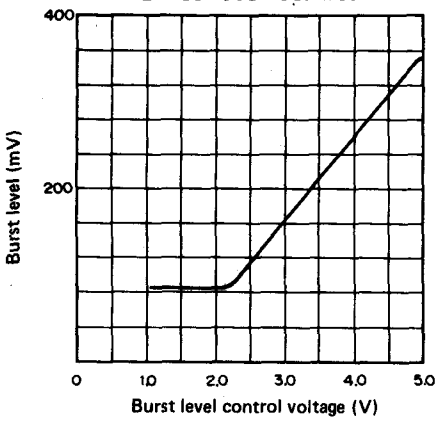
Character level control



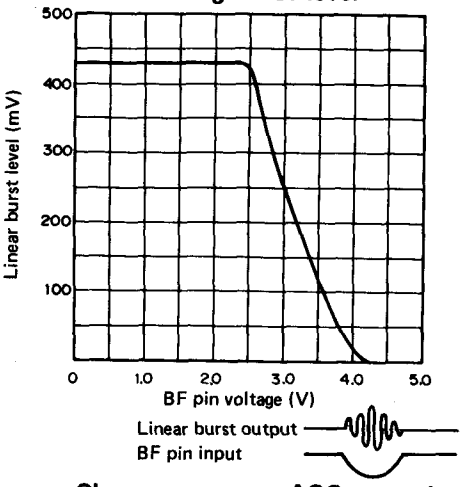
Nega PED control



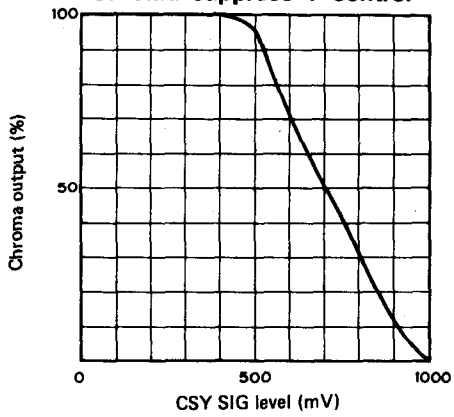
Burst level control



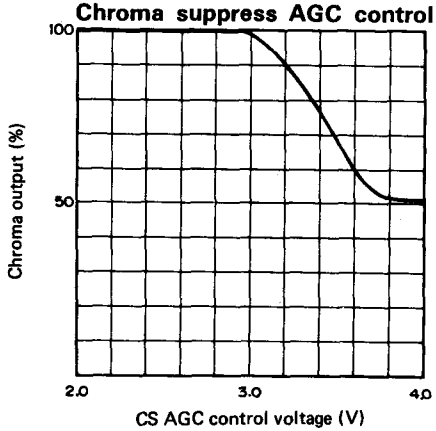
Analog burst level



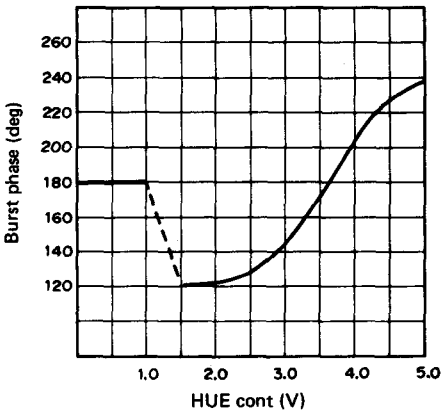
Chroma suppress Y control



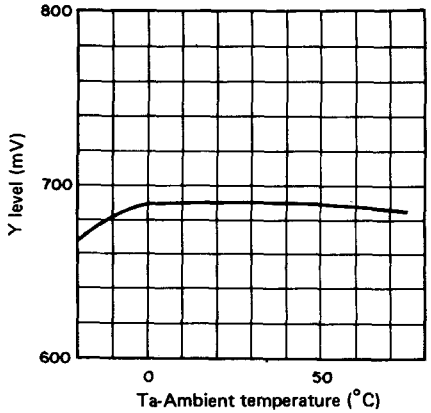
Chroma suppress AGC control



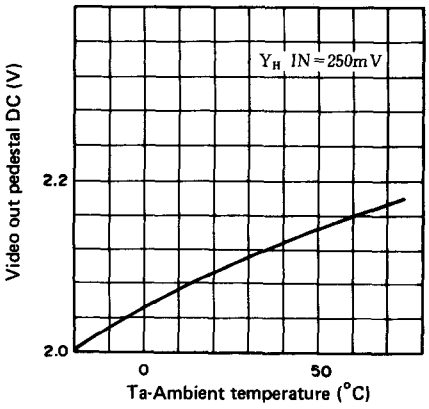
HUE control



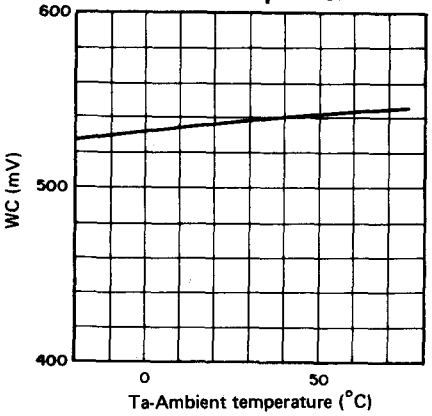
Y level



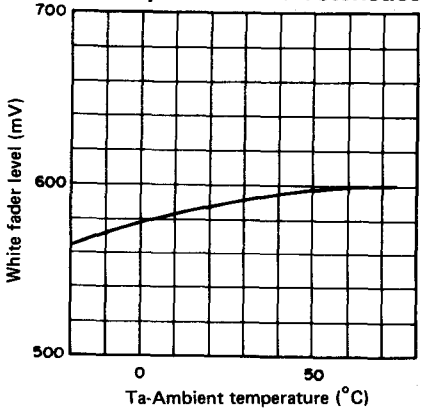
Video out pin pedestal DC



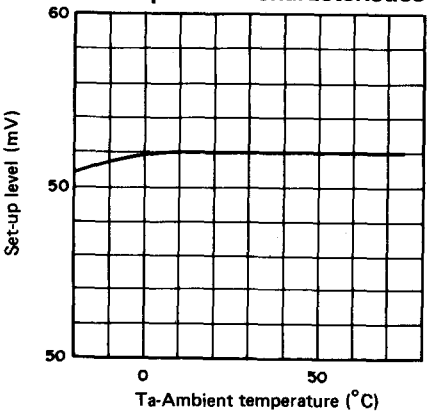
White clip level



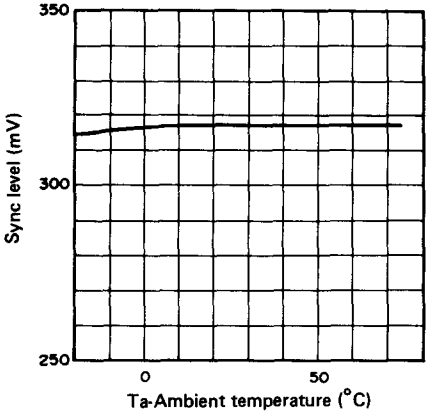
White fader level temperature characteristics



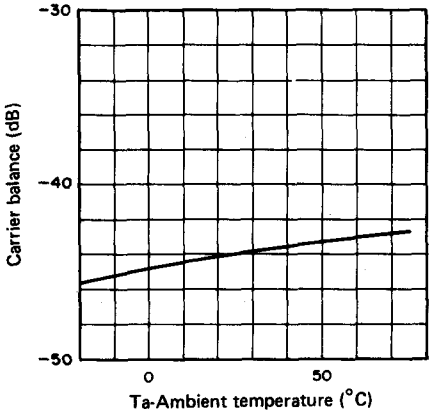
Set-up level temperature characteristics



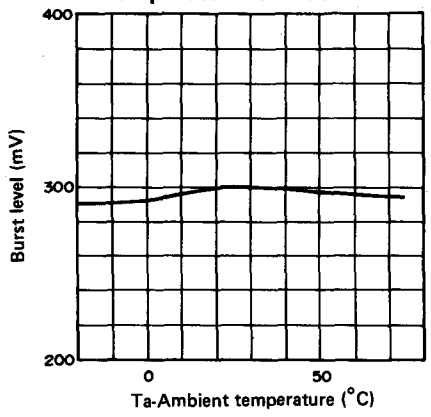
Sync level temperature characteristics



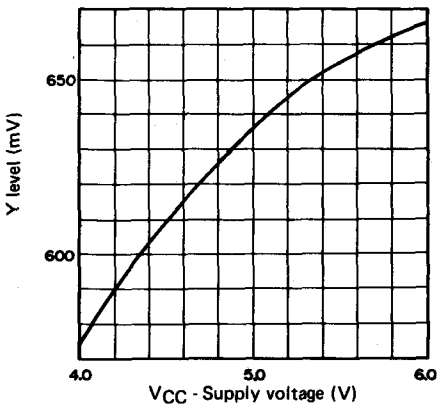
Carrier balance 3.58 MHz temperature characteristics



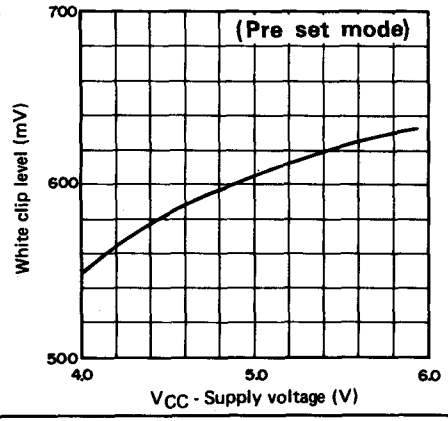
Burst level temperature characteristics



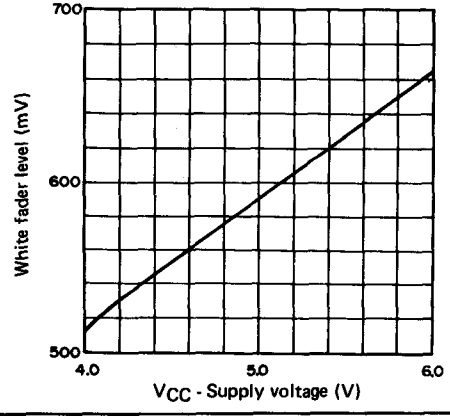
Y level supply fluctuations characteristics



White clip level supply fluctuations characteristics



White fader supply fluctuations characteristics



SONY

CXA1392Q/R

Encoder for CCD Color Camera

Description

The CXA1392Q/R is a bipolar IC developed as an encoder for CCD color cameras.

Color difference and luminance signals are input to be output as composite video and Y/C separate signals.

Features

- Carrier balance adjustment unnecessary (Carrier leak above 36 dB against burst)
- High S/N
- Low power consumption (140mW)

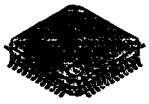
Applications

CCD camera

Absolute Maximum Ratings (Ta = 25℃)

- Supply voltage Vcc 7 V
- Storage temperature Tstg −65 to +150 ℃
- Allowable power dissipation PD 600 mW

CXA1392Q
48 pin QFP (Plastic)



CXA1392R
48 pin VQFP (Plastic)

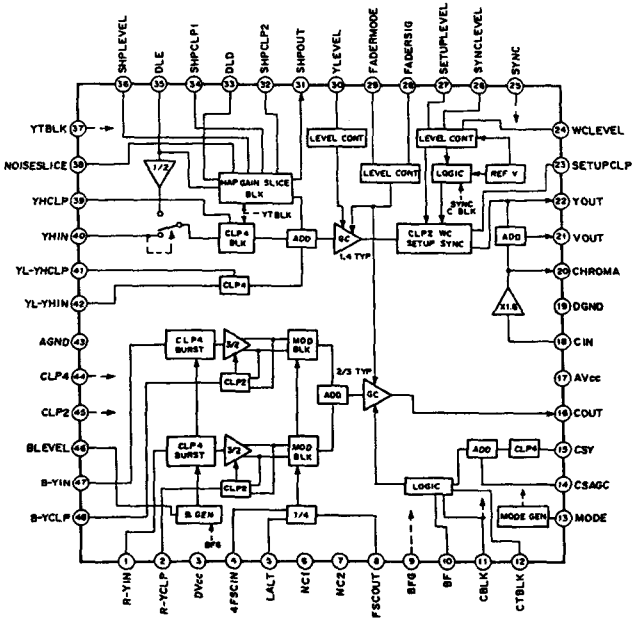
Structure

Bipolar silicon monolithic IC

Operating Conditions

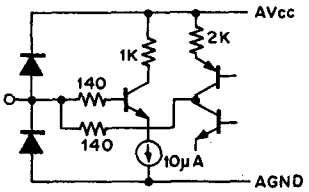
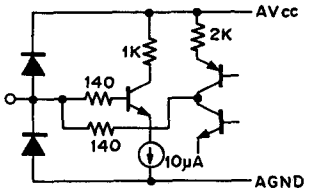
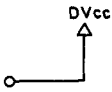
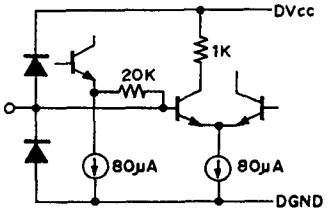
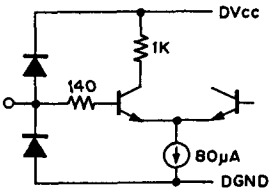
- Supply voltage Vcc 4.75 to 5.25 V
- Ambient temperature Topr −20 to +75 ℃

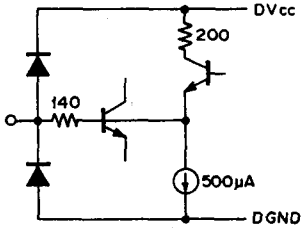
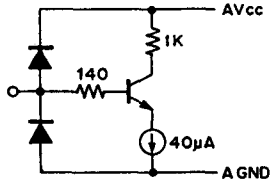
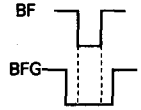
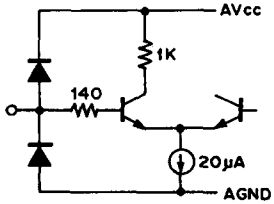
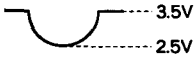
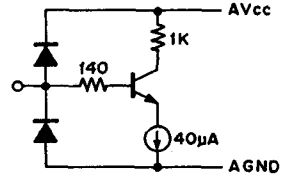
Block Diagram and Pin Configuration

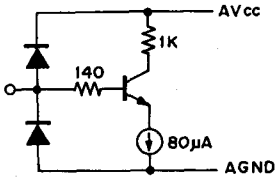
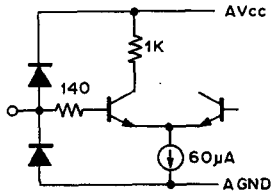
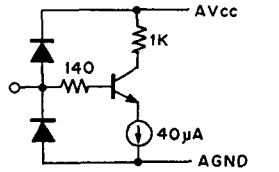
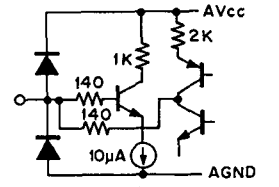
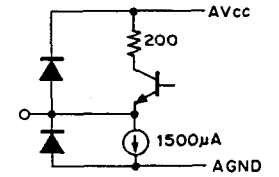


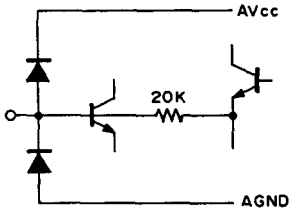
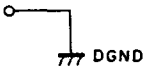
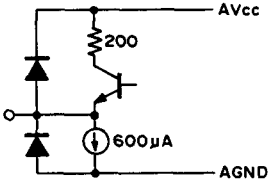
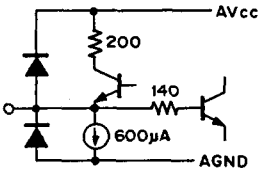
E89Z08 – ST

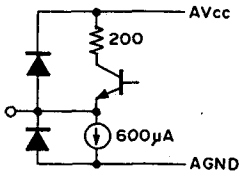
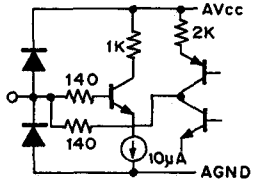
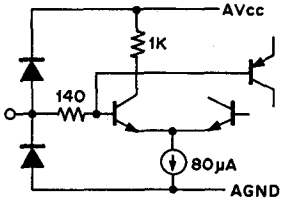
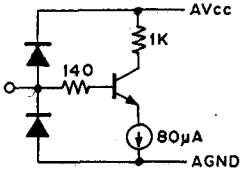
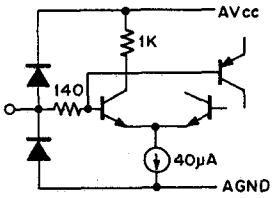
Pin Description

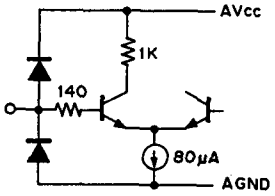
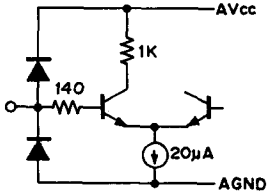
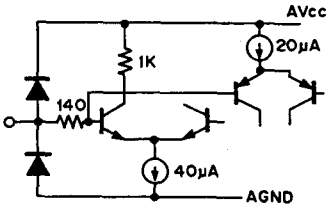
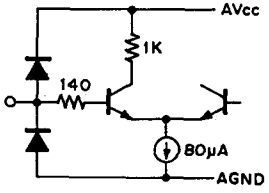
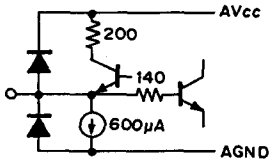
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	R-Y IN	3V		R−Y signal input pin. Clamped internally through C cut input.
2	R-Y CLP	3.4V		Pin connecting the capacitor for R−Y modulator clamp. Setting the capacitance to too small a value will enlarge the carrier leak. 0.1 μF and above is recommended.
3	DVcc	5V		Power supply pin for the 1/4 counter block.
4	4FSCIN	14.32MHz 1Vpp DC2.5V		Input pin for the 4FSC used to make up the Sub Carrier. Input through C cut. Set amplitude to over 500mVp-p.
5	LALT	0V		Input pin for Line Alternate signal during PAL mode. V_{TH} is at 2.5V. Input a pulse with an amplitude larger than $V_{TH} \pm 0.5V$. Set to GND during NTSC mode.

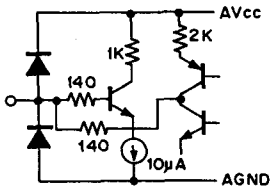
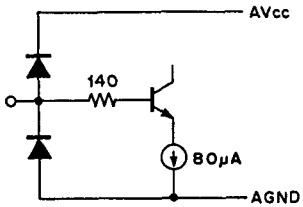
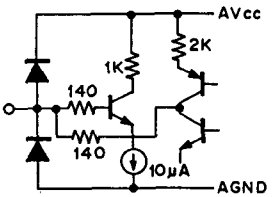
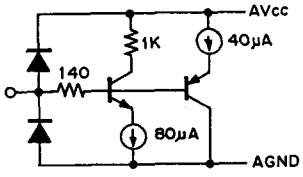
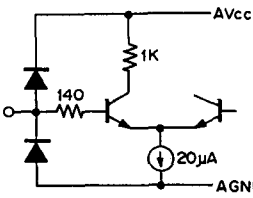
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
6	NC1	—		Not for use. Keep open.
7	NC2	—		Not for use. Keep open.
8	FSCOUT	5V		Outputs a sub carrier with the same phase as B − Y. When not in use, connection to Vcc prevents output and allows for 600 μA of current saving. Determining phase to 4FSC is impossible.
9	BFG	5V 0V		Inserts a pulse slightly larger than BF on both ends.  V_{TH} is at 2.5V. Input a pulse with an amplitude larger than $V_{TH} \pm 0.5V$.
10	BF	5V 0V		Inputs BF (burst flag) pulse. During analog burst, the input pulse smoothens the waveform. The input pulse waveform becomes the envelope of the analog burst waveform.  During the usual burst, be sure to input the pulse.
11	CBLK	5V 0V		Inputs CBLK (composite blanking) pulse. V_{TH} is at 2.5V. Input a pulse with an amplitude larger than $V_{TH} \pm 0.5V$.

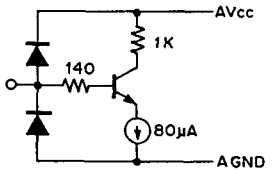
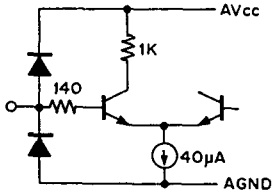
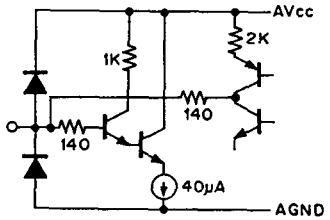
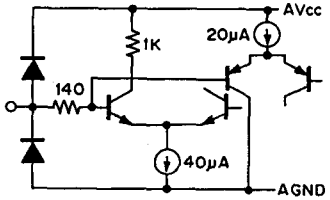
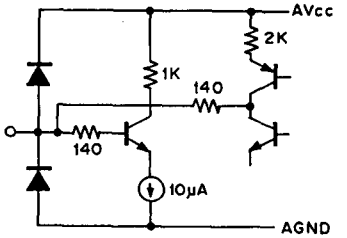
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
12	CTBLK	5V 0V		Inputs CT (chroma titler) pulse. This signal prevents the application of chroma suppress during the titler signal period. V_{TH} is at 2.5V. Input a pulse with an amplitude larger than $V_{TH} \pm 0.5V$.
13	MODE	0V		Selects NTSC, PAL or NTSC × 2, PAL × 2 modes. 0V : NTSC × 1 2.5V : NTSC × 2 3.5V : PAL × 2 5V : PAL × 1
14	CSAGC	0V		Suppresses chroma signal at the AGC gain control signal. 3V (100%) to 4.2V (50%)
15	CSY	2.4V		Suppresses chroma signal at the Y signal. 200mV (100%) to 700mV (0%) Inputs at C cut. Clamped internally.
16	COUT	2.8V		Chroma signal output pin. Output as rectangular waves.

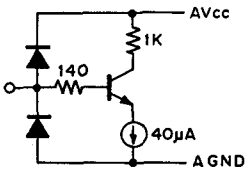
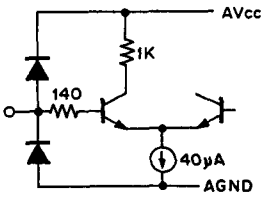
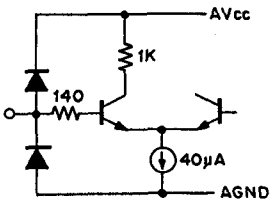
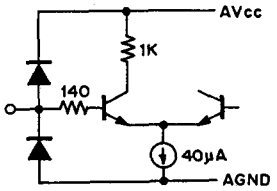
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
17	AVcc	5V		Power supply pin for other than 1/4 counter block.
18	CIN	2.5V		Input pin for chroma signal passed through BPF. Internally biased with a 20kΩ resistance. Input at C cut.
19	DGND	0V		GND pin for 1/4 counter block.
20	CHROMA	2V		Signals input from CIN are amplified and output through this pin. Chroma signal output pin when used for Y/C separation output.
21	VOUT	1.8V		Output pin of composite video signal. When not in use, connection to Vcc allows for 900 μA of current saving.

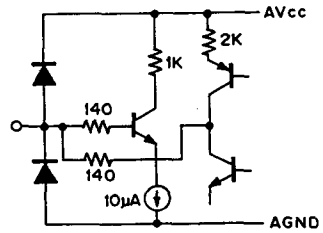
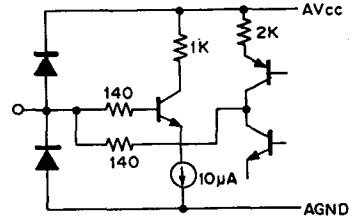
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
22	YOUT	2.4V		Y signal output pin when used for Y/C separation output.
23	SETUPCLP	3.3V		Connecting pin for the white clip clamp capacitor. Over 0.1 μF is recommended.
24	WC LEVEL	3.4V		White clip level control pin. 1.6V (550mV) to 5V (1110mV)
25	SYNC			Sync pulse input pin. V_{TH} is at 2.5V. Input a pulse with an amplitude larger than $V_{TH} \pm 0.5V$.
26	SYNC LEVEL	0V		Sync level control pin. 1.6V (180mV) to 5V (380mV) 0V (287mV) preset.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
27	SETUP LEVEL	3.5V		Set up level control pin. 2.4V (0mV) to 5V (120mV)
28	FADER SIG	0V		Controls the signal suppress level during Black Fader. Controls the signal suppress level during White Fader and at the same time controls the set up level. Signal suppress control : 2V (100%) to 2.9V (0%) Set up level control : 2V (0%) to 2.9V (100%) Black Fader/White Fader mode selection executed through Fader Mode pin.
29	FADER MODE	3.5V		Black Fader and White Fader mode select pin. Also controls the final value (100%) of White Fader white level (set up level). 0V (Black Fader) 1.8V (100mV) to 5V (630mV) (White Fader)
30	Y LEVEL	3.4V		Y signal level control pin. 1.6V (−3.5dB) to 5V (9dB)
31	SHP OUT	3V		Aperture signal output pin. When not in use, connection to Vcc allows for 700 μA of current saving.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
32	SHPCLP2	3.2V		Connects the clamp capacitor used for the slice of the aperture signal.
33	DLD	2.1V		Connects the delay line drive side of the aperture signal.
34	SHPCLP1	3.2V		Connects the clamp capacitor used for the slice of the aperture signal.
35	DLE	2.1V		Connects the delay line end side of the aperture signal. When this pin signals are used as Y_H signals, Y_H IN pin is connected to Vcc.
36	SHP LEVEL	3.5V		Control pin of the aperture signal level. 2.6V (14dB) to 4.2V (−25dB).

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
37	YTBLK	5V 0V		Inputs Y_T (Y titler) pulse. V_{TH} is at 2.5V. Input a pulse with an amplitude larger than V_{TH} ± 0.5V.
38	NOISESLICE	3.5V		Controls the slice level of the aperture signal. 1.8V (0mV) to 5V (150mV)
39	YHCLP	2.7V		Connects the capacitor for Y_H input clamp.
40	YHIN	500mV 1.05V		Y_H signal input pin. When DLE pin signal is set as Y_H signal, connect this pin to Vcc. The input signal DC clamp range stands at 1.05V ± 0.65V. The standard signal level is at 500mV.
41	YL-YHCLP	3.4V		Connects the capacitor for Y_L-Y_H input clamp.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
42	YL-YH IN	2.8V		Inputs V aperture signals, titler signals and Y_L-Y_H signals. The input signal DC clamp range stands at 2.8V ± 1.1V.
43	AGND	0V		GND pin for other than 1/4 counter block.
44	CLP4	5V 0V		CLP4 pulse input pin. V_{TH} is at 2.5V. Input a pulse with an amplitude larger than V_{TH} ± 0.5V.
45	CLP2	5V 0V		CLP2 pulse input pin. V_{TH} is at 2.5V. Input a pulse with an amplitude larger than V_{TH} ± 0.5V.
46	B LEVEL	3.5V		Controls the burst level. 1.6V (95mVp-p) to 5V (280mVp-p) (NTSC pulse burst mode)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
47	B-Y IN	3V		R-Y signal input pin. Clamped internally through C cut input.
48	B-Y CLP	3.4V		Connects the capacitor for B-Y modulator clamp. Setting the capacitance to too small a value will enlarge the carrier leak. Over 0.1 μF is recommended.

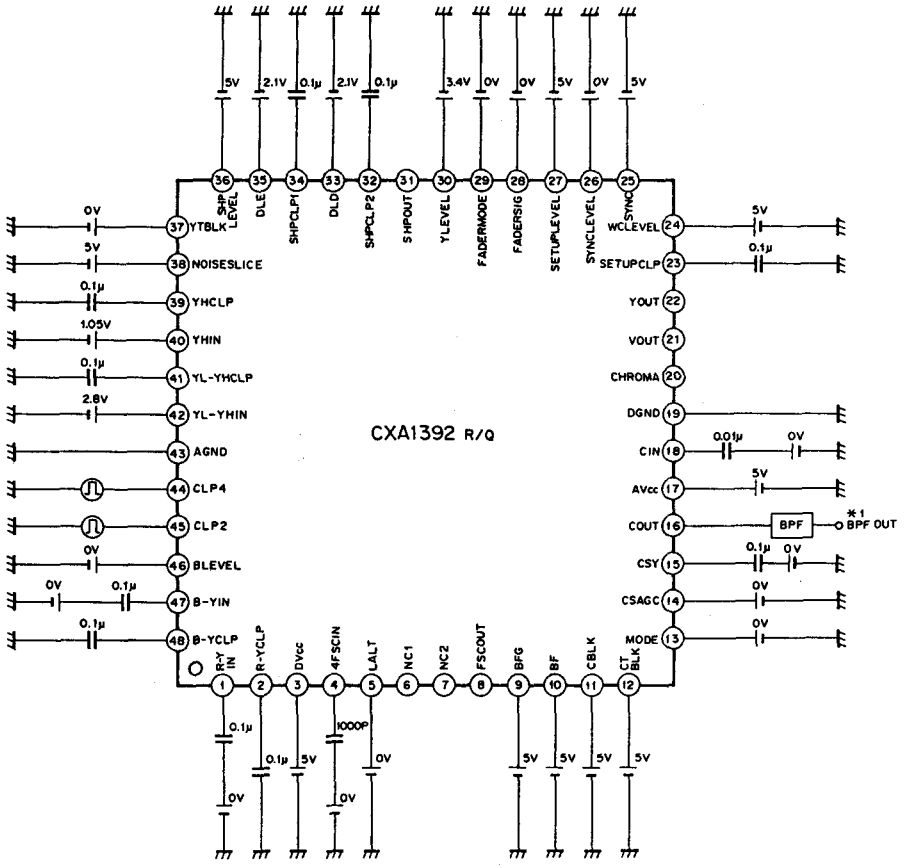
Electrical Characteristics (Vcc = 5V, Ta = 25°C)

No.	Item	Symbol	Conditions	Min	Typ.	Max.	Unit
1	Current Supply	Icc	AVcc + DVcc	19	28	38	mA
2	YH GAIN TYP	YHTYP	FSCOUT = 5V VOUT = 5V SHPOUT = 5V YHIN (500mV pulse) →YOUT	1.8	2.8	3.8	dB
3	YH GAIN MIN	YHMIN	YHIN (500mV pulse) →YOUT YLEVEL = 1.6V	—	− 4	− 2	dB
4	YH GAIN MAX	YHMAX	YHIN (250mV pulse) →YOUT YLEVEL = 5V	8	9.1	—	dB
5	YL-YH GAIN	YL-YH	Y_L-Y_HIN (500mV pulse) →YOUT	1.8	2.8	3.8	dB
6	DLE GAIN	DLE	DLE (1V pulse) →YOUT YHIN = 5V	− 4.3	− 3.3	− 2.3	dB
7	VOUT GAIN	VOUT	YHIN (500mV pulse) →VOUT	1.3	2.3	3.3	dB
8	WHITE FADER MIN	WFMIN	CBLK pulse FADERMODE = 1.6V WFMIN = YOUT output level − SETMAX (No.13)	68	86	104	mV
9	WHITE FADER MAX	WFMAX	CBLK pulse FADERMODE = 5V WFMAX = YOUT output level − SETMAX (No.13)	527	620	713	mV
10	WHITE CLIP MIN	WCMIN	YHIN (500mV pulse) →YOUT CBLK pulse WCLEVEL = 1.6V	522	550	578	mV
11	WHITE CLIP MAX	WCMAX	YHIN (500mV pulse) →YOUT CBLK pulse WCLEVEL = 5V	1056	1112	1168	mV
12	WHITE CLIP PRESET	WCPRE	YHIN (500mV pulse) →YOUT CBLK pulse WCLEVEL = 0V	796	838	880	mV
13	SETUP MAX	SETMAX	CBLK pulse→YOUT SETUPLEVEL = 5V	113	126	139	mV
14	SYNC MIN	SYNCMIN	SYNC pulse→YOUT SYNCLEVEL = 1.6V	165	180	195	mV
15	SYNC MAX	SYNCMAX	SYNC pulse→YOUT SYNCLEVEL = 5V	363	383	403	mV
16	SYNC PRESET	SYNCPRE	SYNC pulse→YOUT SYNCLEVEL = 0V	272	287	302	mV
17	SHP-YOUT GAIN	SHPYOUT	DLD (40mV pulse) →YOUT SHPLEVEL = 2.6V YHIN (500mV pulse)	12	14	16	dB
18	SHP DOWN MIN	SHPMIN	DLD (40mV pulse) →SHPOUT SHPLEVEL = 4.2V	—	− 25	− 5.5	dB
19	SHP DOWN TYP	SHPTYP	DLD (40mV pulse) →SHPOUT SHPLEVEL = 3.4V	5.5	7	8.5	dB
20	SHP DOWN MAX	SHPMAX	DLD (40mV pulse) →SHPOUT··· (DOWNMAX) SHPLEVEL = 2.6V	11.7	13.2	14.7	dB
21	SHP DOWN/UP	SHPD/U	DLE (40mV pulse) →SHPOUT··· (UPMAX) SHPLEVEL = 2.6V SHPD/U = DOWNMAX/UPMAX	2.4	2.8	3.2	times
22	SHP SLICE MAX	SLICEMAX	DLD (40mV pulse) →SHPOUT··· (SLMAX) SHPLEVEL = 2.6V SLICEMAX = DOWNMAX-SLMAX	135	150	165	mV
23	B-Y GAIN	B-Y	B-YIN (300mV pulse) →BPFOUT 4FSCIN = SIN 1Vp-p 14.32MHz B-Y = 20log {BPFOUT(mVp-p)/300mV}	0.4	1.6	2.8	dB

No.	Item	Symbol	Conditions	Min	Typ.	Max.	Unit
24	R-Y GAIN	R-Y	R-YIN(300mV pulse)→BPFOUT ···(R-Y level) 4FSCIN = SIN 1Vp-p 14.32MHz R-Y = 20log {BPFOUT(mVp-p)/300mV}	0.4	1.6	2.8	dB
25	CARRIER LEAK 3.58MHz	L358	4FSCIN = SIN 1Vp-p 14.32MHz L358 = 20log {286mVp-p/ BPFOUTlevel (mVp-p)} BURST (Typ.)	36	48	—	dB
26	CARRIER LEAK 500kHz	L500	4FSCIN = SIN 1Vp-p 2MHz L500 = 20log {286mVp-p/BPFOUT level (mVp-p)} BURST (Typ.)	36	58	—	dB
27	COUT DRANGE	COUTD	R-YIN (600mV pulse) →BPFOUT 4FSCIN = SIN 1Vp-p 14.32MHz	670	730	—	mV
28	CS AGC MAX	CSAGCMAX	R-YIN (300mV pulse) →BPFOUT 4FSCIN = SIN 1Vp-p 14.32MHz CSAGC = 4.2V CSAGCMAX = (BPFOUT level/R-Y level) ×100%	47	52	57	%
29	FSCOUT amplitude	FSC	FSCOUT DC amplitude at 4FSCIN = 2V, 3V	585	673	760	mV
30	BURST NTSC MIN	NTMIN	BFG pulse→BPFOUT BLEVEL = 1.6V 4FSCIN = SIN 1Vp-p 14.32MHz	80	95	110	mV
31	BURST NTSC MAX	NTMAX	BFG pulse→BPFOUT BLEVEL = 5V 4FSCIN = SIN 1Vp-p 14.32MHz	250	280	312	mV
32	BURST PAL MIN	PALMIN	BFG pulse→BPFOUT BLEVEL = 1.6V MODE = 5V 4FSCIN = SIN 1Vp-p 14.32MHz	89	105	120	mV
33	BURST PAL MAX	PALMAX	BFG pulse→BPFOUT BLEVEL = 5V MODE = 5V 4FSCIN = SIN 1Vp-p 14.32MHz	283	316	350	mV
34	BURST NTSC×2 MIN	NT2MIN	BFG pulse→BPFOUT BLEVEL = 1.6V MODE = 2.5V 4FSCIN = SIN 1Vp-p 14.32MHz	153	180	207	mV
35	BURST NTSC×2 MAX	NT2MAX	BFG pulse→BPFOUT BLEVEL = 5V MODE = 2.5V 4FSCIN = SIN 1Vp-p 14.32MHz	468	520	572	mV
36	BURST PAL×2 MIN	PAL2MIN	BFG pulse→BPFOUT BLEVEL = 1.6V MODE = 3.5V 4FSCIN = SIN 1Vp-p 14.32MHz	171	202	232	mV
37	BURST PAL×2 MAX	PAL2MAX	BFG pulse→BPFOUT BLEVEL = 5V MODE = 3.5V 4FSCIN = SIN 1Vp-p 14.32MHz	535	595	655	mV
38	CIN-VOUT GAIN	CINVOUT	CIN (SIN 400mVp-p 3.58MHz) →VOUT	2.5	3.5	4.5	dB
39	CIN-CHROMA GAIN	CINCHROMA	CIN (SIN 400mVp-p 3.58MHz) → CHROMA	2.1	3.1	4.1	dB

Ref.) YHIN→Y OUT Frequency characteristics gain 10MHz, −2.3dB (Typ.)

Test Circuit



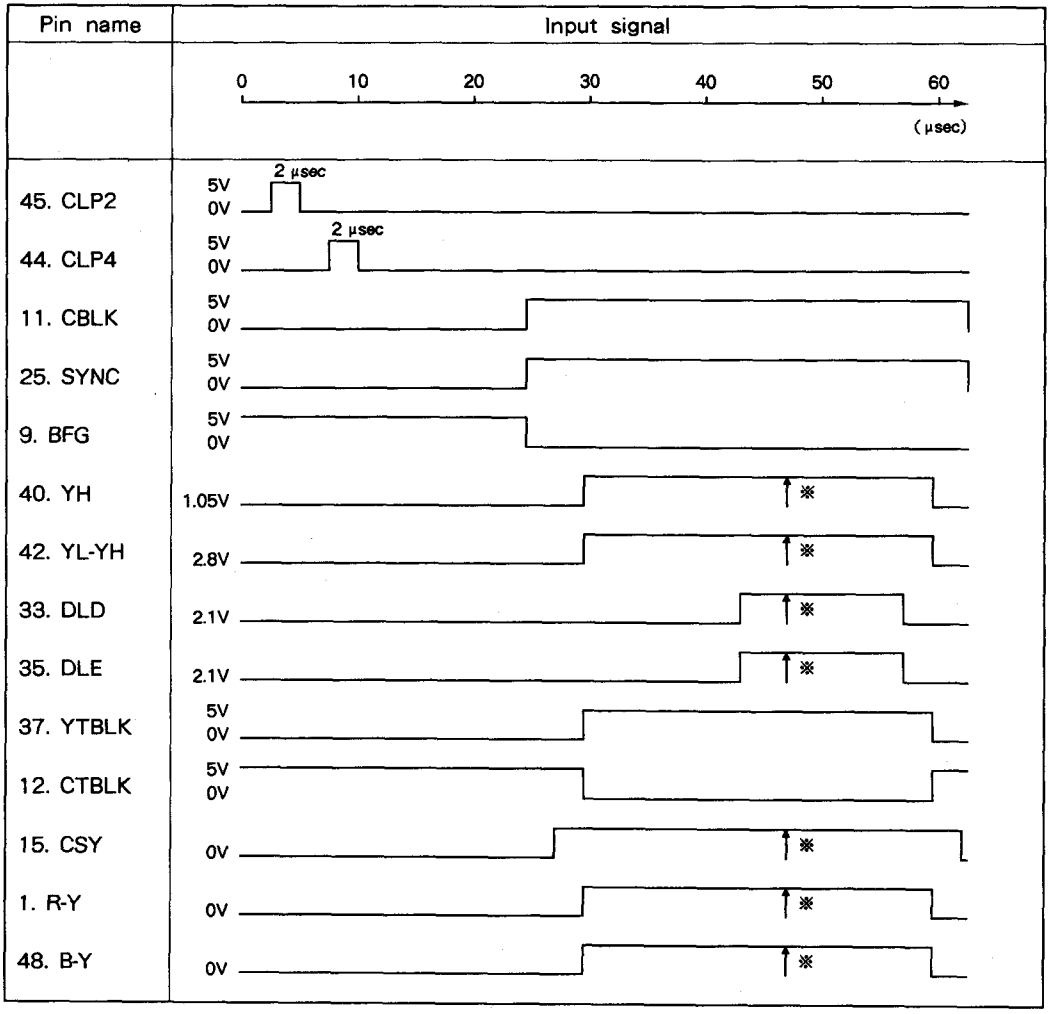
Above conditions are given as the typical setting. The individual conditions of each item are indicated in the chart.

*1 For BPF characteristics proceed as follows.

① When 4FSC IN = 14.32MHz use a 3.58MHz band pass filter where through the input of a 3.58MHz sine wave a ratio of 2 to 1 is obtained for the input vs. output.

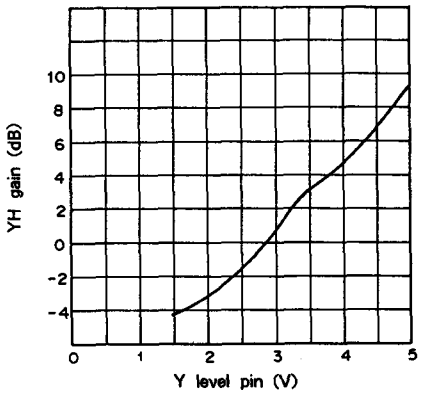
② When 4FSC IN = 2MHz, use a 500kHz band pass filter where through the input of a 500kHz sine wave a ratio of 2 to 1 is obtained for the input vs. output.

Input Signal Timing Chart

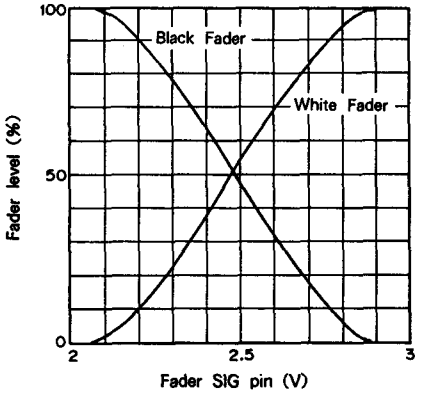


Note) Level is indicated in the conditions shown in the chart.

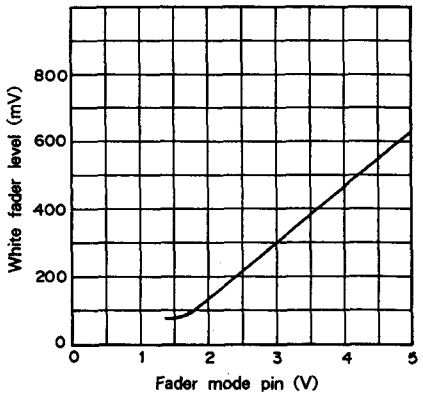
YH Gain control characteristics



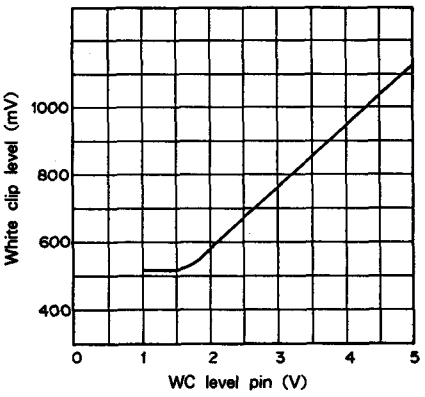
Y fader control characteristics



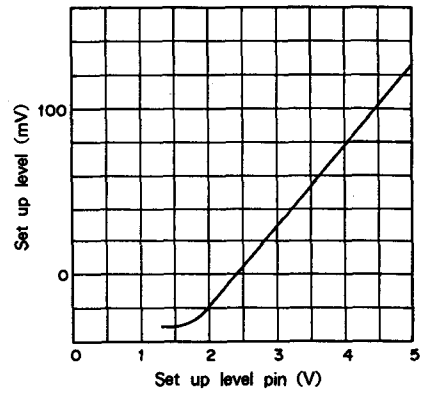
White fader control characteristics



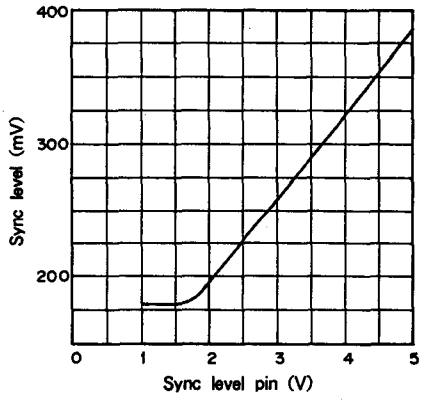
White clip control characteristics



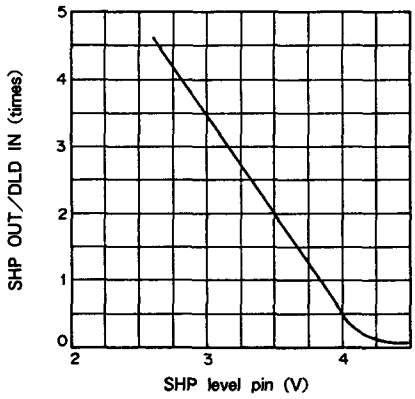
Set up level control characteristics



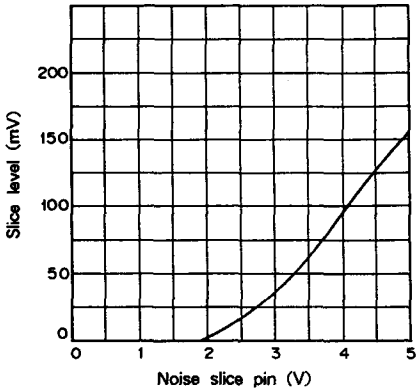
Sync level control characteristics



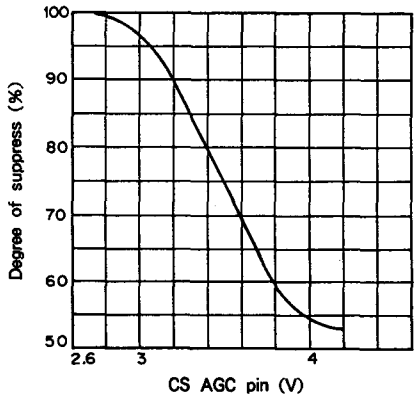
SHP gain control characteristics



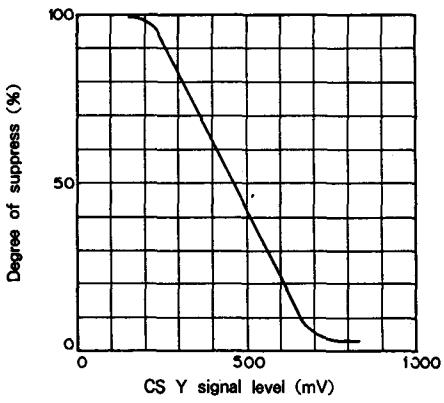
SHP noise slice characteristics



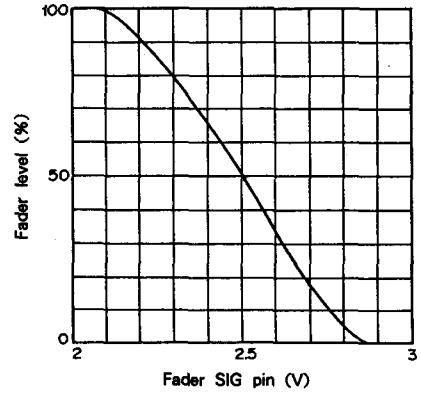
CS AGC control characteristics



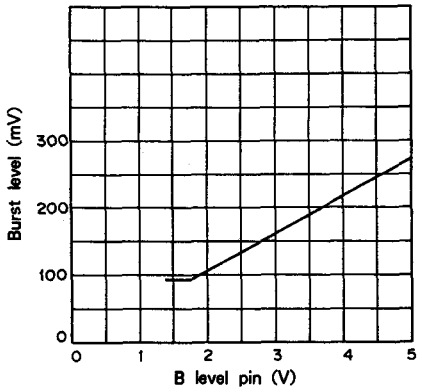
CS Y control characteristics



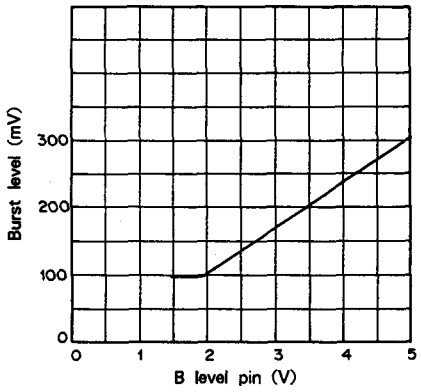
Chroma fader control characteristics



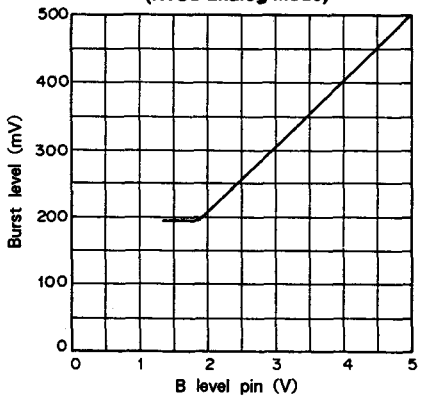
Burst level control characteristics (NTSC pulse mode)



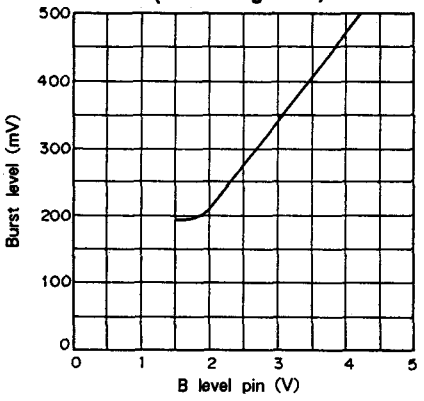
Burst level control characteristics (PAL pulse mode)



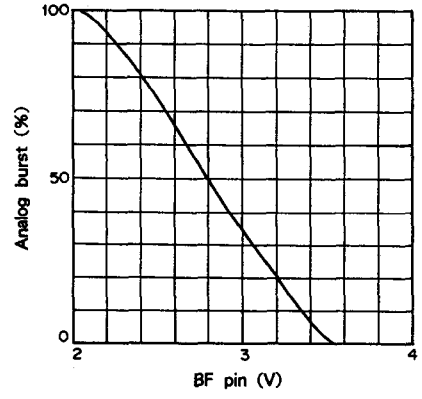
Burst level control characteristics (NTSC analog mode)



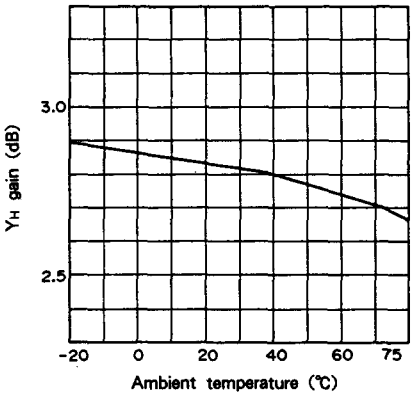
Burst level control characteristics (PAL analog mode)



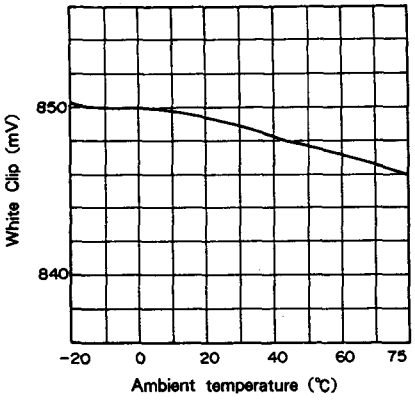
Analog burst control



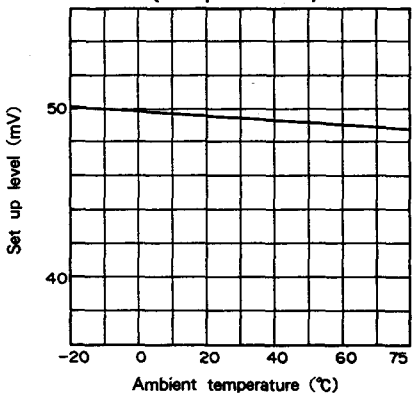
Y_H gain typical temperature characteristics



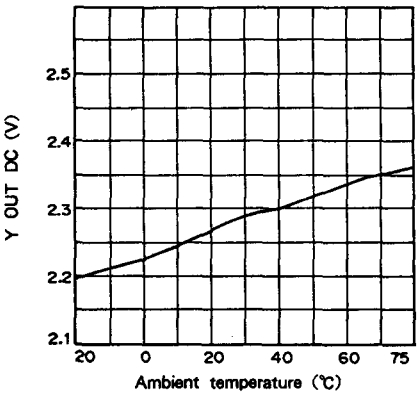
White clip preset temperature characteristics



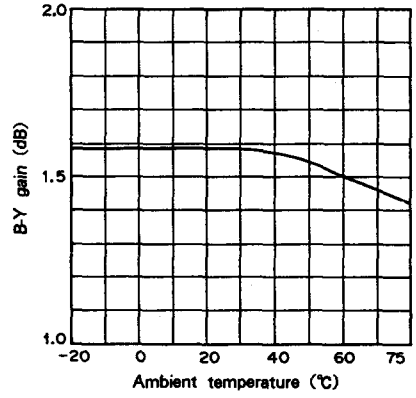
Set up level temperature characteristics (Set up level=3.4V)



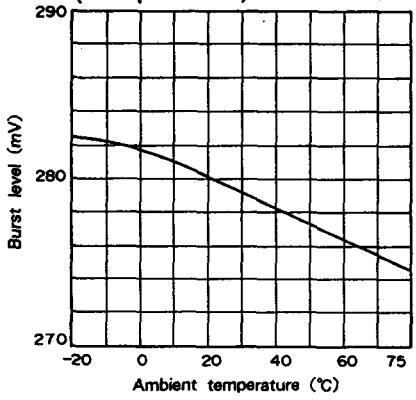
Y OUT DC temperature characteristics



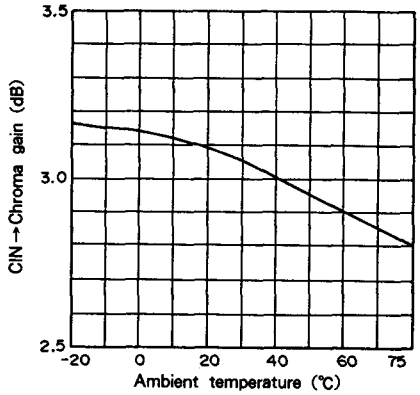
B-Y gain temperature characteristics



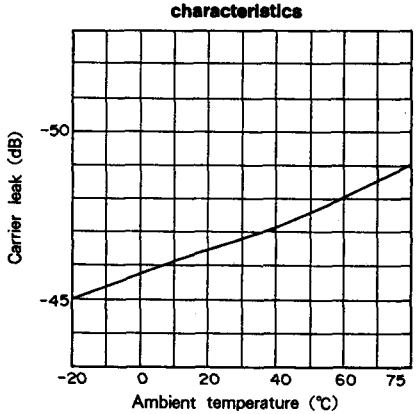
Burst NTSC maximum temperature characteristics (NTSC pulse mode) Burst level=5.0V



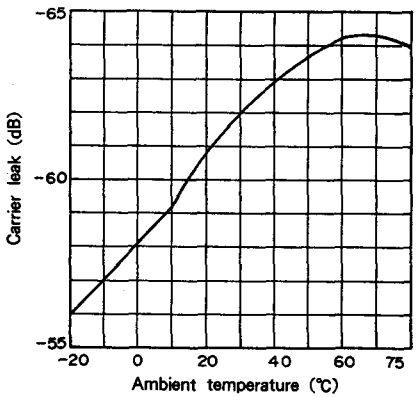
CIN → Chroma gain temperature characteristics



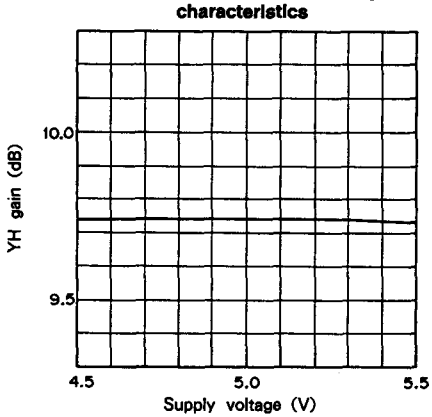
Carrier leak 3.58 MHz temperature characteristics



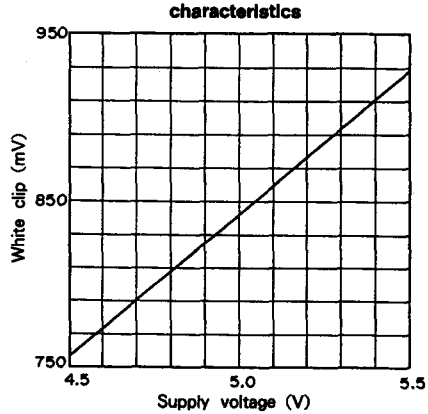
Carrier leak 500 kHz temperature characteristics



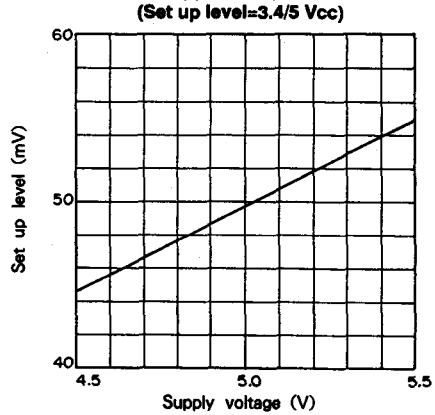
Y_H gain maximum supply voltage characteristics



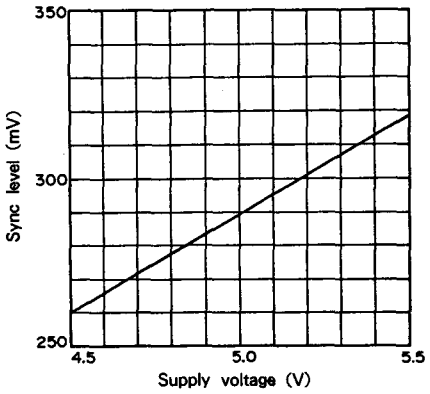
White clip preset supply voltage characteristics



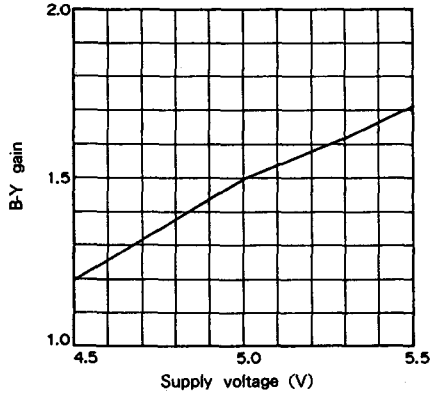
Set up level supply voltage characteristics (Set up level=3.4/5 Vcc)



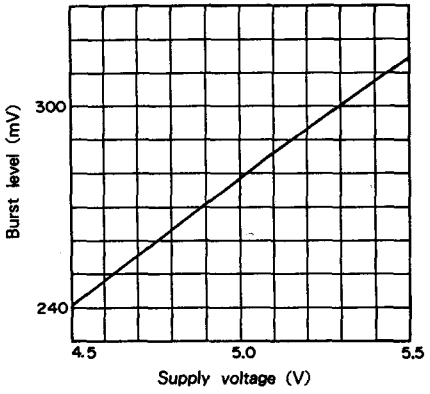
Sync level preset supply voltage characteristics



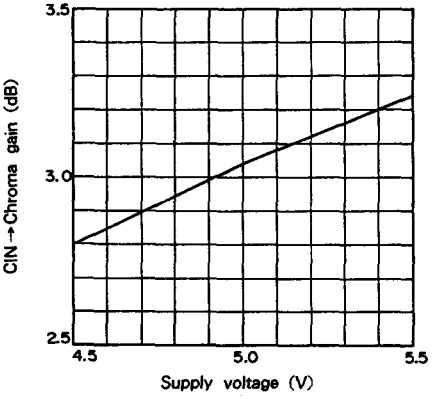
B-Y gain supply voltage characteristics



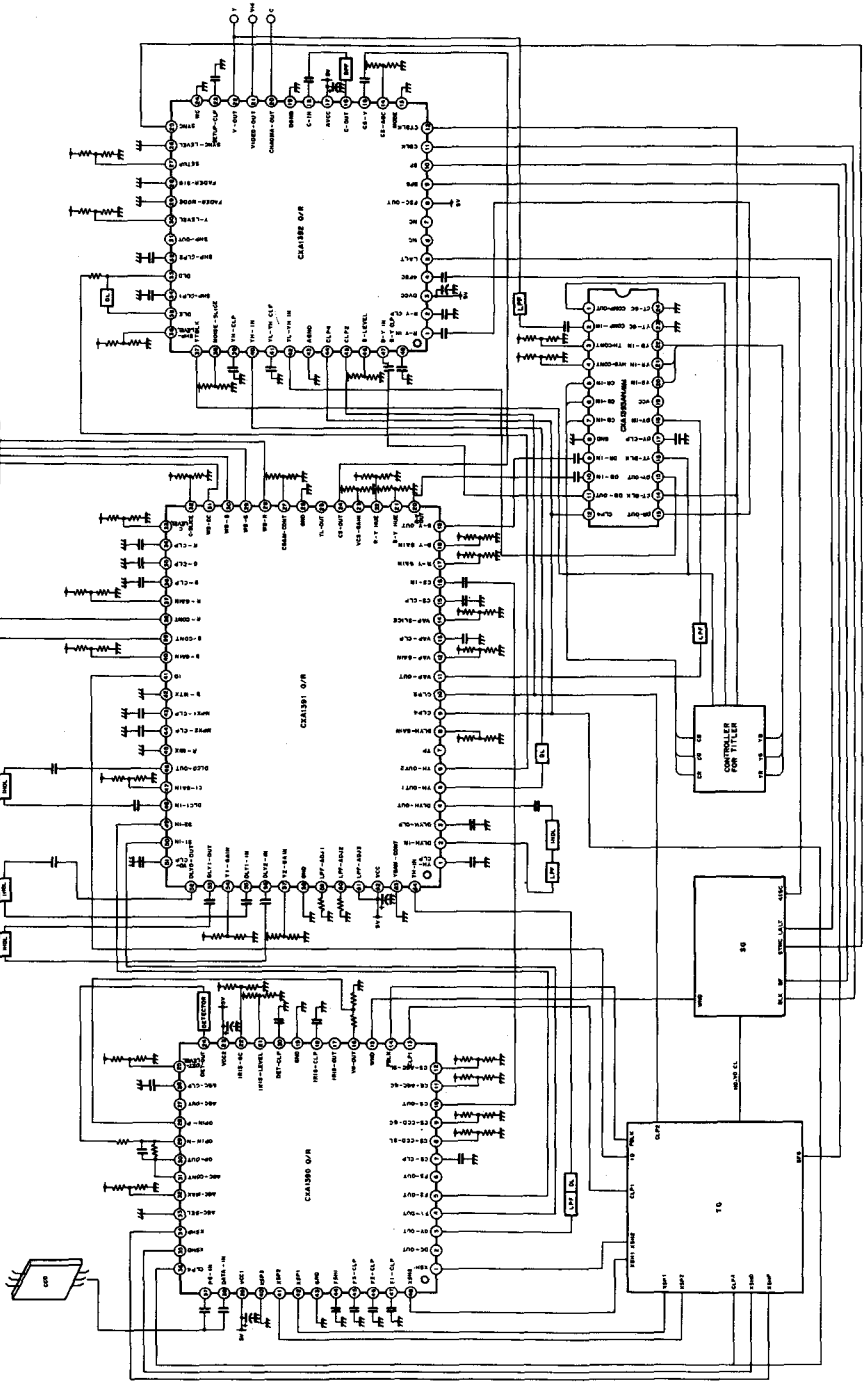
Burst level supply voltage characteristics (NTSC pulse mode) Burst level=Vcc



CIN→Chroma gain supply voltage characteristics

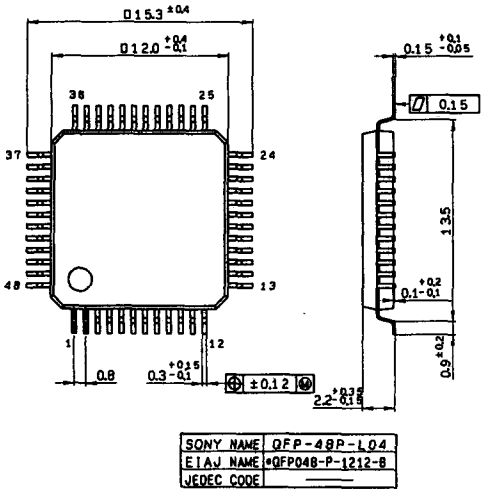


CXA1390 Series System Diagram

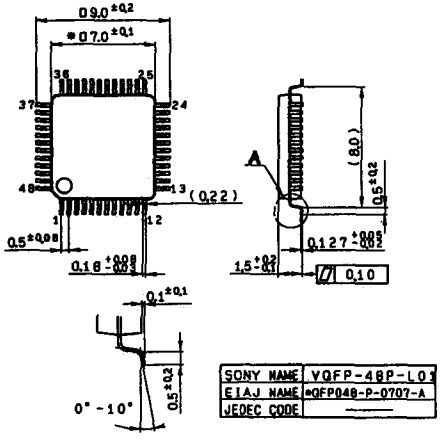


Package Outline Unit : mm

CXA1392Q 48 pin QFP (Plastic) 0.6g



CXA1392R 48 pin VQFP (Plastic) 0.2g



Detailed diagram of A

Note) Dimensions marked with *
does not include resin residue

SONY

CXA1592Q/R

Encoder for CCD Color Camera

Description

The CXA1592Q/R is a bipolar IC developed as an encoder for CCD color cameras.

Color difference and luminance signals are input to be output as composite video and Y/C separate signals.

The CXA1592 is a variant of the CXA1392 in which the down/up ratio and level of sharpness signal have been changed from 1 : 3 to 1.5 : 1.5.

CXA1592Q
48 pin QFP (Plastic)

CXA1592R
48 pin VQFP (Plastic)

Features

- Carrier balance adjustment unnecessary (Carrier leak above 36 dB against burst)
- High S/N
- Low power consumption (140mW)

Applications

CCD camera

Structure

Bipolar silicon monolithic IC

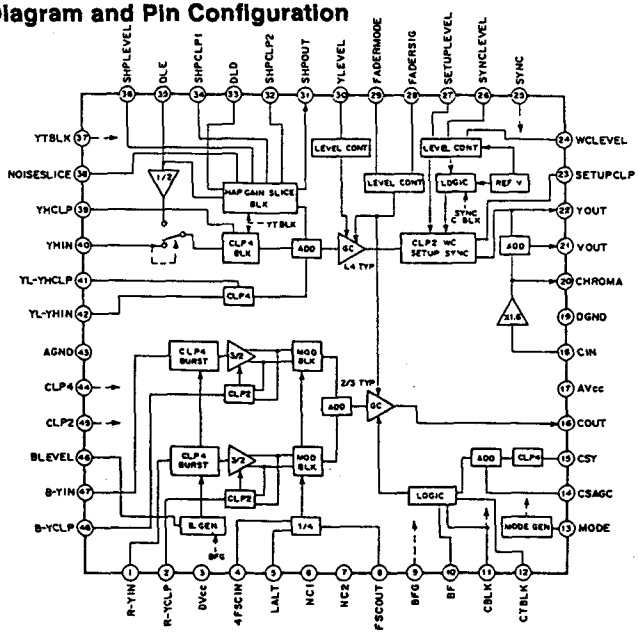
Operating Conditions

• Supply voltage	Vcc	4.75 to 5.25	V
• Ambient temperature	Topr	−20 to +75	°C

Absolute Maximum Ratings (Ta=25°C)

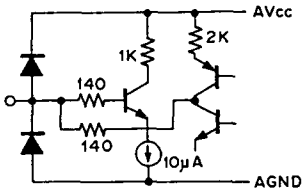
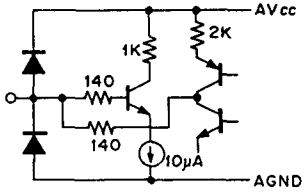
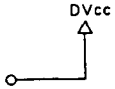
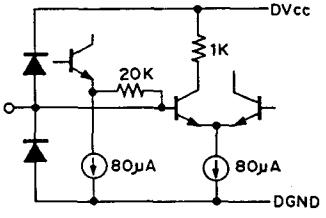
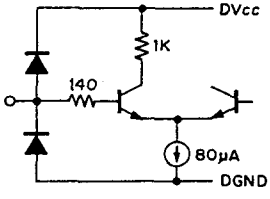
• Supply voltage	Vcc	7	V
• Storage temperature	Tstg	−65 to +150	°C
• Allowable power dissipation	PD	600	mW

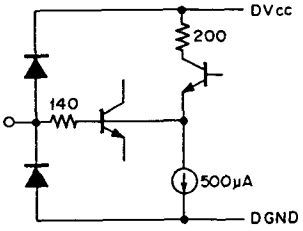
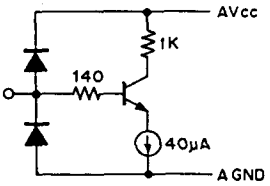
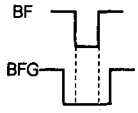
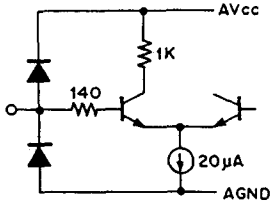
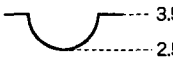
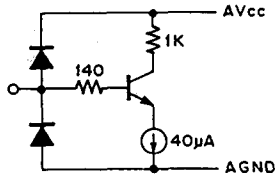
Block Diagram and Pin Configuration

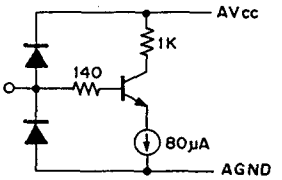
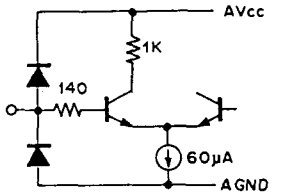
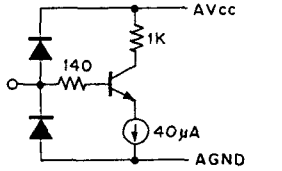
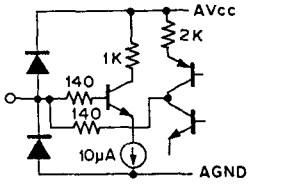
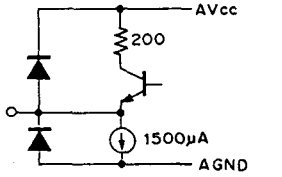


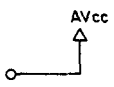
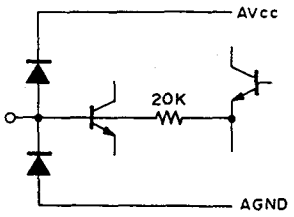
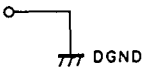
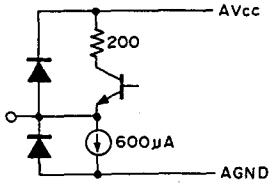
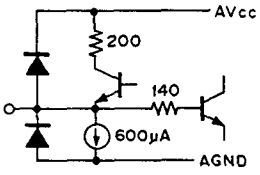
E91537 – ST

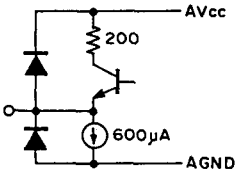
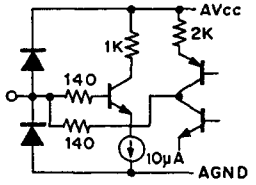
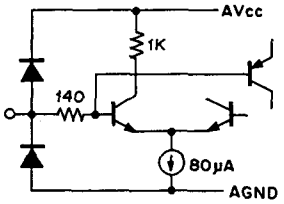
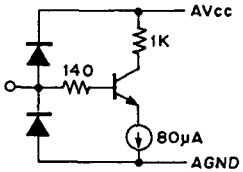
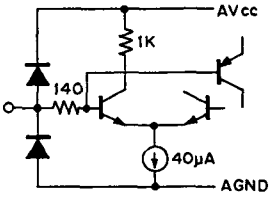
Pin Description

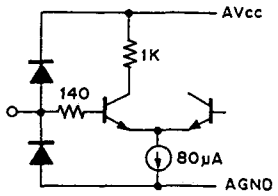
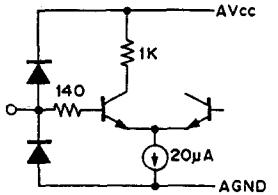
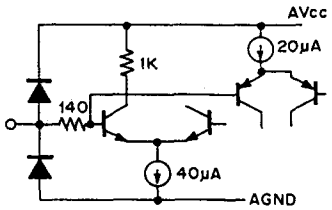
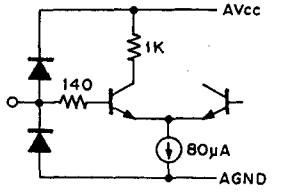
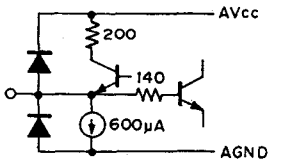
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	R–Y IN	3V		R–Y signal input pin. Clamped internally through C cut input.
2	R–Y CLP	3.4V		Pin connecting the capacitor for R–Y modulator clamp. Setting the capacitance to too small a value will enlarge the carrier leak. 0.1 μF and above is recommended.
3	DVcc	5V		Power supply pin for the 1/4 counter block.
4	4FSCIN	14.32MHz 1Vpp DC2.5V		Input pin for the 4FSC used to make up the Sub Carrier. Input through C cut. Set amplitude to over 500mVp-p.
5	LALT	0V		Input pin for Line Alternate signal during PAL mode. V_{TH} is at 2.5V. Input a pulse with an amplitude larger than $V_{TH} \pm 0.5V$. Set to GND during NTSC mode.

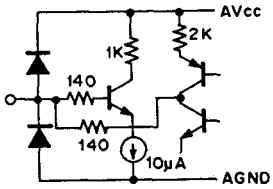
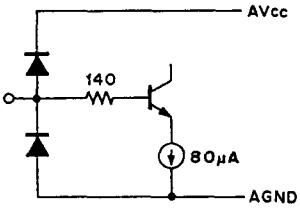
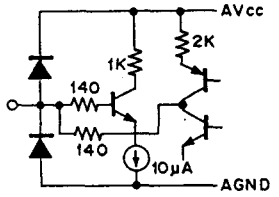
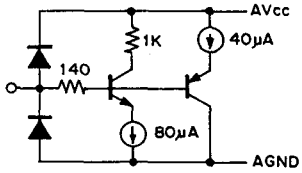
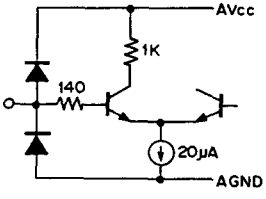
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
6	NC1	—		Not for use. Keep open.
7	NC2	—		Not for use. Keep open.
8	FSCOUT	5V		Outputs a sub carrier with the same phase as B–Y. When not in use, connection to Vcc prevents output and allows for 600 μA of current saving. Determining phase to 4FSC is impossible.
9	BFG			Inserts a pulse slightly larger than BF on both ends.  V_{TH} is at 2.5V. Input a pulse with an amplitude larger than $V_{TH} \pm 0.5V$.
10	BF			Inputs BF (burst flag) pulse. During analog burst, the input pulse smoothens the waveform. The input pulse waveform becomes the envelope of the analog burst waveform.  During the usual burst, be sure to input the pulse.
11	CBLK			Inputs CBLK (composite blanking) pulse. V_{TH} is at 2.5V. Input a pulse with an amplitude larger than $V_{TH} \pm 0.5V$.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
12	CTBLK	5V 0V		Inputs CT (chroma titler) pulse. This signal prevents the application of chroma suppress during the titler signal period. V_{TH} is at 2.5V. Input a pulse with an amplitude larger than $V_{TH} \pm 0.5V$.
13	MODE	0V		Selects NTSC, PAL or NTSC ×2, PAL×2 modes. 0V : NTSC×1 Normal burst 2.5V : NTSC×2 Analog burst 3.5V : PAL×2 Analog burst 5V : PAL×1 Normal burst
14	CSAGC	0V		Suppresses chroma signal at the AGC gain control signal. 3V (100%) to 4.2V (50%)
15	CSY	2.4V		Suppresses chroma signal at the Y signal. 200mV (100%) to 700mV (0%) Inputs at C cut. Clamped internally.
16	COUT	2.8V		Chroma signal output pin. Output as rectangular waves.

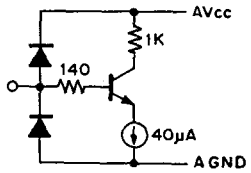
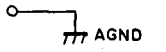
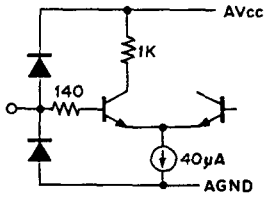
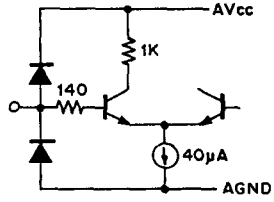
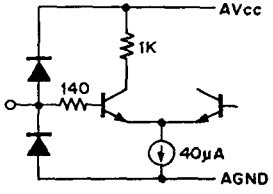
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
17	AVcc	5V		Power supply pin for other than 1/4 counter block.
18	CIN	2.5V		Input pin for chroma signal passed through BPF. Internally biased with a 20kΩ resistance. Input at C cut.
19	DGND	0V		GND pin for 1/4 counter block.
20	CHROMA	2V		Signals input from CIN are amplified and output through this pin. Chroma signal output pin when used for Y/C separation output.
21	VOUT	1.8V		Output pin of composite video signal. When not in use, connection to Vcc allows for 900 μA of current saving.

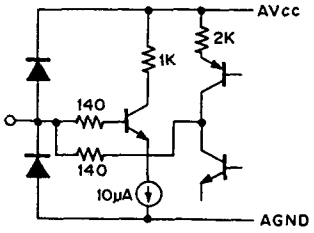
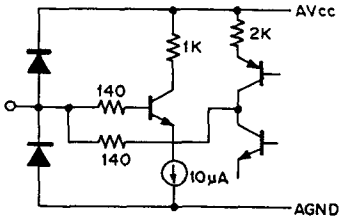
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
22	YOUT	2.4V		Y signal output pin when used for Y/C separation output.
23	SETUPCLP	3.3V		Connecting pin for the white clip clamp capacitor. Over 0.1 µF is recommended.
24	WC LEVEL	3.4V		White clip level control pin. 1.6V (550mV) to 5V (1110mV)
25	SYNC			Sync pulse input pin. V_{TH} is at 2.5V. Input a pulse with an amplitude larger than $V_{TH} \pm 0.5V$.
26	SYNC LEVEL	0V		Sync level control pin. 1.6V (180mV) to 5V (380mV) 0V (287mV) preset.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
27	SETUP LEVEL	3.5V		Set up level control pin. 2.4V (0mV) to 5V (120mV)
28	FADER SIG	0V		Controls the signal suppress level during Black Fader. Controls the signal suppress level during White Fader and at the same time controls the set up level. Signal suppress control: 2V (100%) to 2.9V (0%) Set up level control: 2V (0%) to 2.9V (100%) Black Fader/White Fader mode selection executed through Fader Mode pin.
29	FADER MODE	3.5V		Black Fader and White Fader mode select pin. Also controls the final value (100%) of White Fader white level (set up level). 0V (Black Fader) 1.8V (100mV) to 5V (630mV) (White Fader)
30	Y LEVEL	3.4V		Y signal level control pin. 1.6V (–3.5dB) to 5V (9dB)
31	SHP OUT	3V		Aperture signal output pin. When not in use, connection to Vcc allows for 700 µA of current saving.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
32	SHPCLP2	3.2V		Connects the clamp capacitor used for the slice of the aperture signal.
33	DLD	2.1V		Connects the delay line drive side of the aperture signal.
34	SHPCLP1	3.2V		Connects the clamp capacitor used for the slice of the aperture signal.
35	DLE	2.1V		Connects the delay line end side of the aperture signal. When this pin signals are used as Y_H signals, Y_H IN pin is connected to Vcc.
36	SHP LEVEL	3.5V		Control pin of the aperture signal level. 2.6V (8dB) to 4.2V (−31dB).

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
37	YTBLK	5V 0V	AVcc 1K 140 80μA AGND	Inputs Y_T (Y titler) pulse. V_{TH} is at 2.5V. Input a pulse with an amplitude larger than $V_{TH} \pm 0.5V$.
38	NOISESLICE	3.5V	AVcc 1K 140 40μA AGND	Controls the slice level of the aperture signal. 1.8V (0mV) to 5V (75mV)
39	YHCLP	2.7V	AVcc 2K 1K 140 140 40μA AGND	Connects the capacitor for Y_H input clamp.
40	YHIN	500mV 1.05V	AVcc 20μA 1K 140 40μA AGND	Y_H signal input pin. When DLE pin signal is set as Y_H signal, connect this pin to Vcc. The input signal DC clamp range stands at $1.05V \pm 0.65V$. The standard signal level is at 500mV.
41	YL–YHCLP	3.4V	AVcc 2K 1K 140 140 10μA AGND	Connects the capacitor for Y_L–Y_H input clamp.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
42	YL-YH IN	2.8V		Inputs V aperture signals, titler signals and Y_L-Y_H signals. The input signal DC clamp range stands at 2.8V ± 1.1V.
43	AGND	0V		GND pin for other than 1/4 counter block.
44	CLP4			CLP4 pulse input pin. V_{TH} is at 2.5V. Input a pulse with an amplitude larger than V_{TH} ± 0.5V.
45	CLP2			CLP2 pulse input pin. V_{TH} is at 2.5V. Input a pulse with an amplitude larger than V_{TH} ± 0.5V.
46	B LEVEL	3.5V		Controls the burst level. 1.6V (95mVp-p) to 5V (280mVp-p) (NTSC pulse burst mode)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
47	B–Y IN	3V		R–Y signal input pin. Clamped internally through C cut input.
48	B–Y CLP	3.4V		Connects the capacitor for B–Y modulator clamp. Setting the capacitance to too small a value will enlarge the carrier leak. Over 0.1 μF is recommended.

Electrical Characteristics

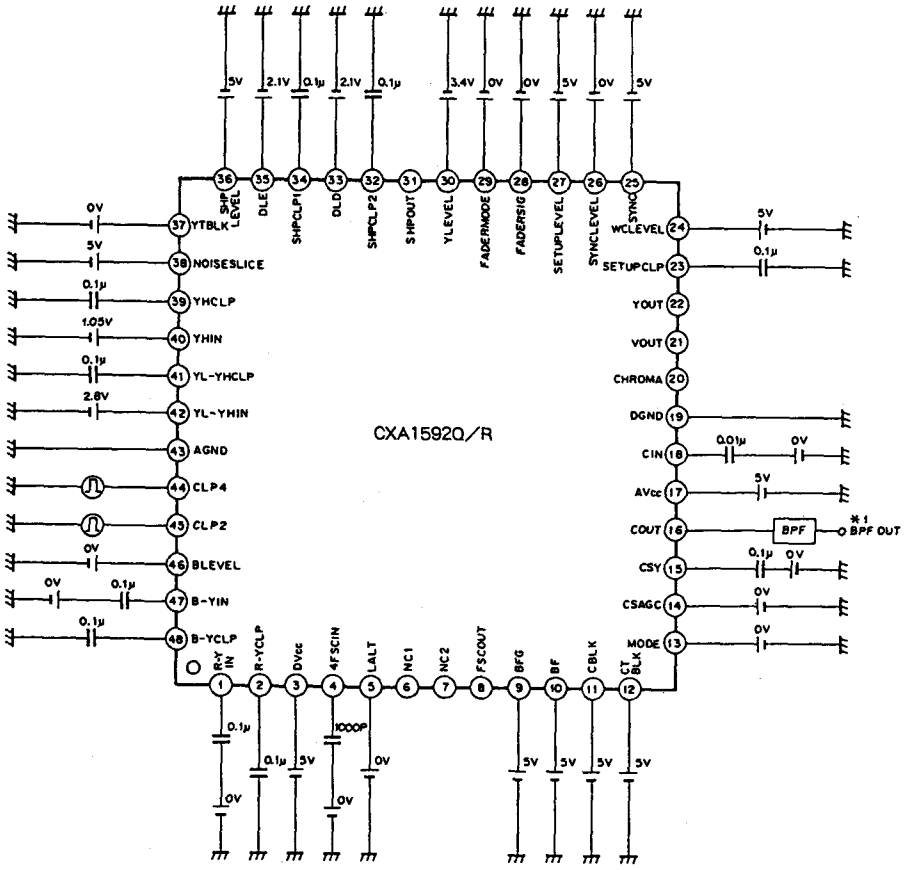
(Vcc=5V, Ta=25℃)

No.	Item	Symbol	Conditions	Min	Typ.	Max.	Unit
1	Current Supply	Icc	AVcc+DVcc	19	28	38	mA
2	YH GAIN TYP	YHTYP	FSCOUT=5V VOUT=5V SHPOUT=5V YHIN (500mV pulse) → YOUT	1.8	2.8	3.8	dB
3	YH GAIN MIN	YHMIN	YHIN (500mV pulse) → YOUT YLEVEL=1.6V	—	–4	–2	dB
4	YH GAIN MAX	YHMAX	YHIN (250mV pulse) → YOUT YLEVEL=5V	8	9.1	—	dB
5	YL-YH GAIN	YL-YH	Y_{L}-Y_{H}IN (500mV pulse) → YOUT	1.8	2.8	3.8	dB
6	DLE GAIN	DLE	DLE (1V pulse) → YOUT YHIN=5V	–4.3	–3.3	–2.3	dB
7	VOUT GAIN	VOUT	YHIN (500mV pulse) → VOUT	1.3	2.3	3.3	dB
8	WHITE FADER MIN	WFMIN	CBLK pulse FADERMODE=1.6V WFMIN=YOUT output level –SETMAX (No.13)	68	86	104	mV
9	WHITE FADER MAX	WFMAX	CBLK pulse FADERMODE=5V WFMAX=YOUT output level –SETMAX (No.13)	527	620	713	mV
10	WHITE CLIP MIN	WCMIN	YHIN (500mV pulse) → YOUT CBLK pulse WCLEVEL=1.6V	522	550	578	mV
11	WHITE CLIP MAX	WCMAX	YHIN (500mV pulse) → YOUT CBLK pulse WCLEVEL=5V	1056	1112	1168	mV
12	WHITE CLIP PRESET	WCPRE	YHIN (500mV pulse) → YOUT CBLK pulse WCLEVEL=0V	796	838	880	mV
13	SETUP MAX	SETMAX	CBLK pulse → YOUT SETUPLEVEL=5V	113	126	139	mV
14	SYNC MIN	SYNCMIN	SYNC pulse → YOUT SYNCLEVEL=1.6V	165	180	195	mV
15	SYNC MAX	SYNCMAX	SYNC pulse → YOUT SYNCLEVEL=5V	363	383	403	mV
16	SYNC PRESET	SYNCPRE	SYNC pulse → YOUT SYNCLEVEL=0V	272	287	302	mV
17	SHP-YOUT GAIN	SHPYOUT	DLD (40mV pulse) → YOUT SHPLEVEL=2.6V YHIN (500mV pulse)	6	8	10	dB
18	SHP DOWN MIN	SHPMIN	DLD (40mV pulse) → SHPOUT SHPLEVEL=4.2V	—	–25	–5.5	dB
19	SHP DOWN TYP	SHPTYP	DLD (40mV pulse) → SHPOUT SHPLEVEL=3.4V	–0.5	1	2.5	dB
20	SHP DOWN MAX	SHPMAX	DLD (40mV pulse) → SHPOUT… (DOWNMAX) SHPLEVEL=2.6V	5.7	7.2	8.7	dB
21	SHP DOWN/UP	SHPD/U	DLE (40mV pulse) → SHPOUT… (UPMAX) SHPLEVEL=2.6V SHPD/U=DOWNMAX/UPMAX	0.8	1	1.2	times
22	SHP SLICE MAX	SLICEMAX	DLD (40mV pulse) → SHPOUT… (SLMAX) SHPLEVEL=2.6V NOISE SLICE=0V SLICEMAX=DOWNMAX-SLMAX	60	75	90	mV
23	B–Y GAIN	B–Y	B–YIN (300mV pulse) → BPFOUT 4FSCIN=SIN 1Vp-p 14.32MHz B–Y=20log {BPFOUT (mVp-p)/300mV}	0.4	1.6	2.8	dB

No.	Item	Symbol	Conditions	Min	Typ.	Max.	Unit
24	R–Y GAIN	R–Y	R–YIN (300mV pulse) →BPFOUT ...(R-Y level) 4FSCIN =SIN 1Vp-p 14.32MHz R-Y=20log {BPFOUT (mVp-p)/300mV}	0.4	1.6	2.8	dB
25	CARRIER LEAK 3.58MHz	L358	4FSCIN=SIN 1Vp-p 14.32MHz L358= 20log {286mVp-p/BPFOUT level (mVp-p)} BURST (Typ.)	36	48	—	dB
26	CARRIER LEAK 500kHz	L500	4FSCIN=SIN 1Vp-p 2MHz L500= 20log {286mVp-p/BPFOUT level (mVp-p)} BURST (Typ.)	36	58	—	dB
27	COUT DRANGE	COUTD	R-YIN (600mV pulse) → BPFOUT 4FSCIN=SIN 1Vp-p 14.32MHz	670	730	—	mV
28	CS AGC MAX	CSAGCMAX	R-YIN (300mV pulse) → BPFOUT 4FSCIN=SIN 1Vp-p 14.32MHz CSAGC=4.2V CSAGCMAX=(BPFOUT level/R–Y level) ×100%	47	52	57	%
29	FSCOUT amplitude	FSC	FSCOUT DC amplitude at 4FSCIN=2V, 3V	585	673	760	mV
30	BURST NTSC MIN	NTMIN	BFG pulse → BPFOUT BLEVEL=1.6V 4FSCIN=SIN 1Vp-p 14.32MHz	80	95	110	mV
31	BURST NTSC MAX	NTMAX	BFG pulse → BPFOUT BLEVEL=5V 4FSCIN=SIN 1Vp-p 14.32MHz	250	280	312	mV
32	BURST PAL MIN	PALMIN	BFG pulse → BPFOUT BLEVEL=1.6V MODE=5V 4FSCIN=SIN 1Vp-p 14.32MHz	89	105	120	mV
33	BURST PAL MAX	PALMAX	BFG pulse → BPFOUT BLEVEL=5V MODE=5V 4FSCIN=SIN 1Vp-p 14.32MHz	283	316	350	mV
34	BURST NTSC×2 MIN	NT2MIN	BFG pulse → BPFOUT BLEVEL=1.6V MODE=2.5V 4FSCIN=SIN 1Vp-p 14.32MHz	153	180	207	mV
35	BURST NTSC×2 MAX	NT2MAX	BFG pulse → BPFOUT BLEVEL=5V MODE=2.5V 4FSCIN=SIN 1Vp-p 14.32MHz	468	520	572	mV
36	BURST PAL×2 MIN	PAL2MIN	BFG pulse → BPFOUT BLEVEL=1.6V MODE=3.5V 4FSCIN=SIN 1Vp-p 14.32MHz	171	202	232	mV
37	BURST PAL×2 MAX	PAL2MAX	BFG pulse → BPFOUT BLEVEL=5V MODE=3.5V 4FSCIN=SIN 1Vp-p 14.32MHz	535	595	655	mV
38	CIN-VOUT GAIN	CINVOUT	CIN (SIN 400mVp-p 3.58MHz) → VOUT	2.5	3.5	4.5	dB
39	CIN-CHROMA GAIN	CINCHROMA	CIN (SIN 400mVp-p 3.58MHz) → CHROMA	2.1	3.1	4.1	dB

Ref.) YHIN → Y OUT Frequency characteristics gain 10MHz, –2.3dB (Typ.)

Test Circuit



Above conditions are given as the typical setting. The individual conditions of each item are indicated in the chart.

*1 For BPF characteristics proceed as follows.

① When 4FSC IN=14.32MHz use a 3.58MHz band pass filter where through the input of a 3.58MHz sine wave a ratio of 2 to 1 is obtained for the input vs. output.

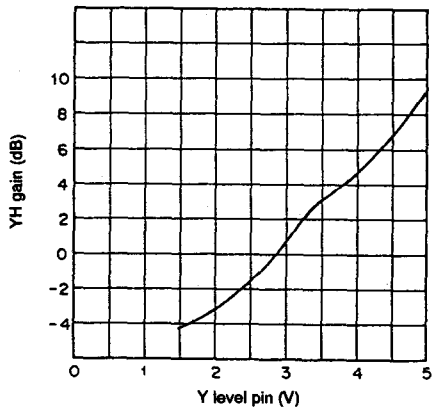
② When 4FSC IN=2MHz, use a 500kHz band pass filter where through the input of a 500kHz sine wave a ratio of 2 to 1 is obtained for the input vs. output.

Input Signal Timing Chart

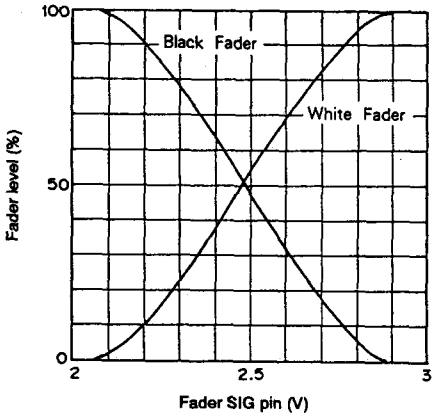
Pin name	Input signal
	0 10 20 30 40 50 60 (μsec)
45. CLP2	5V 0V, 2 μsec
44. CLP4	5V 0V, 2 μsec
11. CBLK	5V 0V
25. SYNC	5V 0V
9. BFG	5V 0V
40. YH	1.05V, ※
42. YL-YH	2.8V, ※
33. DLD	2.1V, ※
35. DLE	2.1V, ※
37. YTBLK	5V 0V
12. CTBLK	5V 0V
15. CSY	0V, ※
1. R–Y	0V, ※
48. B–Y	0V, ※

Note) Level is indicated in the conditions shown in the chart.

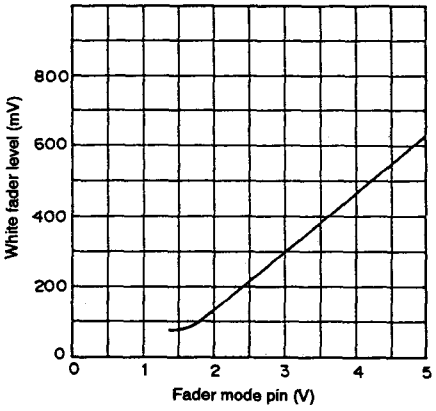
YH Gain control characteristics



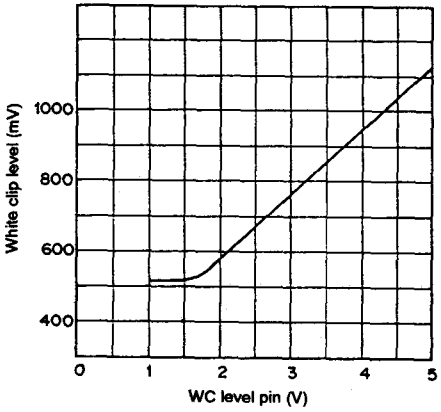
Y fader control characteristics



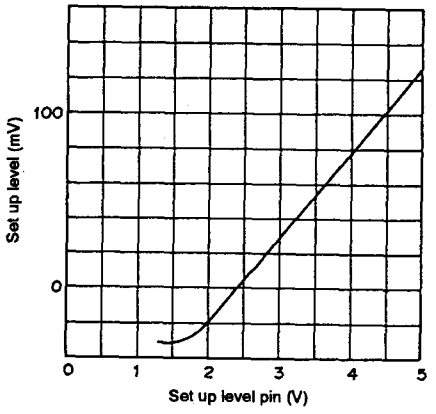
White fader control characteristics



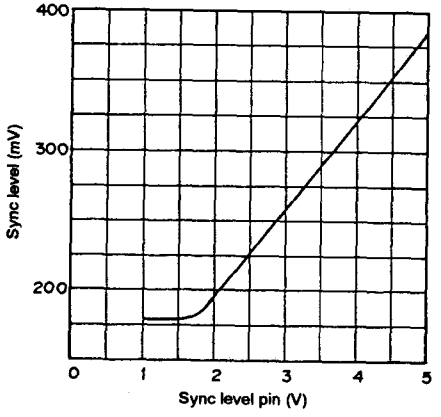
White clip control characteristics



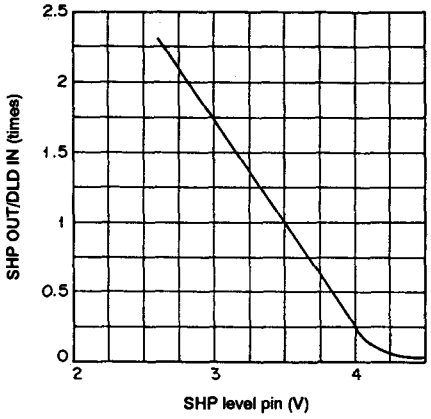
Set up level control characteristics



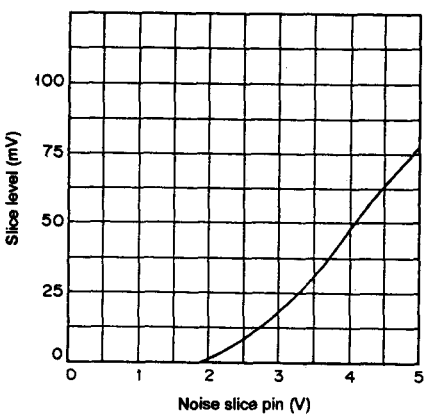
Sync level control characteristics



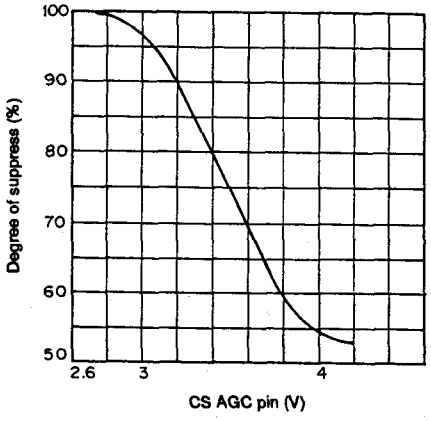
SHP gain control characteristics



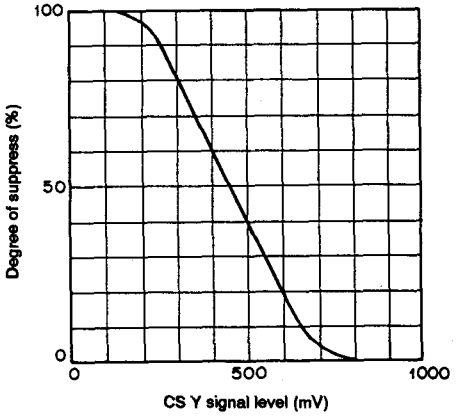
SHP noise slice characteristics



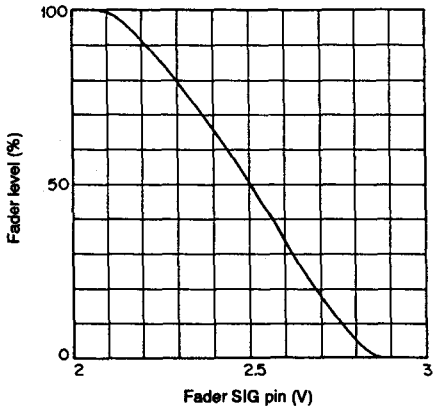
CS AGC control characteristics



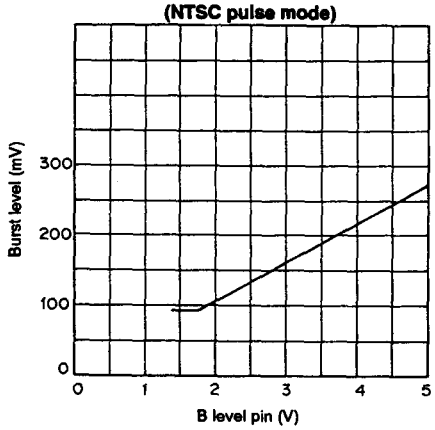
CS Y control characteristics



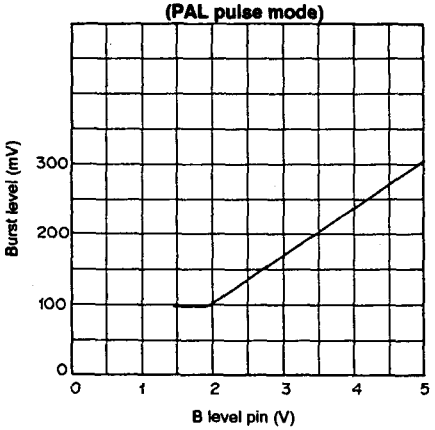
Chroma fader control characteristics



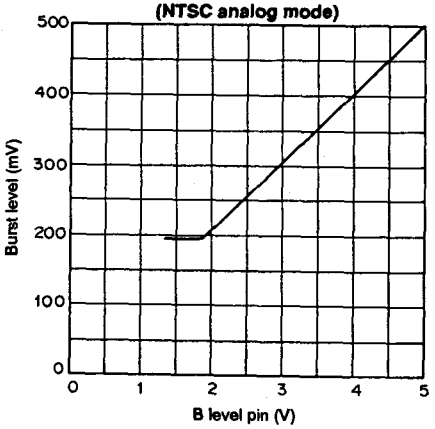
Burst level control characteristics (NTSC pulse mode)



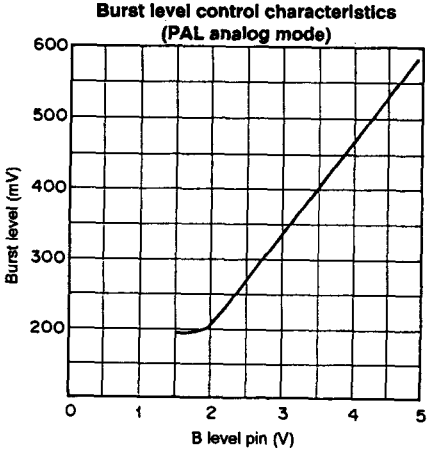
Burst level control characteristics (PAL pulse mode)



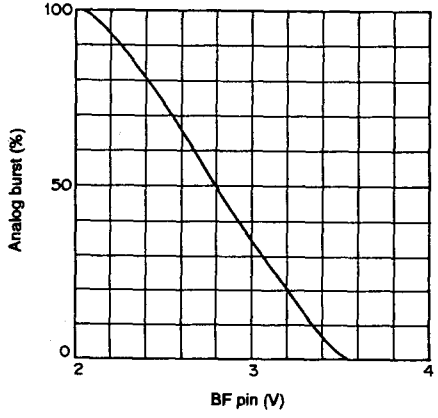
Burst level control characteristics (NTSC analog mode)



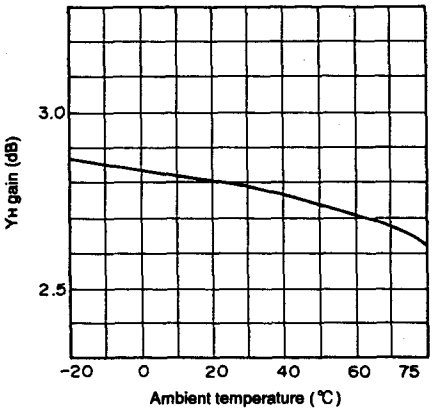
Burst level control characteristics (PAL analog mode)



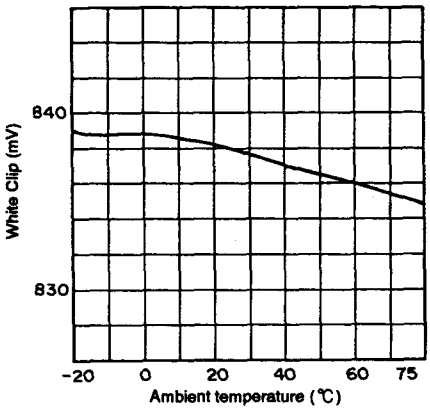
Analog burst control



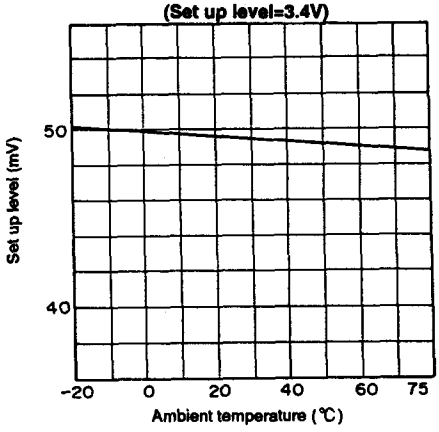
Y_H gain typical temperature characteristics



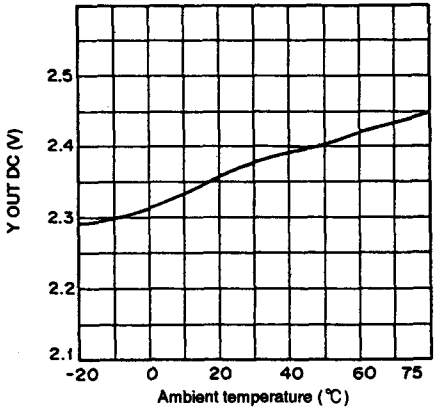
White clip preset temperature characteristics



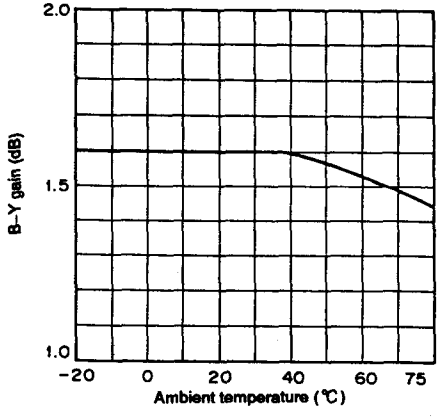
Set up level temperature characteristics (Set up level=3.4V)



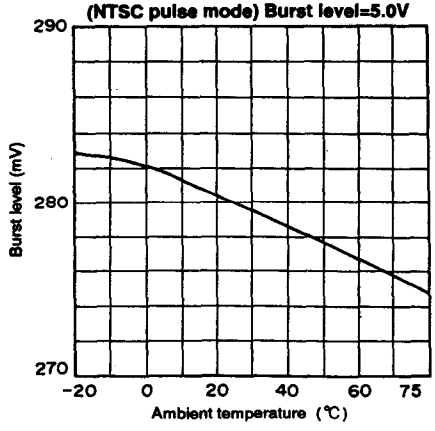
Y OUT DC temperature characteristics



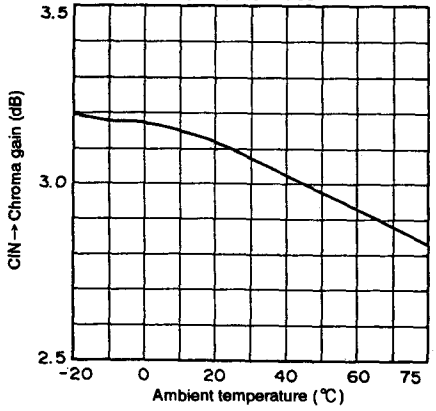
B–Y gain temperature characteristics



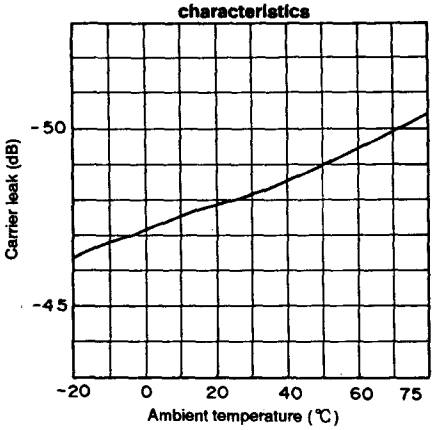
Burst NTSC maximum temperature characteristics (NTSC pulse mode) Burst level=5.0V



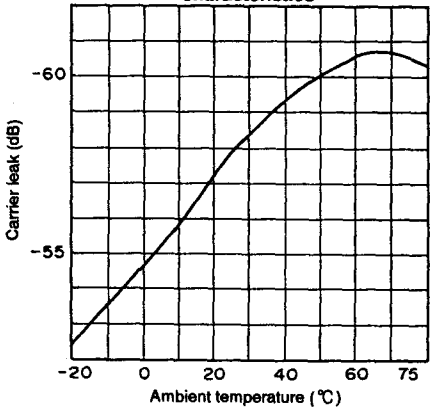
CIN → Chroma gain temperature characteristics



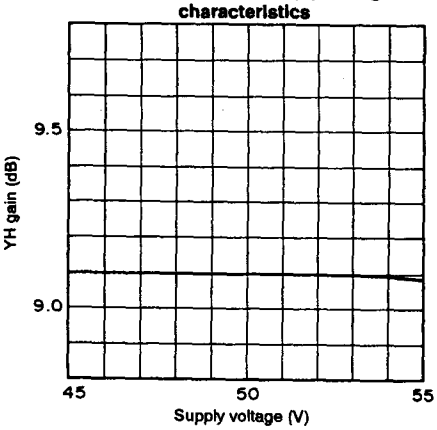
Carrier leak 3.58 MHz temperature characteristics



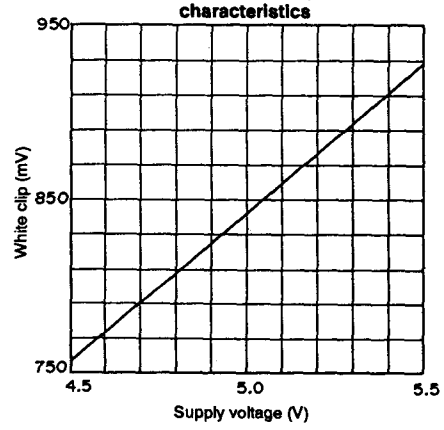
Carrier leak 500 kHz temperature characteristics



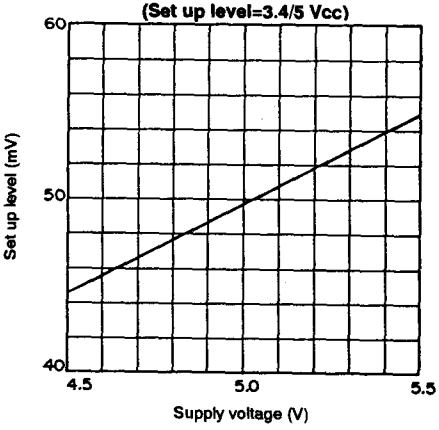
YH gain maximum supply voltage characteristics



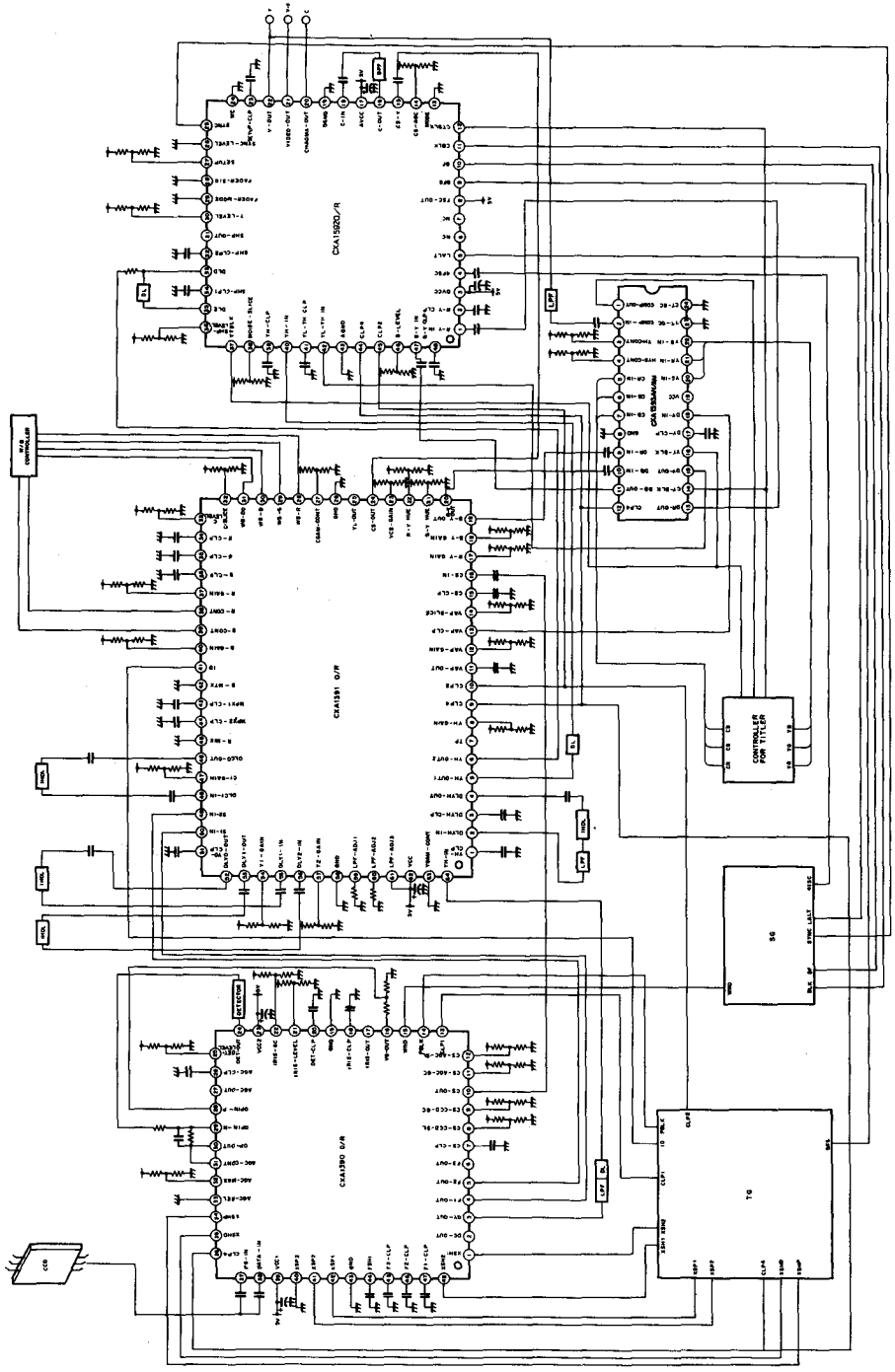
White clip preset supply voltage characteristics



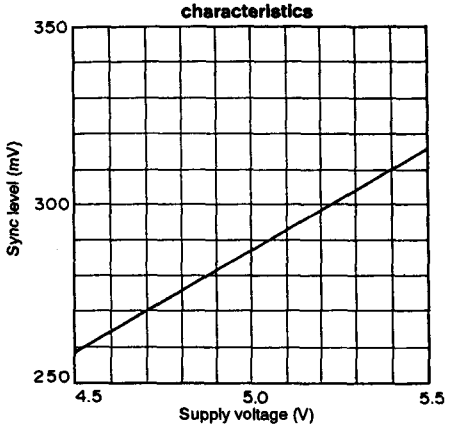
Set up level supply voltage characteristics (Set up level=3.4/5 Vcc)



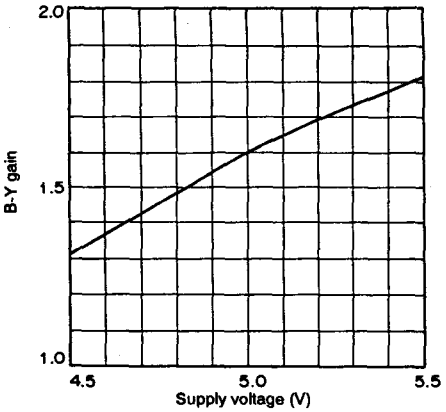
CXA1390 Series System Diagram



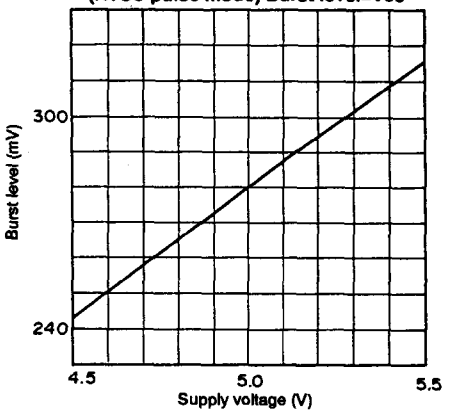
Sync level preset supply voltage characteristics



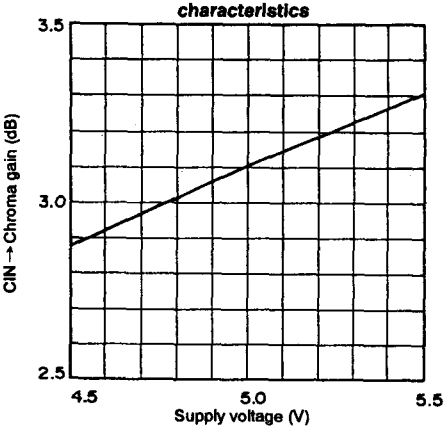
B–Y gain supply voltage characteristics



Burst level supply voltage characteristics (NTSC pulse mode) Burst level=Vcc

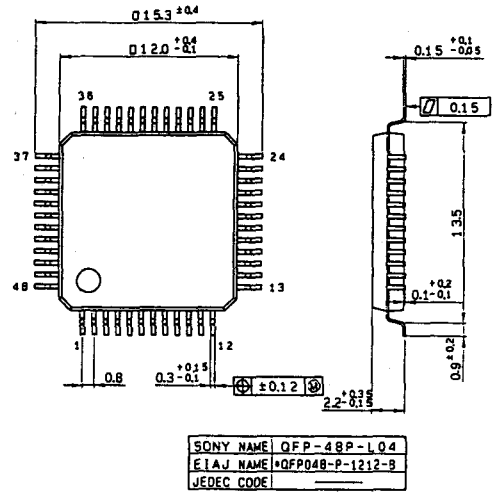


CIN → Chroma gain supply voltage characteristics

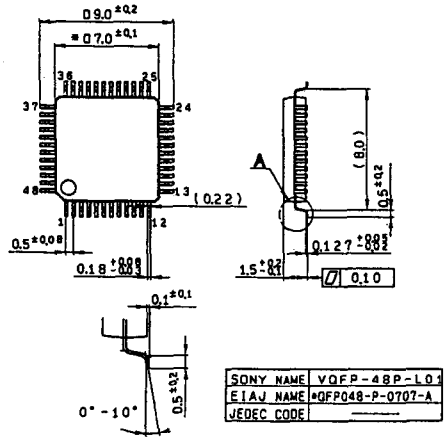


Package Outline Unit : mm

CXA1592Q 48 pin QFP (Plastic) 0.6g



CXA1592R 48 pin VQFP (Plastic) 0.2g



Detailed diagram of A

Note) Dimensions marked with *
does not include resin residue

SONY

CXA1393AN/AM

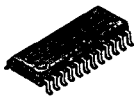
Titler IC for Camera

Description

The CXA1393AN/AM is a title insertion IC for video cameras.

CXA1393AN
24 pin VSOP (Plastic)

CXA1393AM
24 pin SOP (Plastic)



Features

- External parts are integrated in the IC to reduce peripherals.
- Hysteresis volume of the built-in comparator is variable.
- The gain of the Title signal is variable.

Applications

Titler IC for video cameras

Operating Conditions

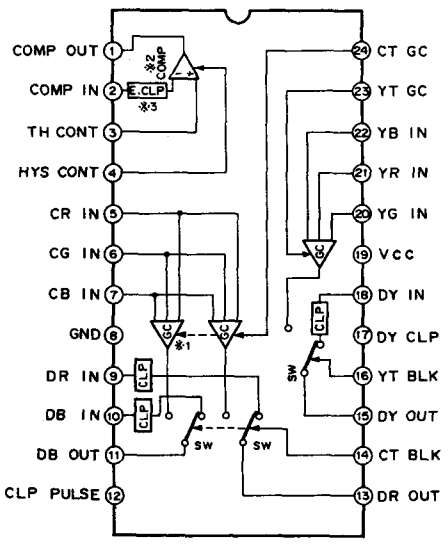
• Supply voltage	Vcc	4.75 to 5.25	V
• Ambient temperature	Topr	−20 to +75	℃

Absolute Maximum Ratings (Ta = 25℃)

• Supply voltage	Vcc	7	V
• Ambient temperature	Topr	−20 to +75	℃
• Storage temperature	Tstg	−65 to +150	℃
• Allowable power dissipation	PD	470	mW (CXA1393AN)
		830	mW (CXA1393AM)

Block Diagram and Pin Configuration

(Top View)



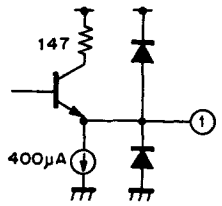
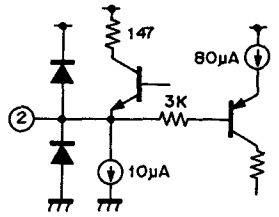
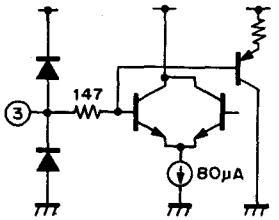
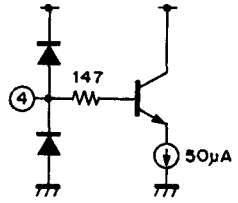
※1 GC
GAIN CONTROL AMP

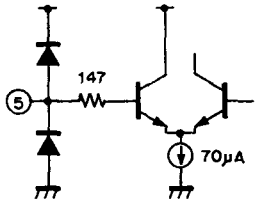
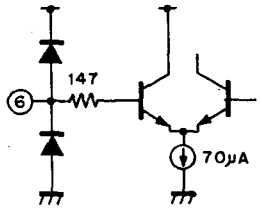
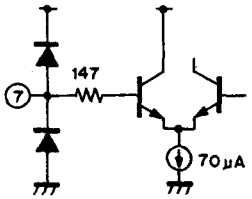
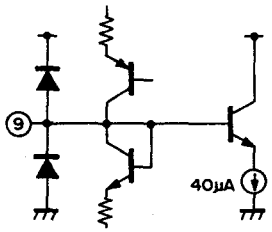
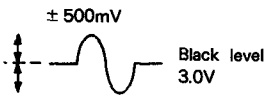
※2 COMP
COMPARATOR

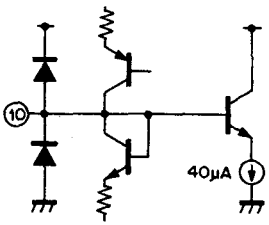
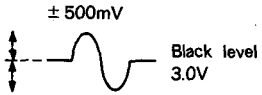
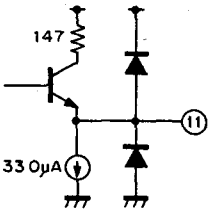
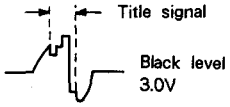
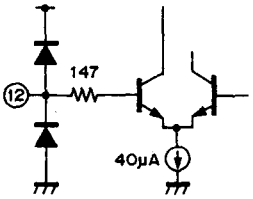
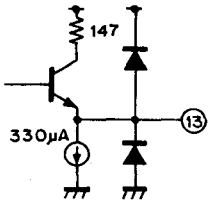
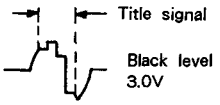
※3 E.CLP
EMITTER CLAMP

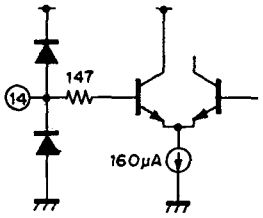
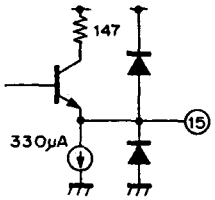
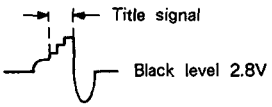
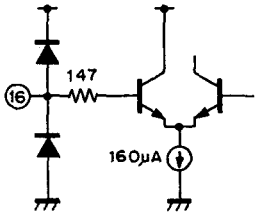
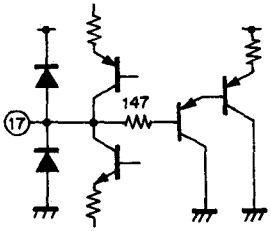
E89Z19 – ST

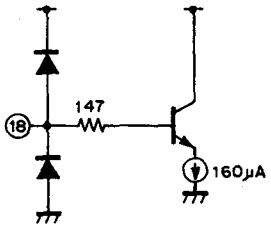
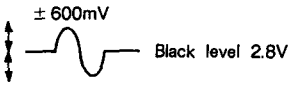
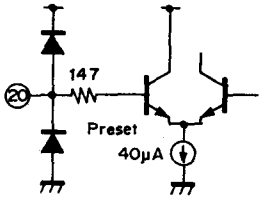
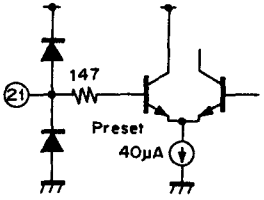
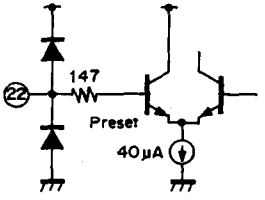
Pin Description

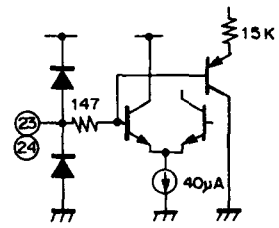
Pin No.	Symbol	Voltage	Equivalent circuit	Description
1	COMP OUT	L : below 0.2Vcc H : above 0.7Vcc		Comparator output pin.
2	COMP IN	approx. 2.1V		Comparator inverted input pin. Clamps Sync Tip inside C-Cut input. (Sync Tip approx. 2.1V) 160IRE (Max.)
3	TH CONT	TH OFF 0V Control 2 to 5V		Comparator threshold adjusting pin. (Non-inverted input pin) 2 to 5V 300 to 1000mV
4	HYS CONT	Control 2 to 5V		Comparator hysteresis adjusting pin. 2 to 5V 150 to 20mV

Pin No.	Symbol	Voltage	Equivalent circuit	Description
5	CR IN	—		Red signal input pin for chroma Title. TH = 2.5V (active H)
6	CG IN	—		Green signal input pin for chroma Title. TH = 2.5V (active H)
7	CB IN	—		Blue signal input pin for chroma Title. TH = 2.5V (active H)
8	GND	GND		
9	DR IN	Input clamp voltage Black level 3.0V		Input pin for main line R − Y signal. Clamps inside C-Cut input. 

Pin No.	Symbol	Voltage	Equivalent circuit	Description
10	DB IN	Input clamp voltage Black level 3.0V		Input pin for main line B−Y signal. Clamps inside C-Cut input. 
11	DB OUT	Black level 3.0V		Output pin for main line B−Y signal + Title signal. 
12	CLP Pulse	—		CLP pulse input pin. TH = 2.5V (active H)
13	DR OUT	Black level 3.0V		Output pin for main line R−Y signal + Title signal. 

Pin No.	Symbol	Voltage	Equivalent circuit	Description
14	CT BLK	—		C blanking pulse input pin. TH = 2.5V (active L)
15	DY OUT	Black level 2.8V		Output pin for main line Y signal + Title signal. 
16	YT BLK	—		Input pin for Y blanking pulse. TH = 2.5V (active H)
17	DY CLP			Capacitor connecting pin for Y clamp.

Pin No.	Symbol	Voltage	Equivalent circuit	Description
18	DY IN	Black level 2.8V ± 400mV		Input Pin for main line Y signal. 
19	Vcc	Vcc		
20	YG IN	—		Input pin of green signal for Y Title signal. TH = 2.5V (active H)
21	YR IN	—		Input pin of red signal for Y Title signal. TH = 2.5V (active H)
22	YB IN	—		Input pin of blue signal for Y Title signal. TH = 2.5V (active H)

Pin No.	Symbol	Voltage	Equivalent circuit	Description
23	YT GC	Preset = 0V 2 to 5V		Adjusting pin for Y Title signal gain. 0V : − 0.5dB 2 to 5V − 4 to + 4dB
24	CT GC	Preset = 0V 2 to 5V		Adjusting pin for C Title signal gain. 0V : − 0.5dB 2 to 5V − 3.5 to + 3.8dB

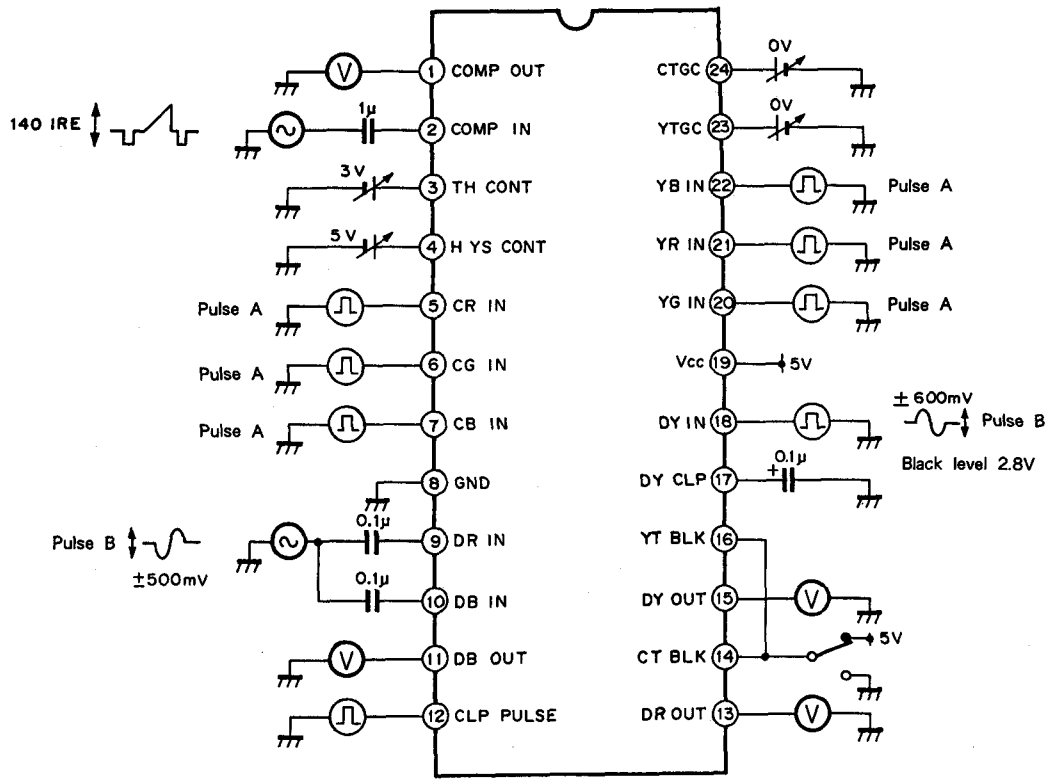
Electrical Characteristics CXA1393AM specifications in brackets ( ).

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption		I_D	⑫ CLP PULSE = 5V	4.5	7.5	11	mA
Y Title signal gain Note 1	fix mode	Y_T FIX	⑮ DY OUT output * 0dB = 340mV	−2	−0.5	1	dB
	min mode	Y_T MIN	⑮ DY OUT output ㉓ YT GC = 1.8V	—	—	−4	dB
	max mode	Y_T MAX	⑮ DY OUT output ㉓ YT GC = 5V	4	—	—	dB
B − Y Title signal gain Note 2	fix mode	DBT FIX	⑪ DB OUT output ⑭ CT BLK = 0V * 0dB = 150mV	−2	−0.5	1	dB
	min mode	DBT MIN	⑪ DB OUT output ⑭ CT BLK = 0V ㉔ CT GC = 1.8V	—	—	−3.5	dB
	max mode	DBT MAX	⑪ DB OUT output ⑭ CT BLK = 0V ㉔ CT GC = 5V	3.8	—	—	dB
R − Y Title signal gain Note 3	fix mode	DRT FIX	⑬ DR OUT output ⑭ CT BLK = 0V * 0dB = 205mV	−2	−0.5	1	dB
	min mode	DRT MIN	⑬ DR OUT output ⑭ CT BLK = 0V ㉔ CT GC = 1.8V	—	—	−3.5	dB
	max mode	DRT MAX	⑬ DR OUT output ⑭ CT BLK = 0V ㉔ CT GC = 5V	3.8	—	—	dB
Y Title signal R, G, B, ratio	R/G	R/G Y	⑮ DY OUT output (Red) ㉑ YR IN ; Pulse A ⑮ DY OUT output (Green) ㉑ YB IN ; Pulse A $R/G\ Y = \frac{⑮\ DY\ OUT\ (Red)}{⑮\ DY\ OUT\ (Green)}$ The other input pin for Y Title signal is GND. Calculation for R, G and B ratio is executed similarly as mentioned above.	0.472	0.5	0.53	—

CXA1393AM specifications in brackets ( ).

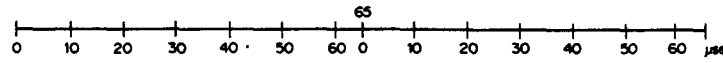
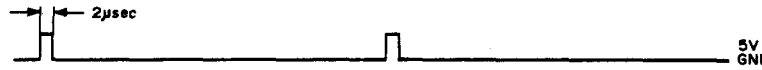
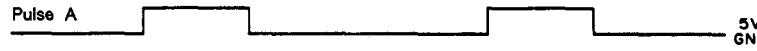
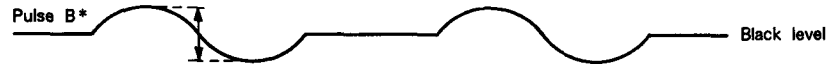
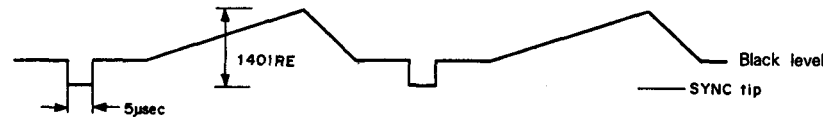
Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Y Title signal R, G, B ratio	B/G	B/G Y	Blue/Green	0.154	0.164	0.177	dB
R−Y Title signal R, G, B ratio	R/G	R/G R	R/G B = ⑬ DR OUT (Red) / ⑬ DR OUT (Green) ⑭ CT BLK = 0V	1.102 (1.05)	1.16	1.236	dB
	B/G	B/G R	Blue/Green ⑭ CT BLK = 0V	0.152 (0.15)	0.163	0.1766	dB
B−Y Title signal R, G, B ratio	R/G	R/G B	R/G B = ⑪ DR OUT (Red) / ⑪ DR OUT (Green) ⑭ CT BLK = 0V	0.472 (0.468)	0.5	0.53 (0.54)	dB
	B/G	B/G B	Blue/Green ⑭ CT BLK = 0V	1.416	1.5	1.589	dB
HYSCOMP		Note 4)	Note 4) TH voltage − CLP voltage = TH volume	—	—	0	IRE
Threshold volume (TH volume)	OFF	TH OFF	① COMP OUT output ③ TH CONT = 0V				
	MID	TH MID	① COMP OUT output ③ TH CONT = 3V	40	50	60	IRE
	MAX	TH MAX	① COMP OUT output ③ TH CONT = 5V	75	85	95	IRE
HYSCOMP output voltage		L level	① COMP OUT output ③ TH CONT = 0V	—	—	0.2Vcc	V
		H level	① COMP OUT output ③ TH CONT = 5V	0.7Vcc	—	—	V

Electrical Characteristics Test Circuit
Standard setting conditions



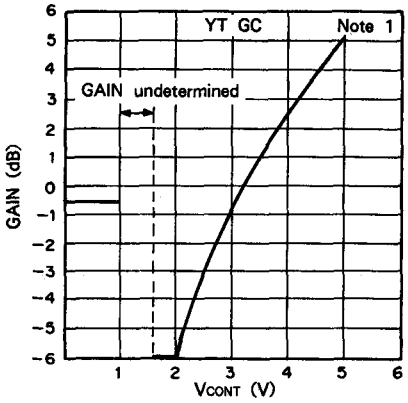
*1 Ⓥ: Voltage waveform test (Both AC and DC)
*2 Standard setting condition voltage for YT BLK and CT BLK pins is 5V.

Input Signal Timing Chart

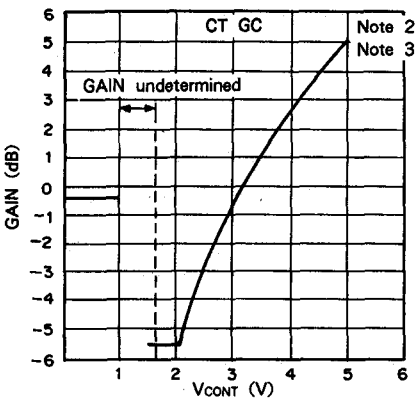
Pin	Input signal
	
⑫ CLP pulse	
⑳ YG IN ㉑ YR IN ㉒ YB IN ⑤ CR IN ⑥ CG IN ⑦ CB IN	
	
⑨ DR IN ⑩ DB IN ⑱ DY IN	
② COMP IN	
	* Refer to the Pin Description.

Vcc = 5V

Y Title signal gain control characteristics

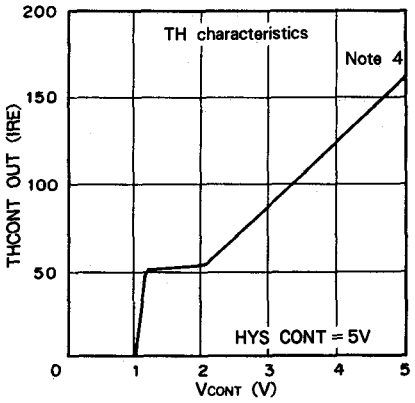


C Title signal gain control characteristics

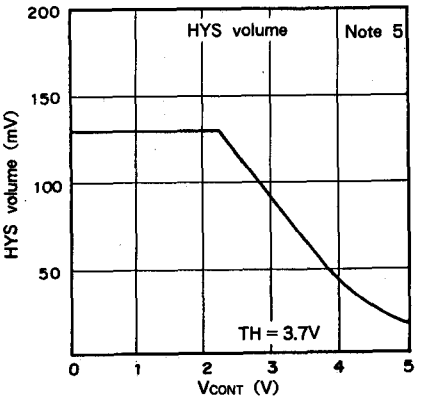


CXA1393A CONT curve data

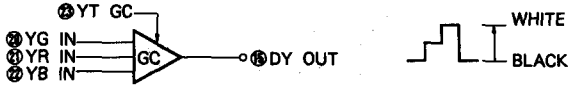
Threshold control characteristics for comparator



Hysteresis control characteristics for comparator

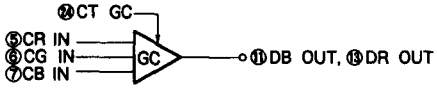


Note 1) | White − Black | = 340mV is taken as 0dB.



When YG IN (Pin 20) is at H, YR IN (Pin 21) is at H and YB IN (Pin 22) is at H, DY OUT (Pin 15) output voltage is White.
When YG IN (Pin 20) is at L, YR IN (Pin 21) is at L and YB IN (Pin 22) is at L, DY OUT (Pin 15) output voltage is Black.

Note 2) | Blue − Black | = 150mV is taken as 0dB.

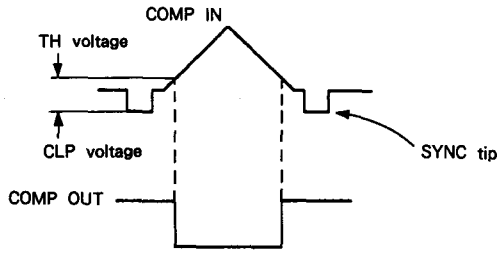


When CR IN (Pin 5) is at L, CG IN (Pin 6) is at L and CB IN (Pin 7) is at H, DB OUT (Pin 11) output voltage is Blue.
When CR IN (Pin 5) is at L, CG IN (Pin 6) is at L and CB IN (Pin 7) is at L, DB OUT (Pin 11) output voltage is Black.

Note 3) | Red − Black | = 205mV is taken as 0dB.

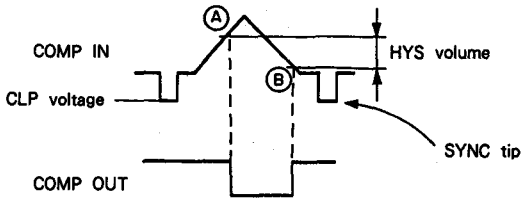
When CR IN (Pin 5) is at H, CG IN (Pin 6) is at L and CB IN (Pin 7) is at L, DR OUT (Pin 13) output voltage is Red.
When CR IN (Pin 5) is at L, CG IN (Pin 6) is at L and CB IN (Pin 7) is at L, DR OUT (Pin 13) output voltage is Black.
Moreover, when the pulse input voltage: L is set to less than 1V and H is set to over 4V.

Note 4)



TH voltage − CLP voltage = TH volume

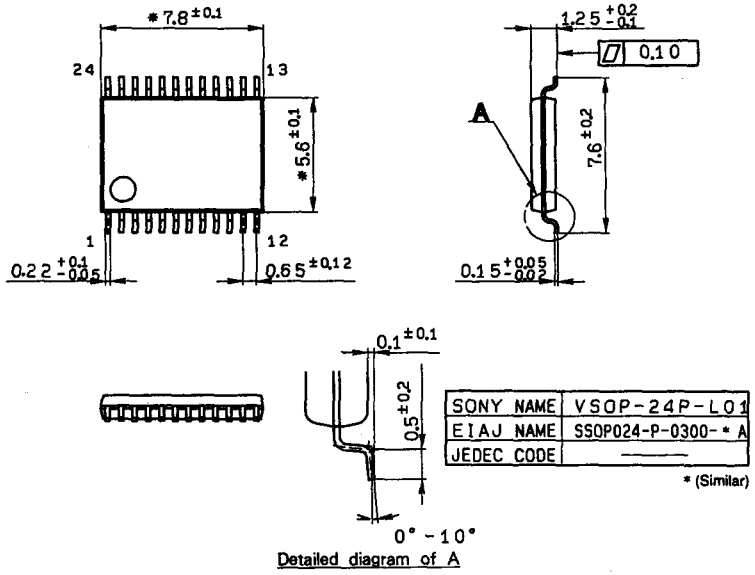
Note 5)



Ⓐ−Ⓑ= HYS volume

Package Outline Unit : mm

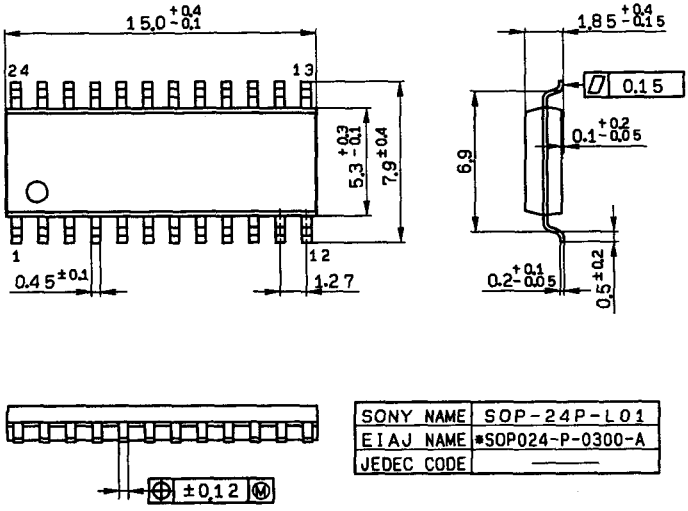
CXA1393AN 24 pin VSOP (Plastic) 300mil



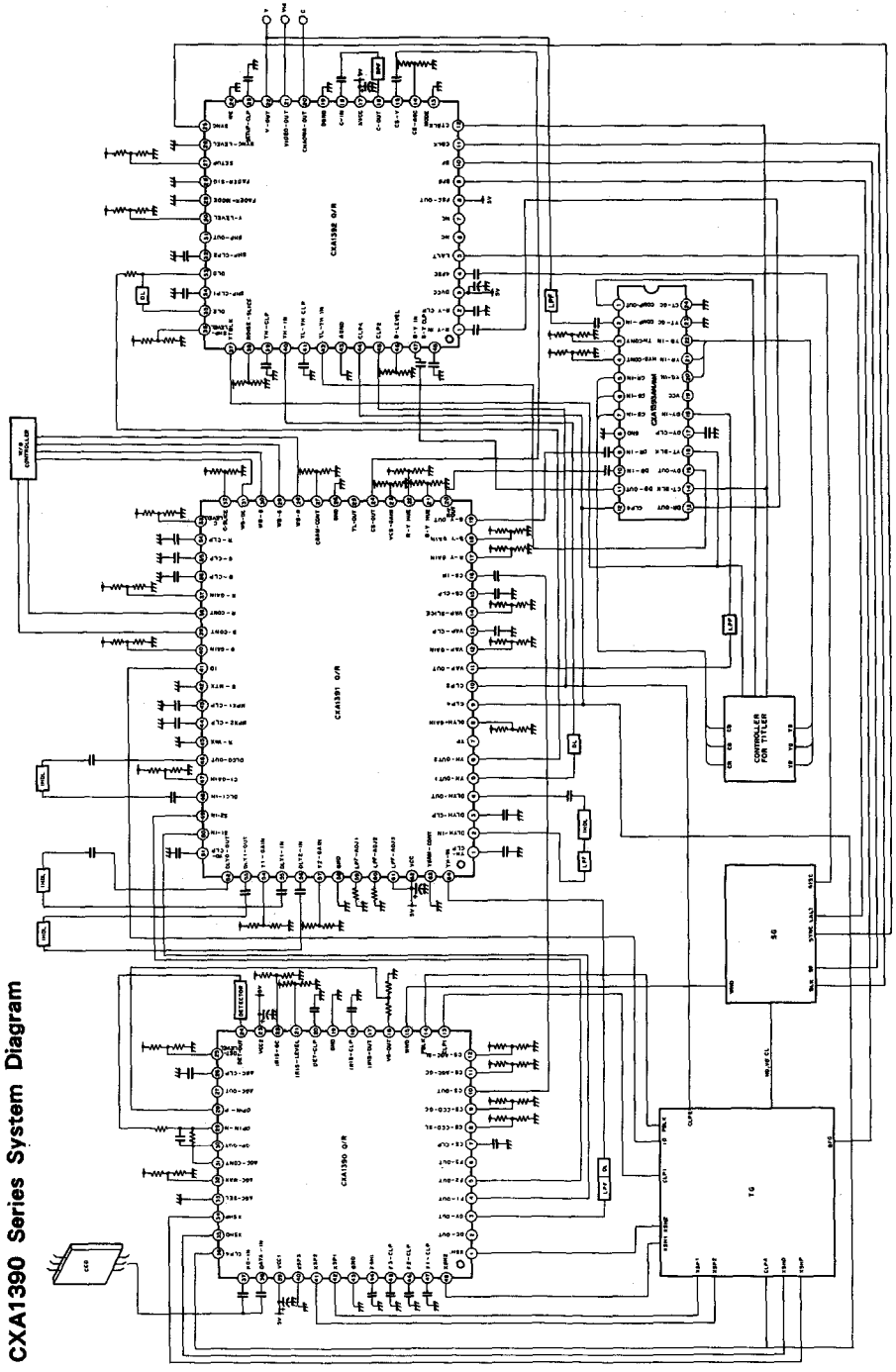
Detailed diagram of A

Note) Dimensions marked with * do not include resin residue.

CXA1393AM 24 pin SOP (Plastic) 300mil 0.3g



CXA1390 Series System Diagram



CDS for CCD camera

Description

The CXA1439M is an IC for CDS (Correlated Double Sampling) to be used in a CCD camera.

Features

- Single power supply (4.8V)
- Low power consumption (57mW)
- Requires less external parts.
- High S/N ratio
- A smaller-size package requiring less mounting space
- Built-in two amplifiers.

Application

CCD camera

Structure

Bipolar silicon monolithic IC

8pin SOP (Plastic)

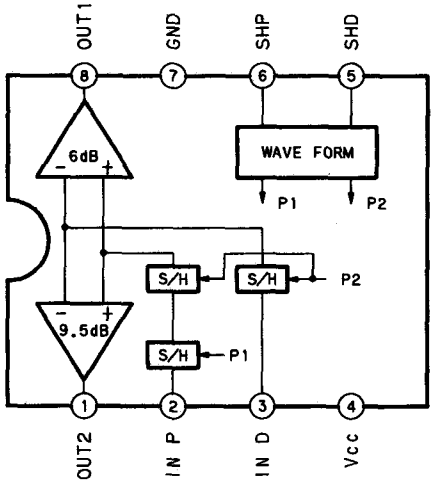
Absolute Maximum Ratings

• Supply voltage	V_{CC}	10	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−60 to +150	°C
• Allowable power dissipation	P_D	300	mW

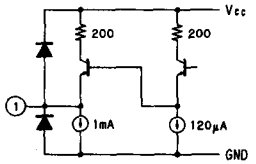
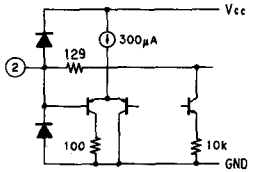
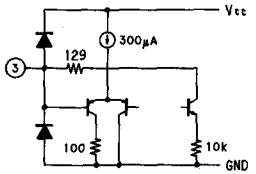
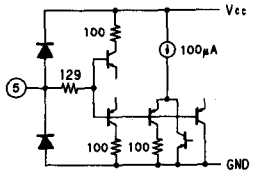
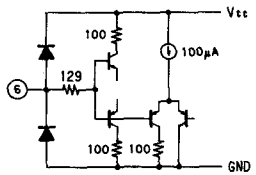
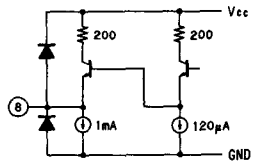
Operating Condition

Supply voltage	4.6 to 5.2	V

Block Diagram and Pin Configuration



Pin Description

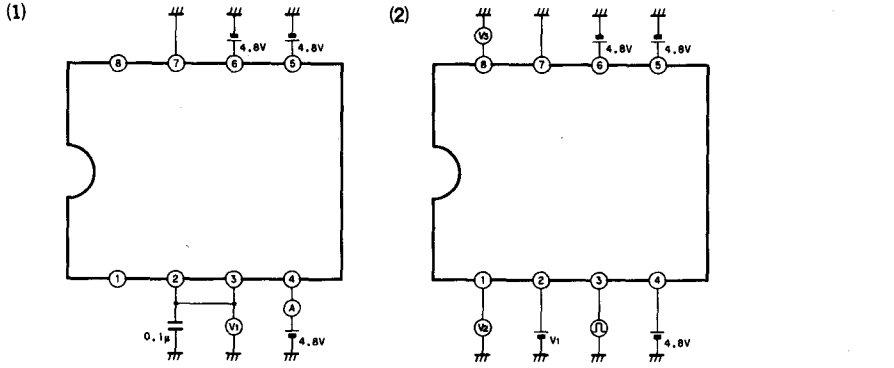
Pin No.	Symbol	Pin Voltage	Equivalent Circuit	Description
1	OUT2	Black level 1.6V		CDS signal output pin. 9.5dB amplifier output.
2	IN P	Black level 2.6V		Output signal from CCD to be input. To be input by capacitance coupling. Input at low impedance.
3	IN D	Black level 2.6V		Output signal from CCD to be input. Normally, coupled with Pin 2 when used. Input at low impedance.
4	V_{CC}	4.8V		V_{CC}
5	SHD	 H···2V or more L···1V or less		Sample and hold high speed pulse to be input. (Active: Hi) V_{TH}=1.5V
6	SHP	 H···2V or more L···1V or more		Sample and hold high speed pulse to be input. (Active: Hi) V_{TH}=1.5V
7	GND			GND
8	OUT1	Black level 1.6V		CDS signal output pin 6dB amplifier output.

Electrical Characteristics (V_{CC}=4.8V, Ta=25°C)

No.	Item	Symbol	Test Circuit	Condition	Min.	Typ.	Max.	Unit
1	Power consumption	P	(1)	V_{CC} value × V_{CC} current value	40	57	80	mW
2	Gain (6dB)	G1	(2)	Input - OUT1 gain IN D input level=300mV	5	6	7	dB
3	Gain (9.5dB)	G2	(2)	Input - OUT2 gain IN D input level=300mV	8.5	9.5	10.5	dB
4	Output D range (6dB)	O DR1	(2)	OUT1 dynamic range IN D input level=1.5V	1.4	1.7		V
5	Output D range (9.5dB)	O DR2	(2)	OUT2 dynamic range IN D input level=1.5V	1.4	1.7		V
6	Amplifier CMRR (6dB)	CMRR1	—	6dB amplifier CMRR 10MHz		−40*1		dB
7	Amplifier CMRR (9.5dB)	CMRR2	—	9.5dB amplifier CMRR 10MHz		−40*1		dB
8	Amplifier frequency response	Fcut	—	3dB down point		100*1		MHz
9	Sample and hold pulse width	Tw	—	Threshold level (1.5V)		17.5*2		nS

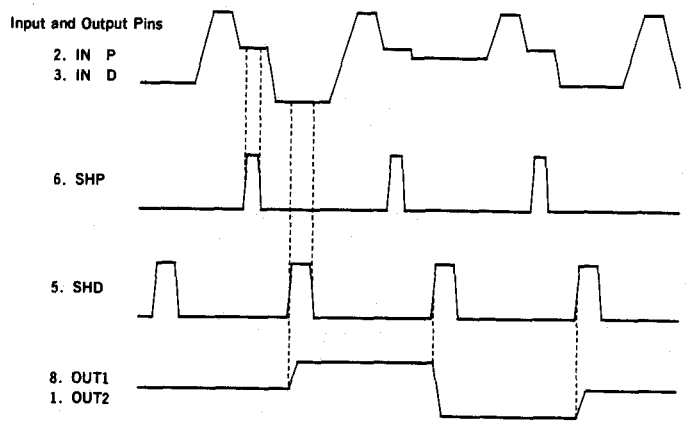
Note) Both * 1 and * 2 are design reference values.
* 1 : Stand-alone characteristics of amplifier
* 2 : Sampling pulse width which enable the level to change over 800mV at 6dB amplifier output.

Electrical Characteristics Test Circuit

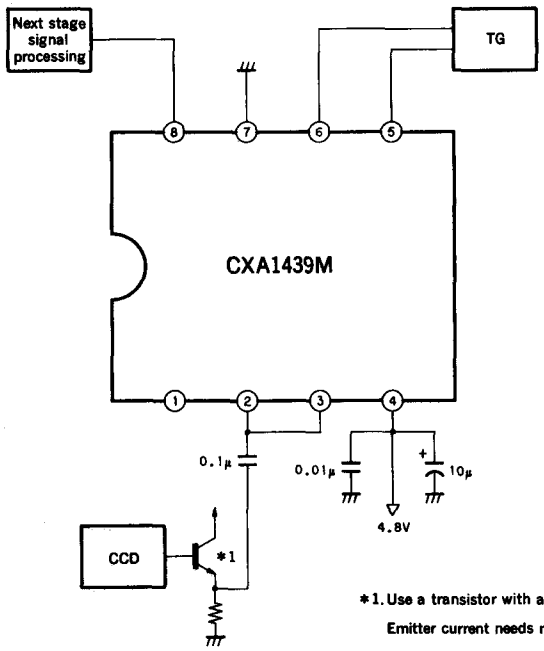


Note 1) The DC value of V1 is the measured value (V1) in (1).
Note 2) The input signal to IN D is input level V1.

Input and Output Waveform Diagram



Application Circuit (6dB amplifier only to be used)



*1. Use a transistor with a high f_T (2SC3355 for example).
Emitter current needs more than 1mA.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

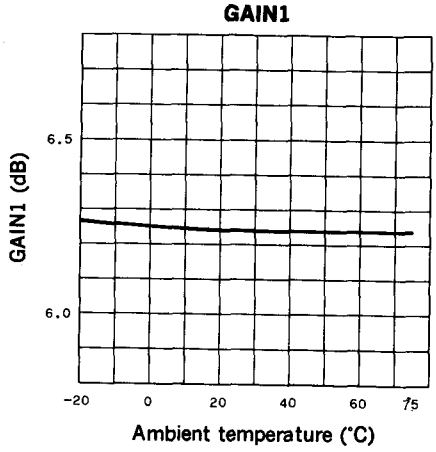
(1) Make short the distance between CXA1439M and a timing IC (TG) in order to reduce the impedance of Vcc and GND.

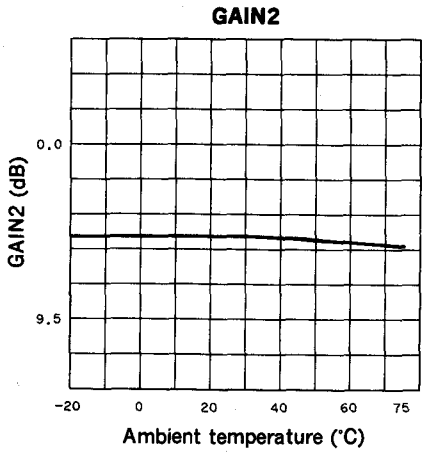
(2) Make impedance of input signal line (output signal from CCD) low and the length of that minimum.

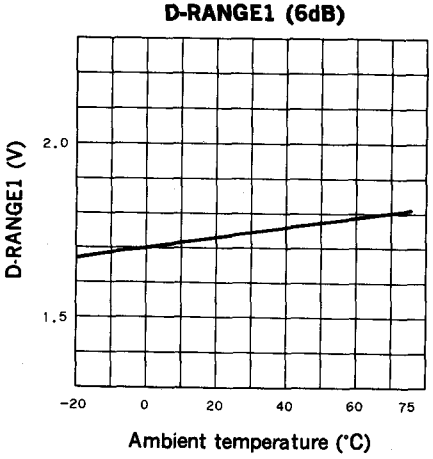
(3) Make short the sample and hold pulse line, not to have coupling between other elements.

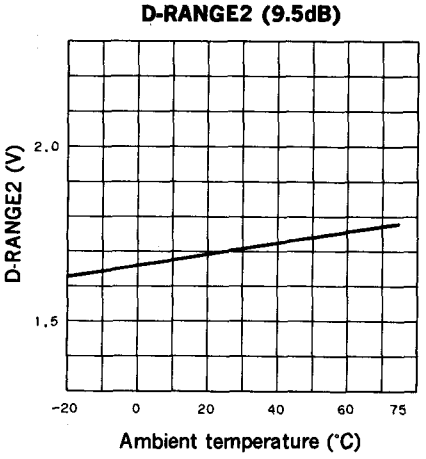
Examples of Typical Characteristics

I. Temperature Characteristics (V_{CC}=4.8V)



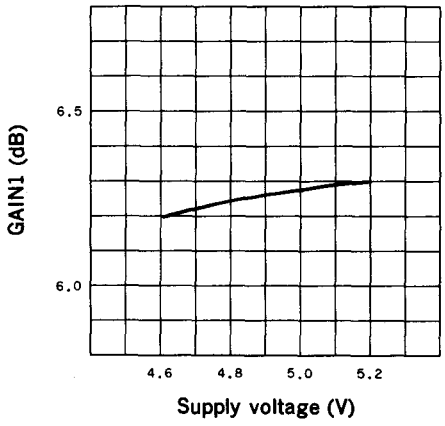




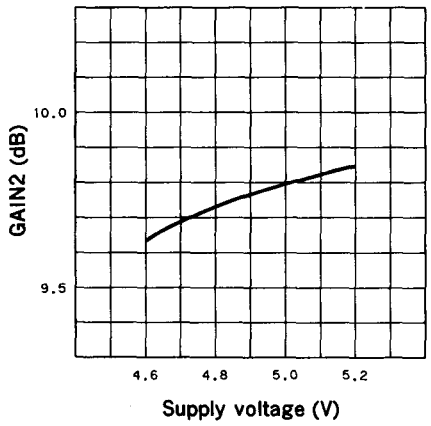


II. Supply Voltage Characteristics (Ta=25°C)

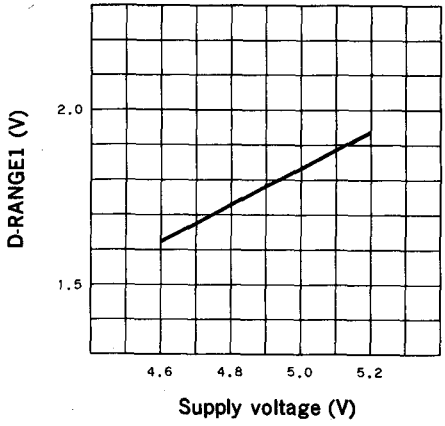
GAIN1



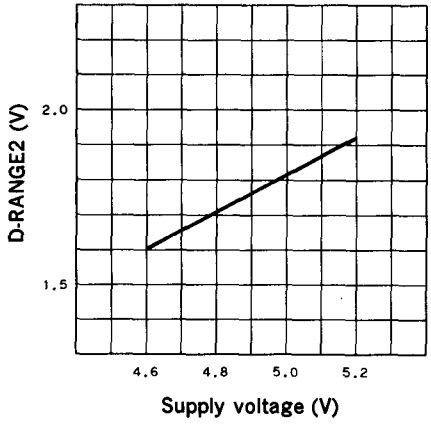
GAIN2



D-RANGE1 (6dB)

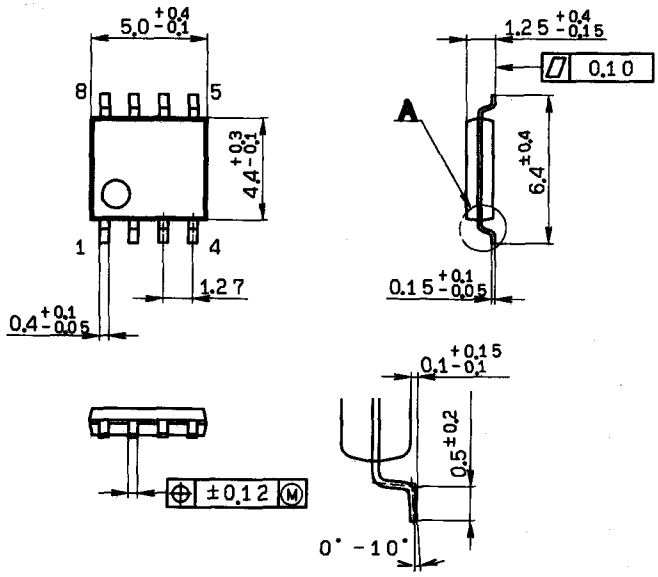


D-RANGE2 (9.5dB)



Package Outline Unit: mm

8pin SOP (Plastic) 225mil



Detailed diagram of A

SONY NAME	SOP-8P-L03
EIAJ NAME	*SOP008-P-0225-A
JEDEC CODE	———

SONY CXL1503M/1505M

CMOS-CCD Signal Processor

Description

CXL1503M and CXL1505M are CMOS-CCD signal processors developed for CCD camera complementary color filter array processing system.

CXL1503M 1H×4 301.5 bit CCD delay line
CXL1505M 1H×4 453.5 bit CCD delay line

Features

- Single power supply 5V
- Low power consumption
  CXL1503M 100mW (Typ.)
  CXL1505M 150mW (Typ.)
- Built-in peripheral circuits
- Built-in CDS(Correlated Double Sampling) circuit

Function

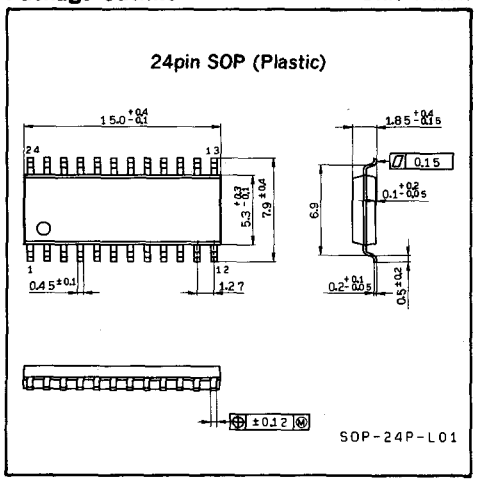
- Clock driver
- Autobias circuit (center and black)
- Pedestal clamp circuit
- CDS circuit

Structure

CMOS-CCD

Package Outline

Unit : mm



Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	6	V
• Operating temperature	T_{opr}	−10 to +60	°C
• Storage temperature	T_{stg}	−55 to +150	°C
• Allowable power dissipation	P_D	500	mW

Recommended Operating Conditions (Ta=25°C)

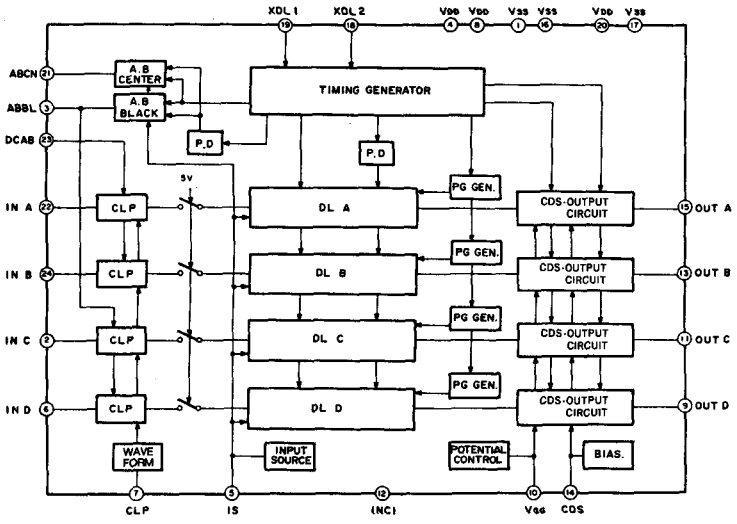
• Supply voltage	V_{DD}	5 ±5%	V

Recommended Clock Conditions (Ta=25°C)

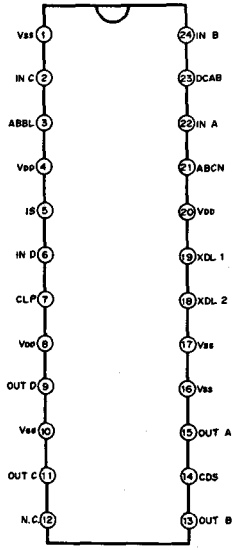
Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Clock voltage Low		V_L	0		1.0	V	
Clock voltage High		V_H	V_{DD}−1.0		V_{DD}	V	
Clock frequency	CXL1503M	f_{CL}		4.77		MHz	NTSC: 910f_H/3 CCIR: 908f_H/3
	CXL1505M	f_{CL}		7.16		MHz	NTSC: 455f_H CCIR: 454f_H

E89174A03-HP

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description	Impedance(Ω)
1, 16, 17	V_{SS}	—	GND	
2	IN C	I	Signal input C channel	>100k (at no clamp)
3	ABBL	O	Autobias DC output for Y signal	2k to 20k
4, 8, 20	V_{DD}	—	5V power supply	
5	IS	O	Input source DC output	5k
6	IN D	I	Signal input D channel	>100k (at no clamp)
7	CLP	I	Clamp pulse input	>100k
9	OUT D	O	Signal output D channel	50 to 500
10	V_{GG}	O	Gate bias DC output	2k to 10k
11	OUT C	O	Signal output C channel	50 to 500
12	N.C.	—	—	
13	OUT B	O	Signal output B channel	50 to 500
14	CDS	O	DC output for CDS	500 to 5k
15	OUT A	O	Signal output A channel	50 to 500
18	XDL2	I	Clock pulse input 2	>100k
19	XDL1	I	Clock pulse input 1	>100k
21	ABCN	O	Autobias DC output for C signal	2k to 20k
22	IN A	I	Signal input A channel	>100k (at no clamp)
23	DCAB	I	DC bias input for A and B channel	>100k
24	IN B	I	Signal input B channel	>100k (at no clamp)

Electrical Characteristics (Ta = 25°C, V_{DD}=5.0V, V_{SS}=0V) f_{CL}=4.77MHz (CXL1503M) f_{CL}=7.16MHz (CXL1505M)

Item		Symbol	Test point	SW position SW1	SW2	SW3	SW4 to 7	Bias condition E1	Conditions	Min.	Typ.	Max.	Unit
Autobias Center level		ABCN	V_1	a	b	a	a			1.0	2.0	4.0	V
Autobias Black level		ABBL	V_2	a	b	a	a			1.2	2.2	4.2	V
Input source level		IS	V_3	a	a	a	a			0.3	0.6	3.0	V
CDS source level		CDS	V_4	a	a	a	a			1.2	2.3	3.5	V
Output circuit bias level		V_{GG}	V_5	a	a	a	a			0.3	0.8	3.0	V
*Supply current	CXL1503M	I_{DD}	A_1	b	a	a	a	V_1		—	20	35	mA
	CXL1505M									—	30	40	
Insertion gain		IG	V_6	b	b	a to d	a	A, Bch → V_1 C, Dch → V_2 −0.2V	$20\log\frac{\text{Output amplitude (mVp-p)}}{\text{Input amplitude (SIN100kHz, 100mVp-p)}}$	−4.5	−3.5	−0.5	dB
*Frequency response	CXL1503M	f_G	V_6	c	b	a to d	a	↓	$20\log\frac{\text{Output amplitude (SIN1MHz, 100mVp-p)}}{\text{Output amplitude (SIN100kHz, 100mVp-p)}}$	−1.8	−0.8	—	dB
	CXL1505M									−1.5	−0.4	—	
Linearity		Lin.	V_6	b	b	a to d	a	↓	(Note 1)	0	5	12	%
Insertion gain difference between channels		ΔG							(Note 2)	0	5	15	%
Linearity difference between channels	Ach ↔ Bch	ΔL_{AB}							(Note 3)	0	1	5	%
	Cch ↔ Dch	ΔL_{CD}							(Note 3)	0	1	5	%
Cross talk between channels		CRT	V_6	a	b	a to d	a ↔ b	A, Bch → V_1 C, Dch → V_2−0.2V	(Note 4)	0	1	3	%

* **Note)** Standard values are different between CXL1503M and CXL1505M.

Note

1. Linearity testing

For A channel and B channel, set input bias E_1 to ABCN +0.2(V) first, and then set it to ABCN(V) and ABCN −0.2(V). Then input a sine wave of 100kHz and 100mVp-p, and compare the three output amplitudes.

For C channel and D channel, set input bias E_1 to ABBL −0.4(V) first, and then set it to ABBL −0.2(V) and ABBL(V). Then input a sine wave of 100kHz and 100mVp-p, and compare the three output amplitudes.

The maximum output amplitude for the respective A, B, C and D channels is taken as Sout max. and the minimum output amplitude as Sout min. The linearity of the respective channels is defined as

$$\text{Lin.} = \frac{\text{Sout max} - \text{Sout min}}{\text{Sout max} + \text{Sout min}} \times 200\ (\%)$$

2. Calculation of insertion gain difference

As the max. insertion gain among A, B, C and D channels' is taken as Gmax and the min. as Gmin., the insertion gain difference between channels becomes:

$$\Delta G = \text{ABS}\left(1 - 10^{\left(\frac{Gmax - Gmin}{20}\right)}\right) \times 100\ (\%)$$

3. Calculation of linearity difference

Define Ach linearity as L_A, and Bch linearity as L_B we obtain the difference ΔL_{AB} as

$$\Delta L_{AB} = |\, L_A - L_B \,|\ (\%)$$

Similarly we obtain the linearity difference ΔL_{CD} of Cch and Dch as

$$\Delta L_{CD} = |\, L_C - L_D \,|\ (\%)$$

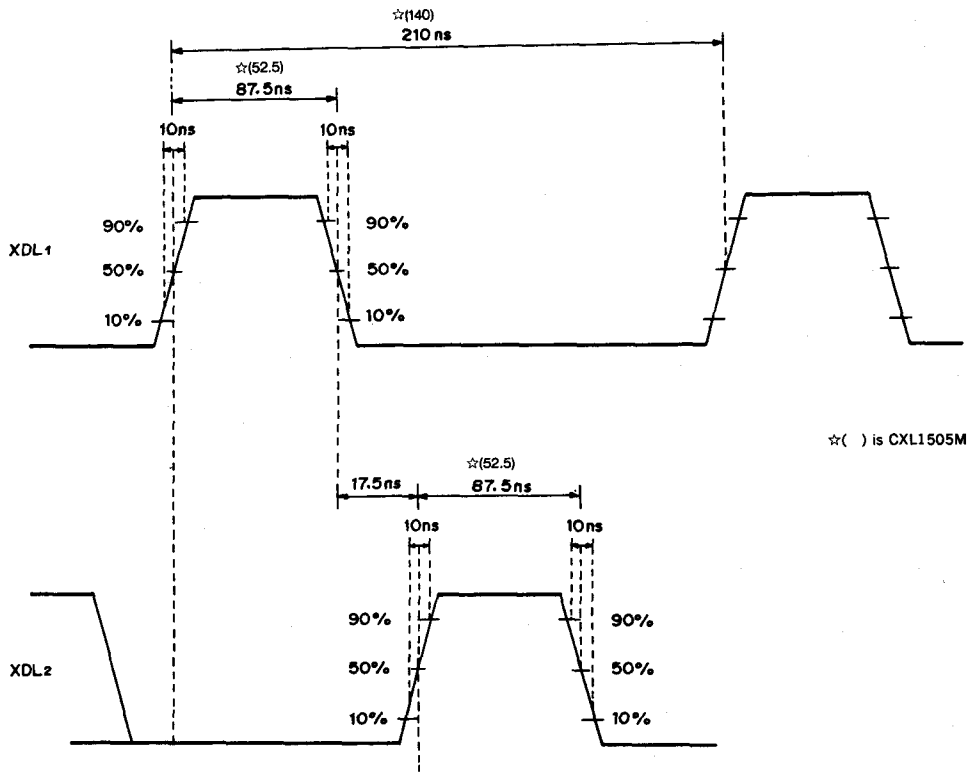
4. Crosstalk calculation

We take CRT_a as: Ach crosstalk value only during Bch input
CRT_b as: Bch crosstalk value only during Ach input
CRT_c as: Cch crosstalk value only during Dch input
CRT_d as: Dch crosstalk value only during Cch input

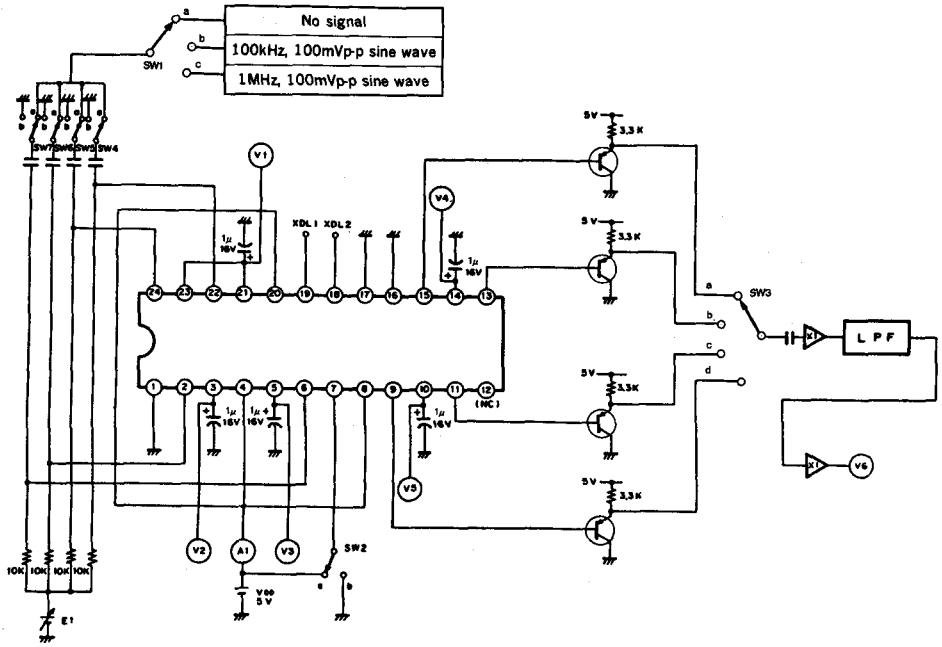
The crosstalk value of respective channels becomes:

$$CRT_{a\ \text{to}\ d} = \frac{\text{Crosstalk component}}{\text{Each channel output value}} \times 100\ (\%)$$

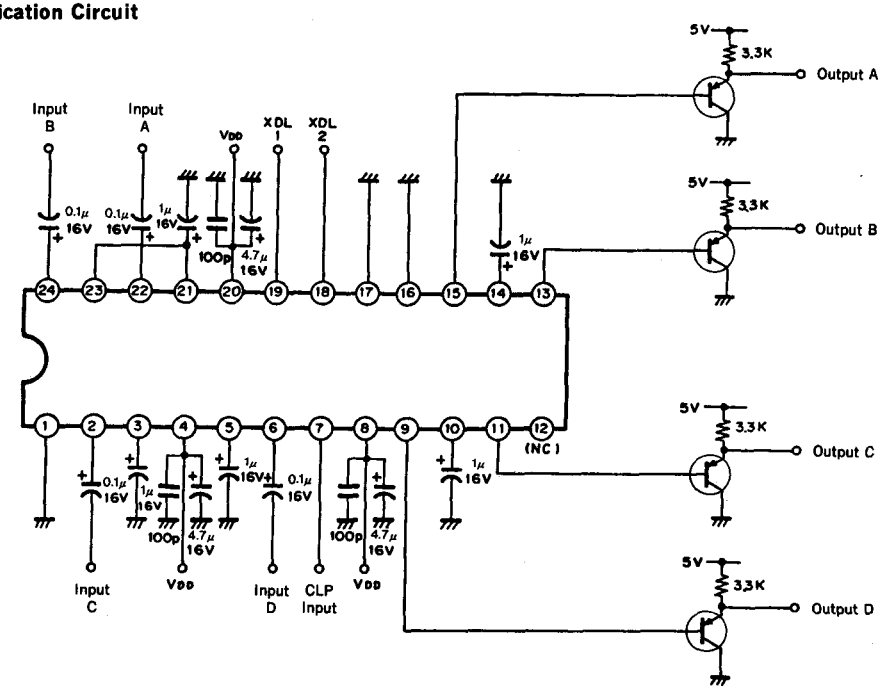
Clock Waveform Timing



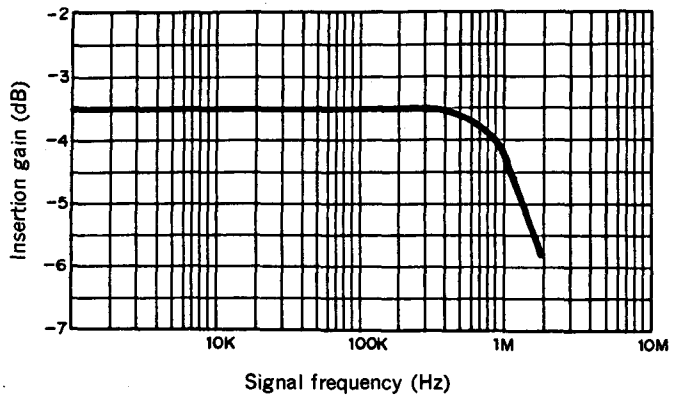
Electrical Characteristics Test Circuit



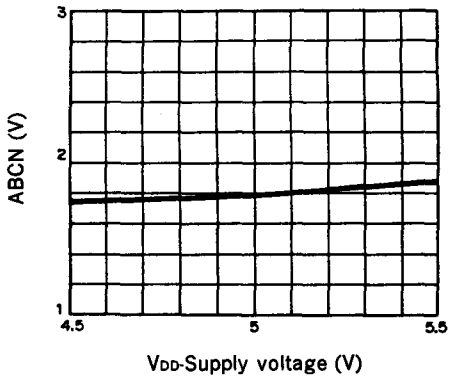
Application Circuit



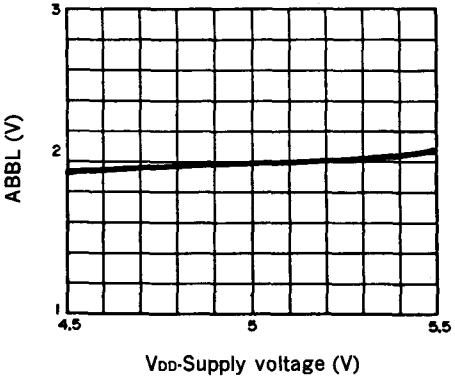
Frequency response



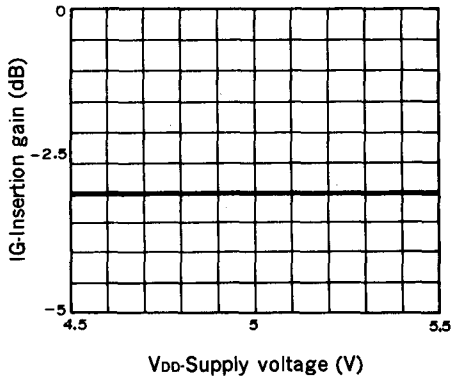
ABCN vs. Supply voltage



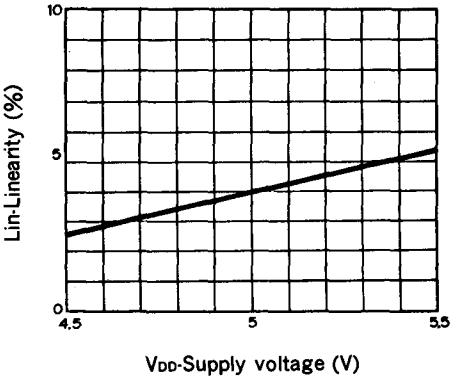
ABBL vs. Supply voltage



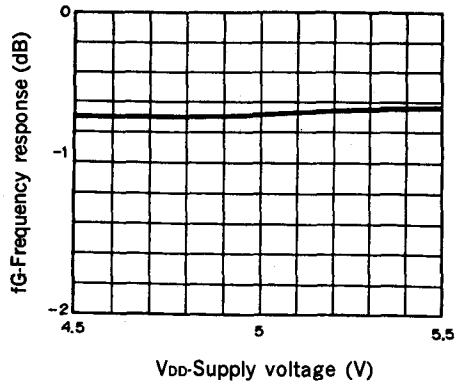
Insertion gain vs. Supply voltage



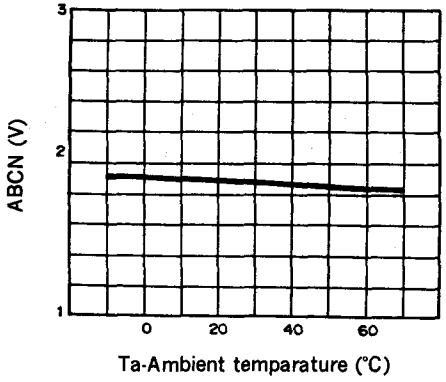
Linearity vs. Supply voltage



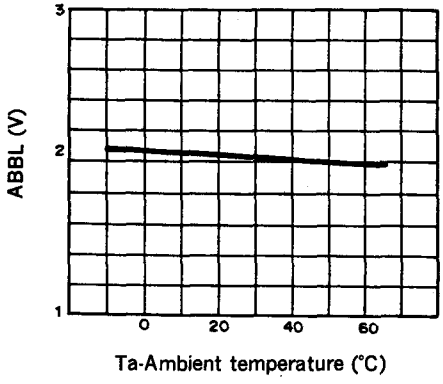
Frequency response vs. Supply voltage



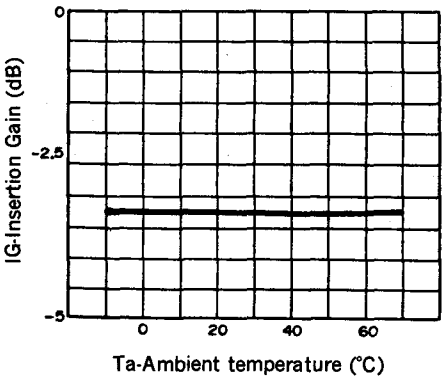
ABCN vs. Ambient temperature



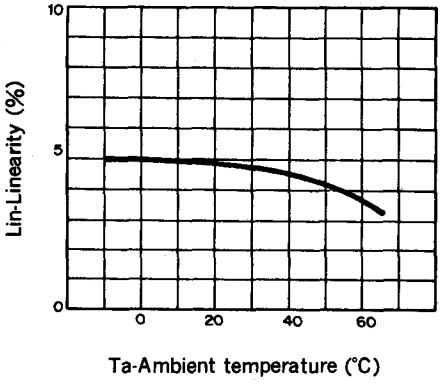
ABBL vs. Ambient temperature



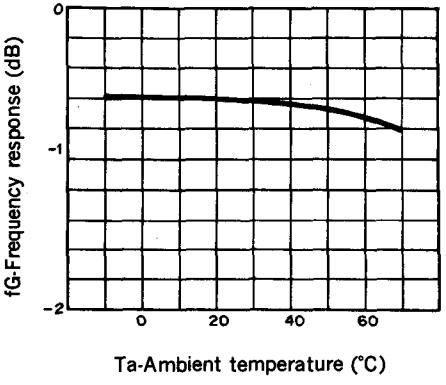
Insertion gain vs. Ambient temperature



Linearity vs. Ambient temperature



Frequency response vs. Ambient temperature



SONY

CXL1517M/1518M

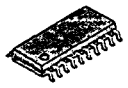
CMOS-CCD Signal Processor

Description

CXL1517M and CXL1518M are CMOS-CCD signal processors developed for CCD camera complementary color filter array processing system.

CXL1517M
452.5-bit × 2, 453.5-bit 1H CCD delay line
CXL1518M
300.5-bit × 2, 301.5-bit 1H CCD delay line

20 pin SOP (Plastic)



Features

- Single power supply 5V
- Low power consumption (Typ.)
  CXL1517M 120mW
  CXL1518M 75mW
- Built-in peripheral circuits
- Built-in CDS (Correlated Double Sampling) circuit

Functions

- Clock driver
- Autobias circuit (Center and black)
- Pedestal clamp circuit
- CDS circuit
- Overflow prevention circuit

Structure

CMOS-CCD

Absolute Maximum Ratings (Ta=25℃)

• Supply voltage	V_{DD}	6	V
• Operating temperature	Topr	−10 to +65	℃
• Storage temperature	Tstg	−55 to +150	℃
• Allowable power dissipation	P_D	500	mW (SOP package)

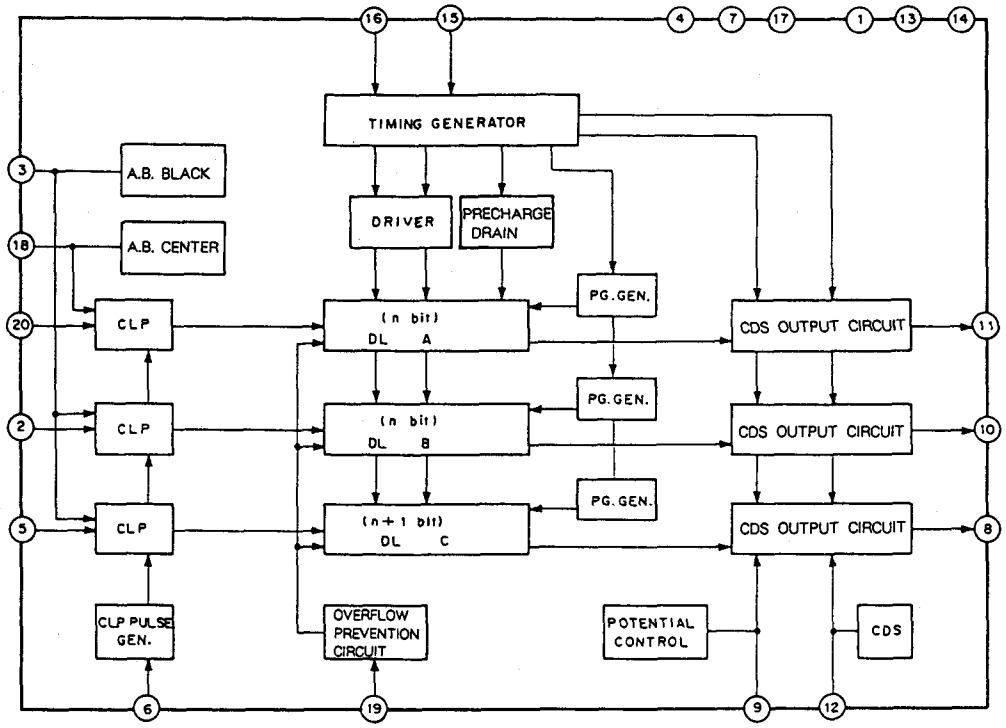
Recommended Operating Supply Voltage (Ta=25℃)

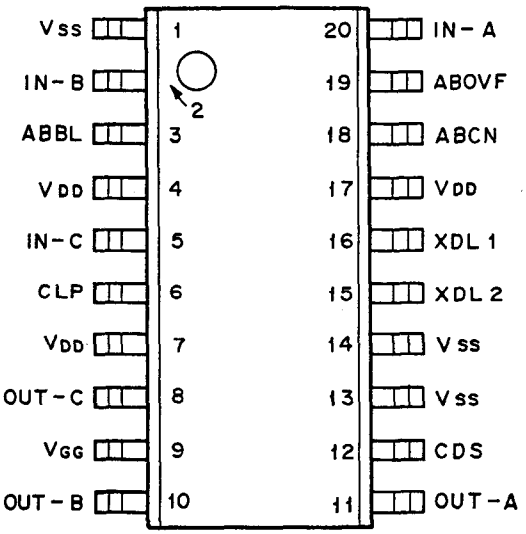
Supply voltage	V_{DD}	5V	+0.25V −0.40V

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Clock voltage Low		V_L	Vss		0.3 × V_{DD}	V	
Clock voltage High		V_H	0.7 × V_{DD}		V_{DD}	V	
Clock frequency	CXL1517M	f_{CL}		7.16		MHz	NTSC: 455f_H CCIR: 454f_H
	CXL1518M	f_{CL}		4.77		MHz	NTSC: 910f_H/3 CCIR: 908f_H/3

E91777 – ST

Block Diagram and Pin Configuration (Top View)





Pin Description

Pin No.	Symbol	I/O	Description	Comment
1	Vss	—	GND	Analog
2	IN-B	I	Signal input B channel (Y)	
3	ABBL	O	Autobias DC output for Y signal	Black level bias
4	V_{DD}	—	Power supply	Analog
5	IN-C	I	Signal input C channel (Y)	Black level bias at no clamp>100K
6	CLP	I	Clamp pulse input	>100K
7	V_{DD}	—	Power supply	Output circuit
8	OUT-C	O	Signal output C channel	
9	V_{GG}	O	Output circuit bias DC output	
10	OUT-B	O	Signal output B channel	
11	OUT-A	O	Signal output A channel	
12	CDS	O	DC output for CDS	
13	Vss	—	GND	Output circuit
14	Vss	—	GND	timing
15	XDL2	I	Clock pulse input 2	>100K
16	XDL1	I	Clock pulse input 1	>100K
17	V_{DD}	—	Power supply	timing
18	ABCN	O	Autobias DC output for C signal	Center level bias
19	ABOVF	O	Autobias DC output for overflow prevention circuit	
20	IN-A	I	Signal input A channel (C)	Center level bias at no clamp>100K

Electrical Characteristics

Ta=25℃, V_{DD}=5.0V, V_{SS}=0V f_{CL}=4.77MHz (CXL1518M)
f_{CL}=7.16MHz (CXL1517M)

Item		Symbol	Test point	SW conditions SW1	SW2	SW3	SW4 to 6	Bias conditions E1	Conditions	Standard values Min.	Typ.	Max.	Unit
Autobias center level		ABCN	V_1	a	b	a	a			4.2	4.6	4.8	V
Autobias black level		ABBL	V_2	a	b	a	a			3.9	4.3	4.5	V
Overflow prevention circuit Auto bias level		ABOVF	V_3	a	b	a	a			2.6	3.0	3.3	V
CDS source level		CDS	V_4	a	a	a	a			1.2	2.3	3.5	V
Output circuit bias level		V_{GG}	V_5	a	a	a	a			0.3	0.8	3.0	V
☆ Current supply	CXL1517M	I_{DD}	A_1	b	a	a	a	V_1		—	24	35	mA
	CXL1518M									—	15	25	
Insertion gain		IG	V_6	b	b	a to c	a	A→V_1 B, C→ V_2+0.25V	$20\log \frac{\text{Output amplitude (mVp-p)}}{\text{Input amplitude (SIN100kHz, 100mVp-p)}}$	−4.5	−3.5	—	dB
☆ Frequency response	CXL1517M	f_G	V_6	b ↕ c	b	a to c	a	↓	$20\log \frac{\text{Output amplitude (SIN1MHz, 100mVp-p)}}{\text{Output amplitude (SIN100kHz, 100mVp-p)}}$	−1.5	−0.4	—	dB
	CXL1518M									−1.8	−0.8	—	
Linearity		Lin.	V_6	b	b	a to c	a		Note 1)	0	5	12	%
The insertion gain difference between channels		ΔG							Note 2)	0	5	12	%
Linearity difference between channels	Bch→Cch	ΔL_{BC}							Note 3)	0	1	5	%
Cross-talk between channels		CRT	V_6	b	b	a to c	a ↕ b	A→V_1 B, C→ V_2+0.25V	Note 4)	0	1	3	%

☆ Standard values are different between CXL1517M and CXL1518M.

Note 1) Linearity testing

For A channel, set input bias to ABCN–0.2 (V) first, and then set it to ABCN and ABCN+0.2 (V). Then input a sine wave of 100kHz and 100mVp-p, and compare the three output amplitudes. For B channel and C channel, set input bias to ABBL+0.45 (V) first, and then set it to ABBL+0.25 (V) and ABBL+0.05 (V). Then input a sine wave of 100kHz and 100mVp-p, and compare the three output amplitudes. The maximum output amplitude for the respective A, B and C channels is taken as Sout max and the minimum output amplitude as Sout min. The linearity of the respective channels is defined as

$$\text{Lin.} = \frac{\text{Sout max} - \text{Sout min}}{\text{Sout max} + \text{Sout min}} \times 200\ (\%)$$

Note 2) Calculation of insertion gain difference

As the maximum insertion gain among A, B and C channels is taken as Gmax and the minimum as Gmin, the insertion gain difference between channels Δ G as:

$$\Delta G = \left|1 - 10^{\left(\frac{Gmax - Gmin}{20}\right)}\right| \times 100\ (\%)$$

Note 3) Calculation of linearity difference

Define B channel linearity as L_B and C channel linearity as Lc we obtain the difference ΔL_{BC} as

$\Delta L_{BC} = |L_B - Lc|$ (%)

Note 4) Cross-talk calculation

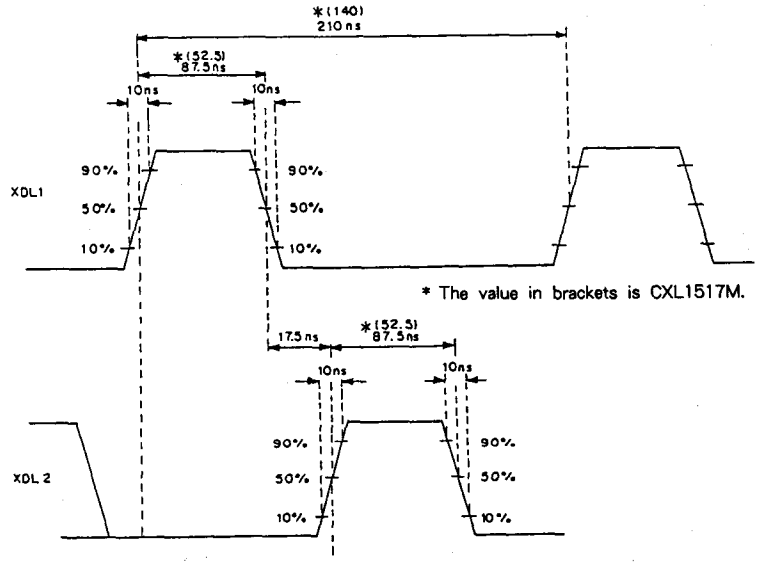
CRTa : The cross-talk value of A channel when B and C channels are input

OUT_{A-a} : The output value of A channel when A channel is input
SW3-a, SW4-a, SW5, 6-b

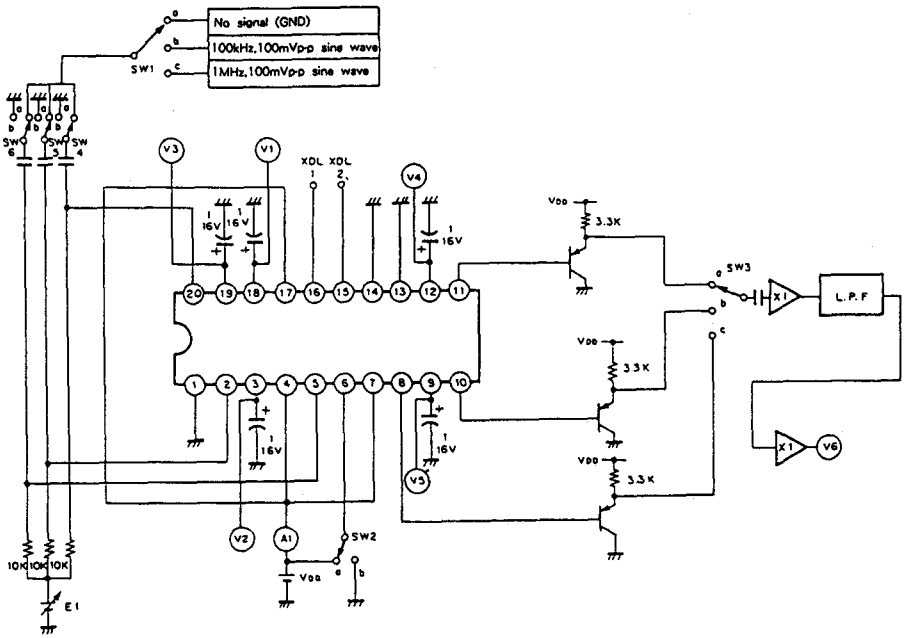
OUT_{A-bc} : The output value of A channel when B and C channels are input
(Cross-talk component)
SW3-a, SW4-b, SW5, 6-a

$$CRTa = \frac{OUT_{A-bc}}{OUT_{A-a}} \times 100\ (\%)$$

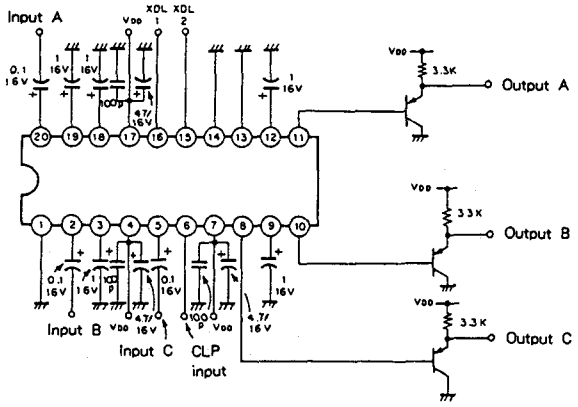
Clock Waveform Timing



Electrical Characteristics Test Circuit



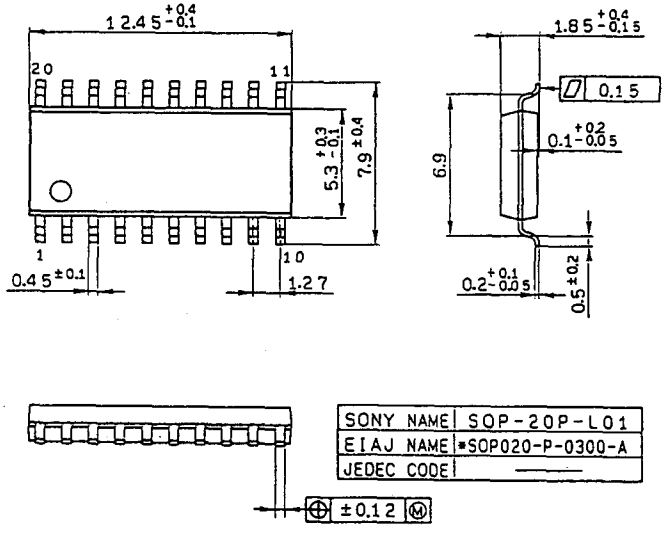
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline

Unit : mm



SONY NAME	SOP-20P-L01
EIAJ NAME	*SOP020-P-0300-A
JEDEC CODE	———

SONY

CXL1517N/1518N

CMOS-CCD Signal Processor

Description

CXL1517N and CXL1518N are CMOS-CCD signal processors developed for CCD camera complementary color filter array processing system.

CXL1517N
452.5-bit × 2, 453.5-bit 1H CCD delay line
CXL1518N
300.5-bit × 2, 301.5-bit 1H CCD delay line

24 pin VSOP (Plastic)

Features

- Single power supply 5V
- Low power consumption (Typ.)
  CXL1517N 120mW
  CXL1518N 75mW
- Built-in peripheral circuits
- Built-in CDS (Correlated Double Sampling) circuit

Functions

- Clock driver
- Autobias circuit (Center and black)
- Pedestal clamp circuit
- CDS circuit
- Overflow prevention circuit

Structure

CMOS-CCD

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	6	V
• Operating temperature	Topr	−10 to +65	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	350	mW (VSOP package)

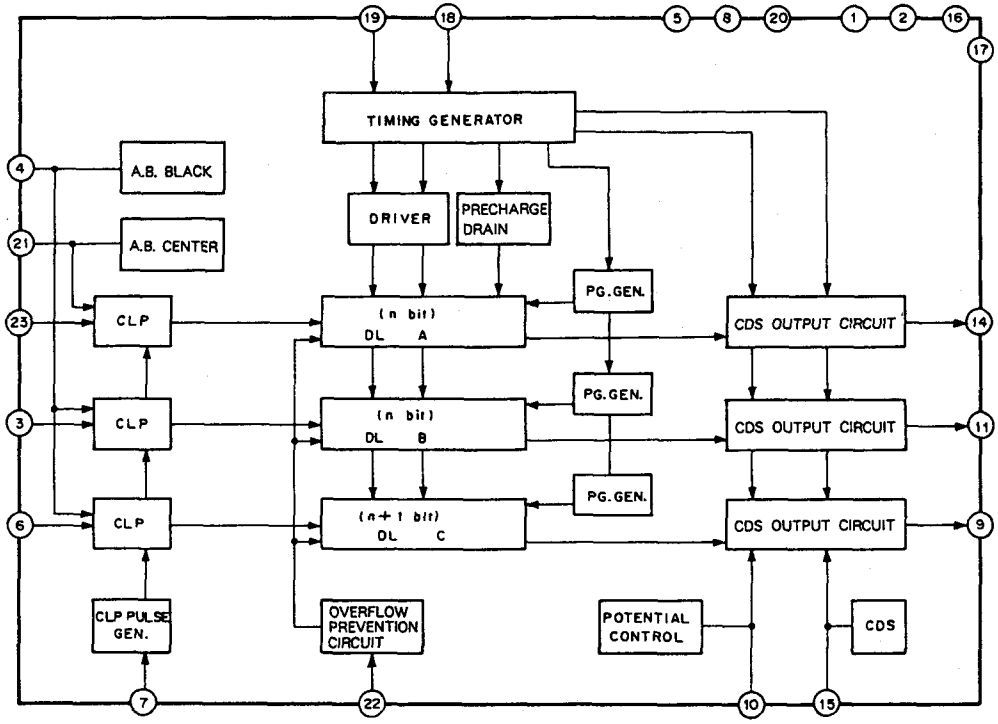
Recommended Operating Supply Voltage (Ta=25°C)

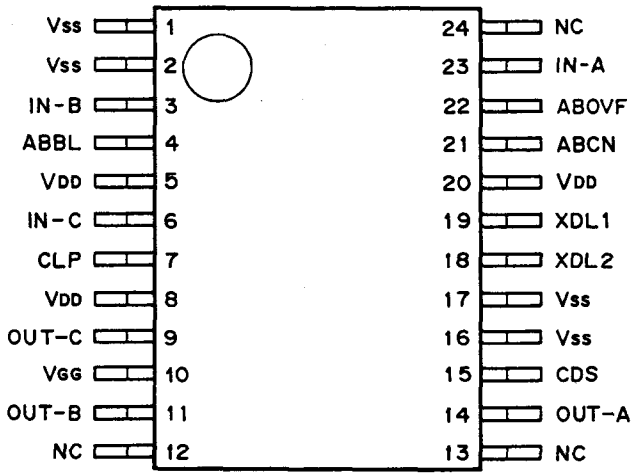
Supply voltage V_{DD} 5V +0.25V −0.40V

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Clock voltage Low		V_L	Vss		0.3 × V_{DD}	V	
Clock voltage High		V_H	0.7 × V_{DD}		V_{DD}	V	
Clock frequency	CXL1517N	f_{CL}		7.16		MHz	NTSC: 455f_H CCIR: 454f_H
	CXL1518N	f_{CL}		4.77		MHz	NTSC: 910f_H/3 CCIR: 908f_H/3

E91778 – ST

Block Diagram and Pin Configuration (Top View)





Pin Description

Pin No.	Symbol	I/O	Description	Comment
1	Vss	—	GND	
2	Vss	—	GND	Analog
3	IN-B	I	Signal input B channel (Y)	
4	ABBL	O	Autobias DC output for Y signal	Black level bias
5	V_{DD}	—	Power supply	Analog
6	IN-C	I	Signal input C channel (Y)	Black level bias at no clamp>100K
7	CLP	I	Clamp pulse input	>100K
8	V_{DD}	—	Power supply	Output circuit
9	OUT-C	O	Signal output C channel	
10	V_{GG}	O	Output circuit bias DC output	
11	OUT-B	O	Signal output B channel	
12	NC	—	—	
13	NC	—	—	
14	OUT-A	O	Signal output A channel	
15	CDS	O	DC output for CDS	
16	Vss	—	GND	Output circuit
17	Vss	—	GND	timing
18	XDL2	I	Clock pulse input 2	>100K
19	XDL1	I	Clock pulse input 1	>100K
20	V_{DD}	—	Power supply	timing
21	ABCN	O	Autobias DC output for C signal	
22	ABOVF	O	Autobias DC output for overflow prevention circuit	
23	IN-A	I	Signal input A channel (C)	Center level bias at no clamp>100K
24	NC	—	—	

Electrical Characteristics

Ta=25℃, V_{DD}=5.0V, V_{SS}=0V f_{CL}=4.77MHz (CXL1518N)
f_{CL}=7.16MHz (CXL1517N)

Item		Symbol	Test point	SW conditions SW1	SW2	SW3	SW4 to 6	Bias conditions E1	Conditions	Standard values Min.	Typ.	Max.	Unit
Autobias center level		ABCN	V_1	a	b	a	a			4.2	4.6	4.8	V
Autobias black level		ABBL	V_2	a	b	a	a			3.9	4.3	4.5	V
Overflow prevention circuit Auto bias level		ABOVF	V_3	a	b	a	a			2.6	3.0	3.3	V
CDS source level		CDS	V_4	a	a	a	a			1.2	2.3	3.5	V
Output circuit bias level		V_{GG}	V_5	a	a	a	a			0.3	0.8	3.0	V
☆ Current supply	CXL1517N	I_{DD}	A_1	b	a	a	a	V_1		—	24	35	mA
	CXL1518N									—	15	25	
Insertion gain		IG	V_6	b	b	a to c	a	A→V_1 B, C→ V_2+0.25V	$20\log \frac{\text{Output amplitude (mVp-p)}}{\text{Input amplitude (SIN100kHz, 100mVp-p)}}$	−4.5	−3.5	—	dB
☆ Frequency response	CXL1517N	f_G	V_6	b ↕ c	b	a to c	a	↓	$20\log \frac{\text{Output amplitude (SIN1MHz, 100mVp-p)}}{\text{Output amplitude (SIN100kHz, 100mVp-p)}}$	−1.5	−0.4	—	dB
	CXL1518N									−1.8	−0.8	—	
Linearity		Lin.	V_6	b	b	a to c	a		Note 1)	0	5	12	%
The insertion gain difference between channels		ΔG							Note 2)	0	5	12	%
Linearity difference between channels	Bch→Cch	ΔL_{BC}							Note 3)	0	1	5	%
Cross-talk between channels		CRT	V_6	b	b	a to c	a ↕ b	A→V_1 B, C→ V_2+0.25V	Note 4)	0	1	3	%

☆ Standard values are different between CXL1517N and CXL1518N.

Note 1) Linearity testing

For A channel, set input bias to ABCN–0.2 (V) first, and then set it to ABCN and ABCN+0.2 (V). Then input a sine wave of 100kHz and 100mVp-p, and compare the three output amplitudes. For B channel and C channel, set input bias to ABBL+0.45 (V) first, and then set it to ABBL+0.25 (V) and ABBL+0.05 (V). Then input a sine wave of 100kHz and 100mVp-p, and compare the three output amplitudes. The maximum output amplitude for the respective A, B and C channels is taken as Sout max and the minimum output amplitude as Sout min. The linearity of the respective channels is defined as

$$\text{Lin.} = \frac{\text{Sout max} - \text{Sout min}}{\text{Sout max} + \text{Sout min}} \times 200\ (\%)$$

Note 2) Calculation of insertion gain difference

As the maximum insertion gain among A, B and C channels is taken as Gmax and the minimum as Gmin, the insertion gain difference between channels Δ G as:

$$\Delta G = \left|1 - 10^{\left(\frac{Gmax - Gmin}{20}\right)}\right| \times 100\ (\%)$$

Note 3) Calculation of linearity difference

Define B channel linearity as L_B and C channel linearity as Lc we obtain the difference Δ L_{BC} as

$\Delta L_{BC} = |L_B - Lc|$ (%)

Note 4) Cross-talk calculation

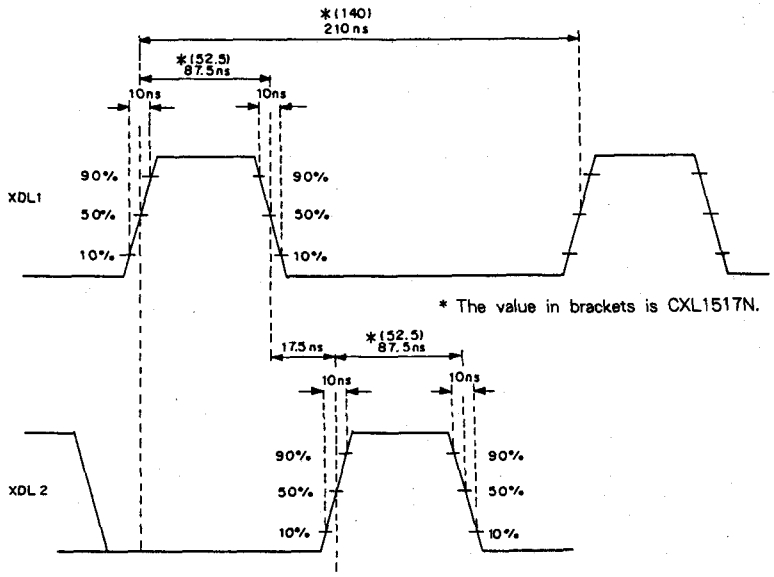
CRTa : The cross-talk value of A channel when B and C channels are input

OUT_{A-a} : The output value of A channel when A channel is input
SW3-a, SW4-a, SW5, 6-b

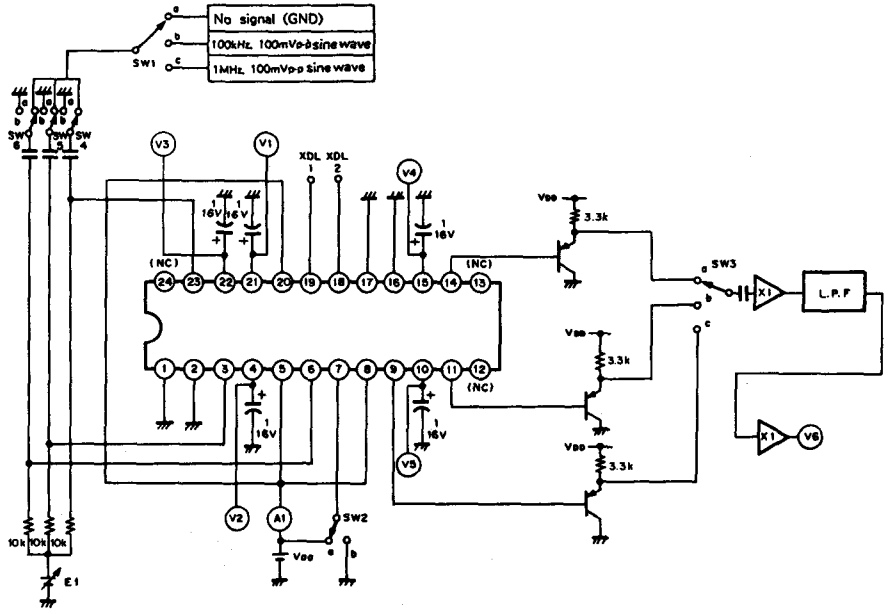
OUT_{A-bc} : The output value of A channel when B and C channels are input
(Cross-talk component)
SW3-a, SW4-b, SW5, 6-a

$$CRTa = \frac{OUT_{A-bc}}{OUT_{A-a}} \times 100\ (\%)$$

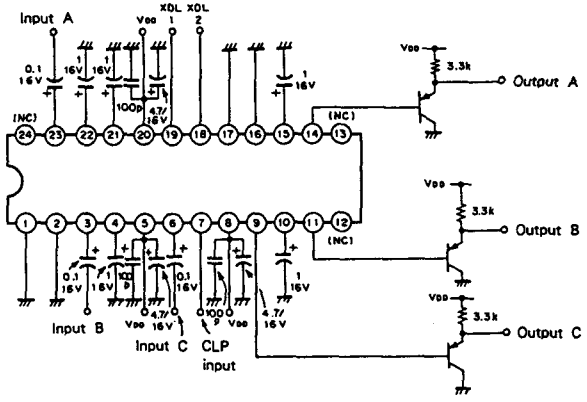
Clock Waveform Timing



Electrical Characteristics Test Circuit



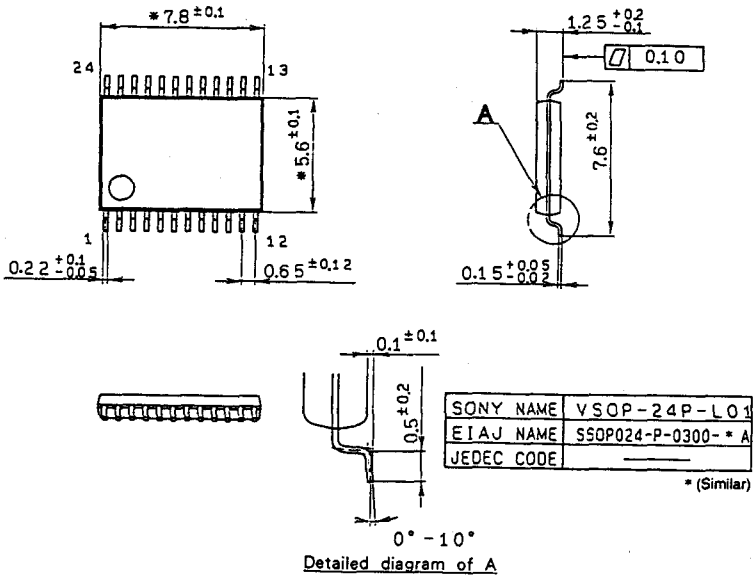
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit : mm

24pin VSOP (Plastic) 275mil



SONY NAME	VSOP-24P-L01
EIAJ NAME	SSOP024-P-0300-*A
JEDEC CODE	———

* (Similar)

Detailed diagram of A

Note) Dimensions marked with * does not include resin residue.

SONY CXL1504M

CMOS-CCD 1H Delay line for NTSC

Description

CXL1504M is a delay line used in conjunction with an external low pass filter. Through negative phase input and positive phase output 1H delay time is obtained for NTSC signals.

Features

- 5V single supply
- 14.3 MHz driver
- Low consumption at 160 mW (Typ.)
- Built-in peripheral circuits
- Completely adjustment free

Functions

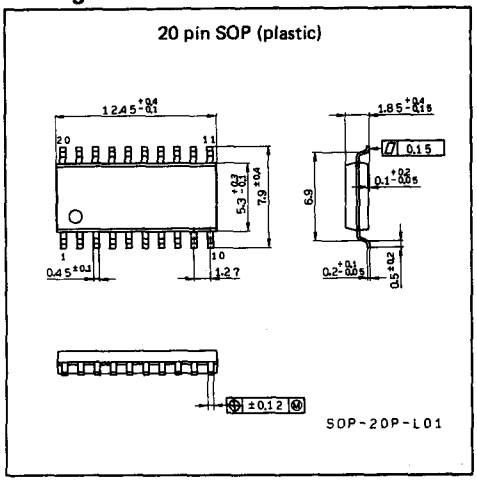
- 905.5bit CCD register
- Clock driver
- Autobias circuit
- Input clamp circuit
- Sample and hold circuit

Structure

CMOS-CCD

Package Outline

Unit: mm



Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	+6	V
• Operating temperature	Topr	−10 to +60	°C
• Storage ambient temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	500	mW

Operating Voltage Range (Ta=25°C)

	V_{DD}	5V±5%

Recommended Clock Conditions (Ta=25°C)

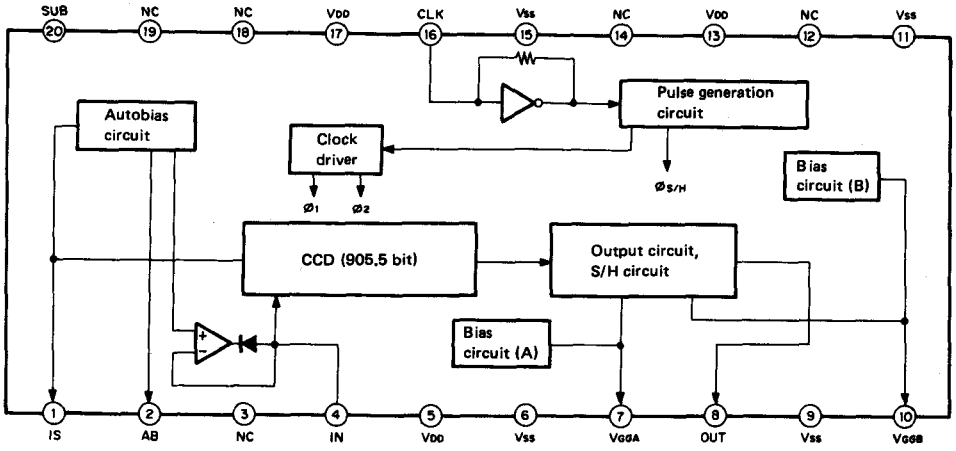
• Input clock amplitude	V_{CLK}	0.3 to 1.0	Vp-p (0.5 Vp-p Typ.)
• Clock frequency	f_{CLK}	14.318182	MHz
• Input clock waveform	sinewave		

Input Signal Amplitude

	V_{SIG}	560(Max.)	mVp-p

80128-ST

Block Diagram and Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description	Impedance [Ω]
1	IS	O	CCD bias DC output	600 to 2k
2	AB	O	Autobias DC output	2k to 20k
3	(NC)	–		
4	IN	I	Signal input (Negative phase signal)	>100k (at no clamp)
5	V_{DD}	–	5V supply (For clock driver)	
6	V_{SS}	–	GND	
7	V_{GGA}	O	Gate bias (A) DC output	2k to 10k
8	OUT	O	Signal output (positive phase signal)	40 to 500
9	V_{SS}	–	GND	
10	V_{GGB}	O	Gate bias (B) DC output	2k to 10k
11	V_{SS}	–	GND	
12	(NC)	–		
13	V_{DD}	–	5V supply (for analog system)	
14	(NC)	–		
15	V_{SS}	–	GND	
16	CLK	I	Clock input	4k to 50k
17	V_{DD}	–	5V supply (for digital system)	
18	(NC)	–		
19	(NC)	–		
20	SUB	–	GND	

Electrical Characteristics

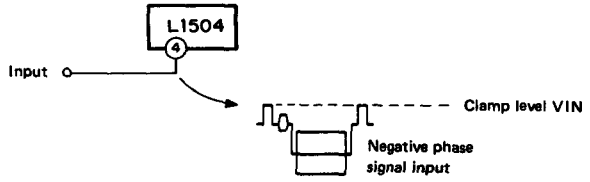
See the Electrical Characteristics Test Circuits

Ta=25°C, V_{DD}=5V, f_{CLK}=14.318182 MHz, V_{CLK}=500 mVp-p sinewave

Item	Symbol	Test conditions	SW conditions				*Note) Bias conditions	Min.	Typ.	Max.	Unit	Note
			1	2	3	4	V_{BIAS1} (V)					
Supply current	I_{DD}	–	a	a	a	–	–	20	32	42	mA	1
Insertion gain	IG	200 kHz 500 mVp-p Sinewave	a	a	a	b	–	−5.0	−3.0	−1.0	dB	2
Frequency response	fr	200 kHz ↔3.58 MHz 150 mVp-p Sinewave	b↔c	a	b	b	VIN−0.2	−2.5	−1.3	0	dB	3
Differential gain	DG	5-staircase wave (See Note 4)	d	a	a	c	–	0	3	7	%	4
Differential phase	DP	5-staircase wave (See Note 4)	d	a	a	c	–	0	3	7	deg	4
S/H pulse coupling	CP	No-signal input	–	b	b	a	VIN	–	200	350	mVp-p	5
S/N ratio	S/N	50% white video signal (See Note 7)	e	a	a	d	–	54	56	–	dB	6

***Note)** VIN is defined as follows.

VIN is the input signal clamp level, it clamps the Video signal sync tip level.



VIN is the pin voltage for pin 4 at no-input signal. Testing is executed with a voltmeter under the following SW conditions.

Item	SW Conditions				Test point
	1	2	3	4	
VIN	–	b	a	–	V1

As VIN varies with each IC, they are all subject to testing.

1) I_{DD} is the IC supply current value during clock and signal input.

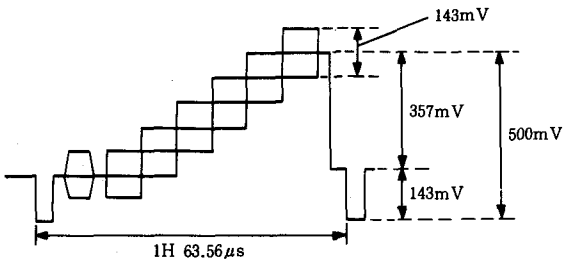
2) IG is the OUT pin output gain when a 500 mVp-p, 200 kHz sinewave is input to IN pin.

$$IG=20 \log \frac{\text{OUT pin output voltage [mVp-p]}}{500\ [\text{mVp-p}]}\ [\text{dB}]$$

3) Indicates the dissipation at 3.58 MHz in relation to 200 kHz.
From the OUT output voltage when a 150 mVp-p, 200kHz sinewave is fed to IN pin and from the OUT pin output voltage when a 150 mVp-p, 3.58 MHz sinewave is fed to same, calculation is made according to the below formula. The input part bias is tested at VIN—0.2V.

$$fr=20 \log \frac{\text{OUT pin output voltage (3.58 MHz) [mVp-p]}}{\text{OUT pin output voltage (200 kHz) [mVp-p]}} [dB]$$

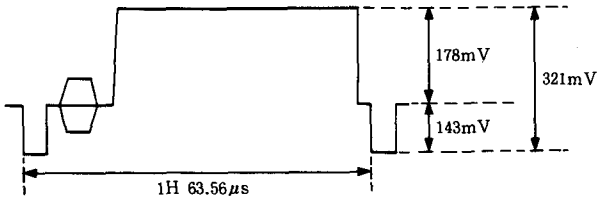
4) The differential gain (DG) and the differential phase (DP), when the 5-staircase wave in the fig. below is input are tested at the vector scope.



IN pin input waveform is the inverted waveform in the above Fig.

5) The internal clock component to the output signal during no-signal input and the leakage of that high harmonic component are tested. The input part bias is tested at VINV.

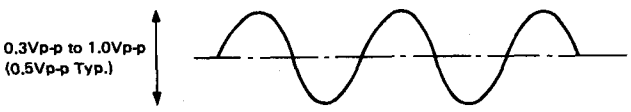
6) S/N ratio during 50% white video signal input shown in Fig. below is tested at video noise meter, in BPF 100 kHz to 4 MHz, Sub Carrier Trap mode.



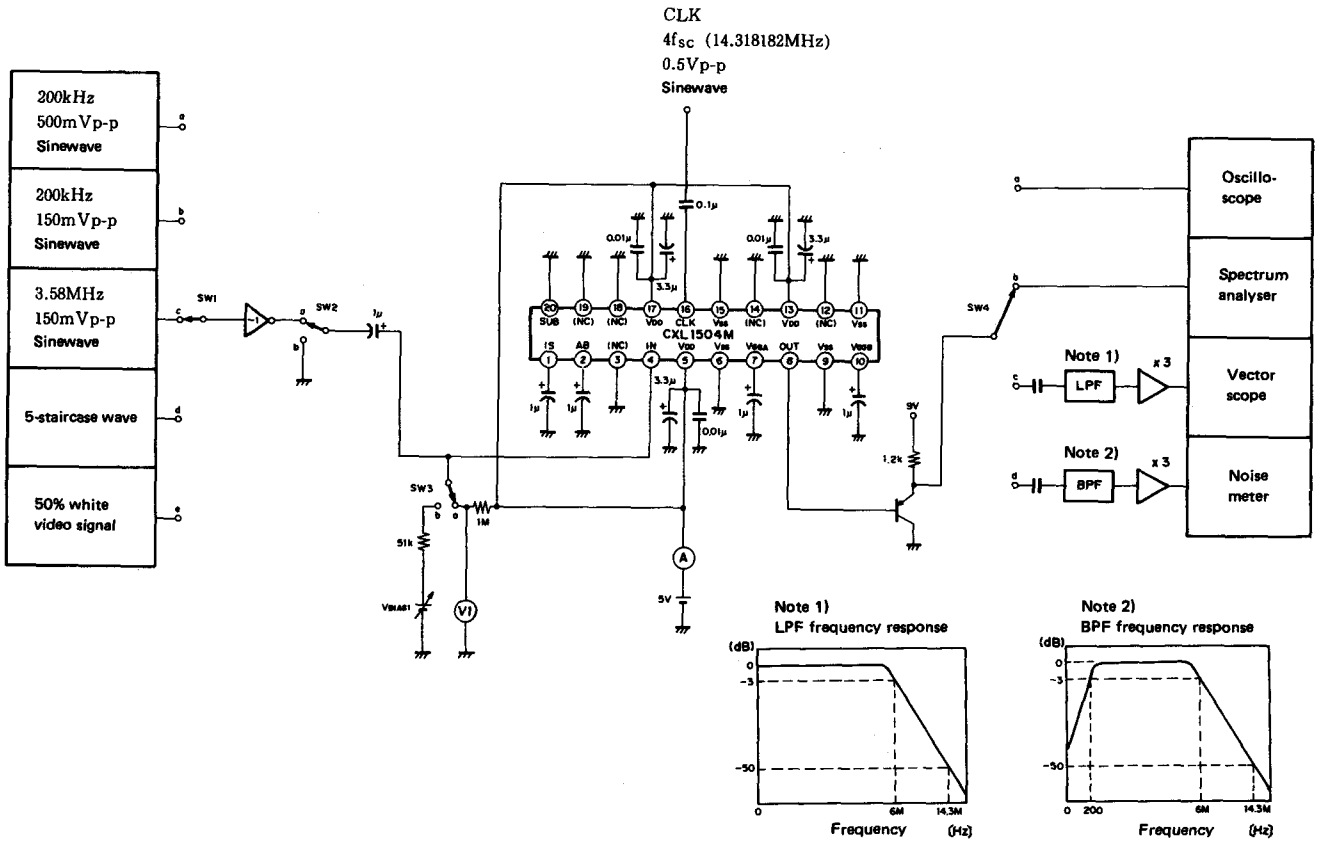
IN pin input waveform is the inverted waveform in the above Fig.

CLOCK

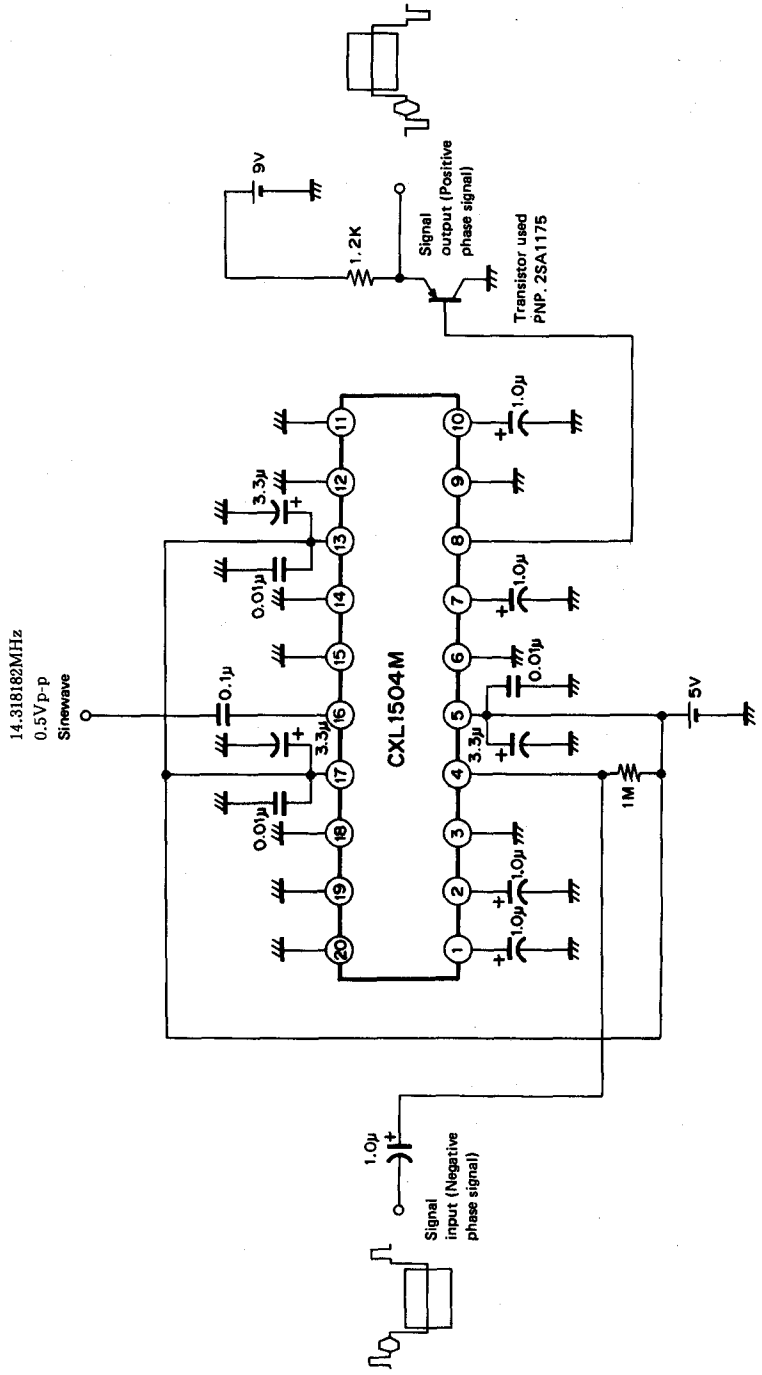
4fsc (14.318182MHz) sinewave



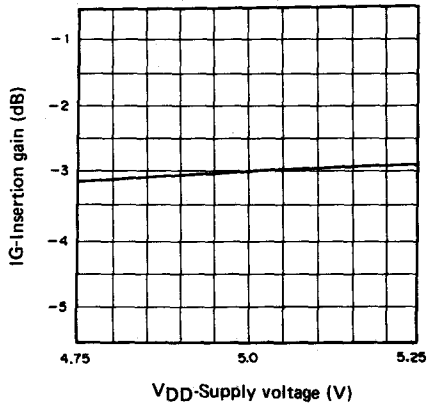
Electrical Characteristics Test Circuits



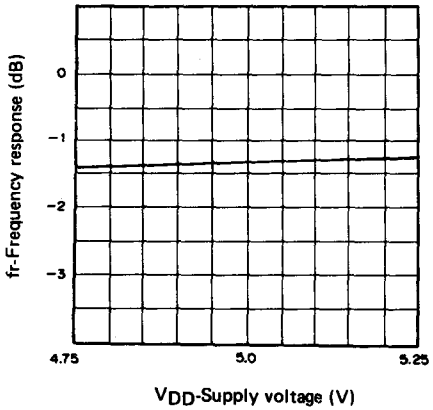
Application Circuit



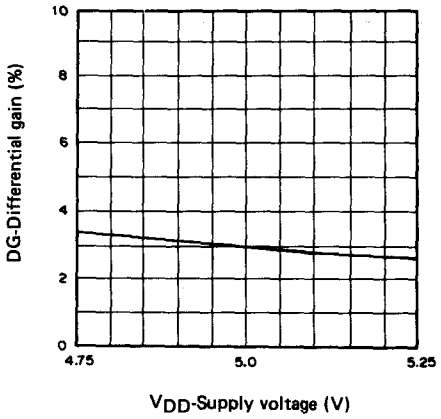
Supply voltage vs. Insertion gain



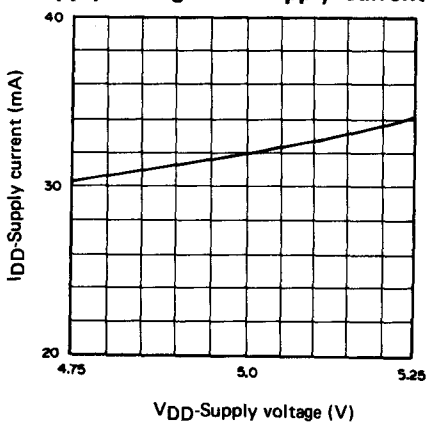
Supply voltage vs. Frequency response



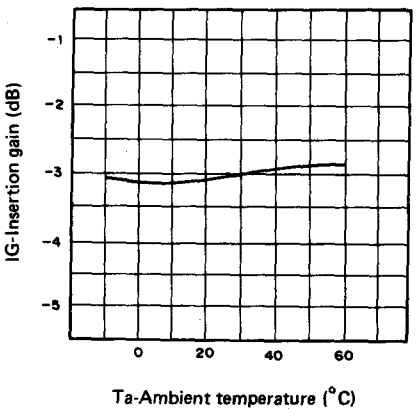
Supply voltage vs. Differential gain



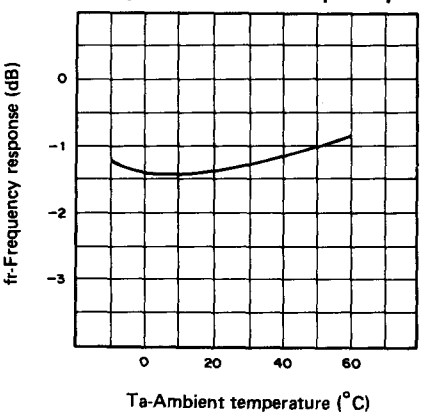
Supply voltage vs. Supply current



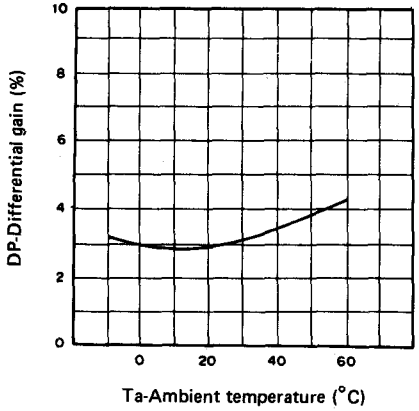
Ambient temperature vs. Insertion gain



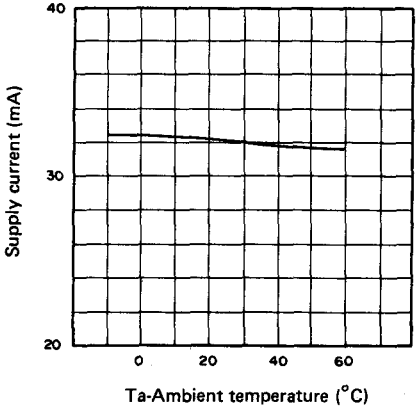
Ambient temperature vs. Frequency response



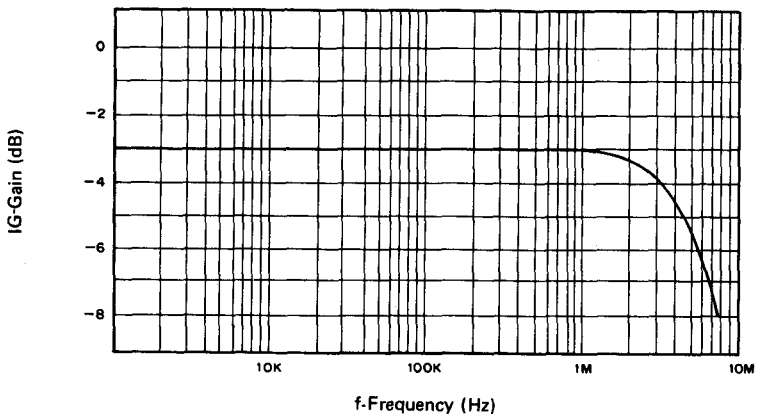
Ambient temperature vs. Differentical gain



Ambient temperature vs. Supply current



Frequency response



SONY

CXL5504M/P

CMOS-CCD 1H Delay Line for NTSC

Description

The CXL5504M/P are CMOS-CCD delay line ICs that provide 1H delay for NTSC signals including the external low pass filter.

CXL5504M	CXL5504P
8 pin SOP (Plastic)	8 pin DIP (Plastic)

Features

- Single power supply (5V)
- Low power consumption 90mW (Typ.)
- Built-in peripheral circuits
- Clamp level of input signal can be selected

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	+6	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation			
	P_D		
	CXL5504M	350	mW
	CXL5504P	480	mW

Recommended Operating Condition (Ta = 25°C)

Supply voltage	V_{DD}	5 ± 5%	V

Recommended Clock Conditions (Ta = 25°C)

• Input clock amplitude	V_{CLK}	0.4 to 1.0	Vp-p (0.5Vp-p Typ.)
• Clock frequency	f_{CLK}	14.318182	MHz
• Input clock waveform	Sine wave		

Input Signal Amplitude

V_{SIG} 500mVp-p (Typ.), 572mVp-p (Max.)
(at Internal clamp condition)

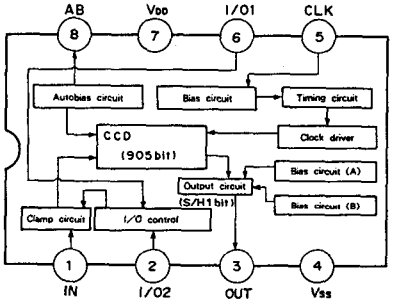
Functions

- 905-bit CCD register
- Clock driver
- Autobias circuit
- Input clamp circuit
- Sample and hold circuit

Structure

CMOS-CCD

Block Diagram and Pin Configuration (Top View)



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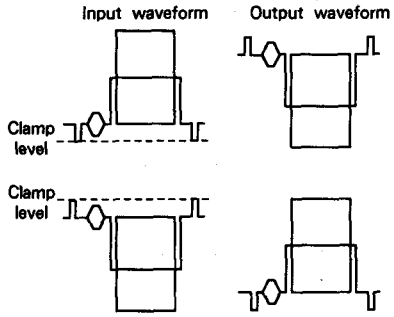
Pin Description

No.	Symbol	I/O	Description	Impedance
1	IN	I	Signal input	> 10kΩ at no clamp
2	I/O2	I	I/O control 2	
3	OUT	O	Signal output	40 to 500 Ω
4	Vss	—	GND	
5	CLK	I	Clock input	> 100kΩ
6	I/O1	I	I/O control 1	
7	V_{DD}	—	Power supply (5V)	
8	AB	O	Autobias DC output	600 to 200kΩ

Description of Function

In the CXL5504M/P, the condition of I/O control pins (Pins 2 and 6) control the input signal clamp condition and the mode of the output signal with relation to its input signal.

There are 2 modes for the I/O signal.



① PN mode
(Low level clamp/reverse phase output mode)

② NP mode
(High level clamp/positive phase output mode)

I/O Control Pin

① I/O1 (Pin 6)
Control of the I/O signal condition

DC open····Input signal is low level clamped and the output signal is inverted in relation to the input signal. As the pin is biased to 2.5V by means of the resistance inside the IC, a decoupling capacitor of around 1000pF is necessary.

GND·····Input signal is high level clamped and the output signal turns into an inverted signal.

② I/O2 (Pin 2)
Control of the input signal clamp condition

0V·····Internal clamp condition

5V·····Non internal clamp condition

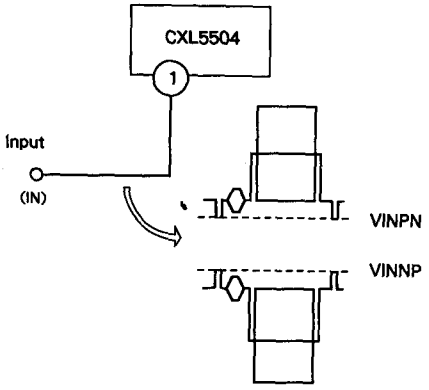
Center biased to approx. 2.1V by means of the IC internal resistance (several 10kΩ). Usage in this mode is limited to APL 50 % signals and in this mode, the maximum input signal amplitude is 200mVp-p.

Electrical Characteristics ($Ta = 25℃$, $V_{DD} = 5V$, $f_{CLK} = 14.318182MHz$, $V_{CLK} = 500mVp\text{-}p$, Sine wave)
See "Electrical Characteristics Test Circuit"

Item	Symbol	Test condition	SW condition 1	2	3	4	5	6	7	Bias condition Vbias1 (V) (NOTE 1)	Min.	Typ.	Max.	Unit	NOTE
Supply current	IDDPN	—	—	c	b	b	b	a	—	—	10	18	28	mA	2
	IDDNP					a	a								
Low frequency gain	GLPN	200kHz 500mVp-p Sine wave	a	a	b	b	b	a	b	—	−2	0	2	dB	3
	GLNP					a	a								
Frequency response	fPN	200kHz↔3.57MHz 150mVp-p Sine wave	b ↕ c	a	a	b	b	b	b	2.1	−2	−1	0	dB	4
	fNP					a	a								
Differential gain	DGPN	5-staircase wave (See Note 5)	d	a	b	b	b	a	c	—	0	5	7	%	5
	DGNP			b		a	a								
Differential phase	DPPN	5-staircase wave (See Note 5)	d	a	b	b	b	a	c	—	0	5	7	degree	5
	DPNP			b		a	a								
S/H pulse coupling	CPPN	No signal input	—	c	a	b	b	b	a	VINPN + 0.5	—	—	350	mVp-p	6
	CPNP					a	a			VINNP					
SN ratio	SNPN	50% white video signal (See Note 7)	e	a	b	b	b	a	d	—	52	56	—	dB	7
	SNNP			b		a	a								

NOTE

① VINPN and VINNP are defined as follows.
VINPN and VINNP are the input signal clamp levels of PN and NP modes clamping the video signal sync chip level.



Testing of VINPN and VINNP is executed with a voltmeter under the following SW conditions.

Item	SW condition 1	2	3	4	5	6	7	Test point
VINPN	—	c	b	b	b	a	—	V1
VINNP	—	c	b	a	a	a	—	

② This is the IC supply current value during clock and signal input.

③ GLPN, GLNP are output gain of pin OUT when a 500mVp-p, 200kHz sine wave is fed to pin IN.

(Example of calculation)

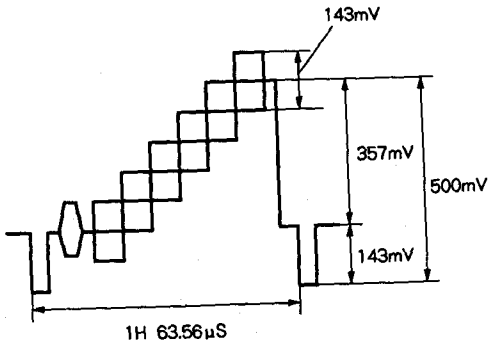
$$GLPN = 20\log \frac{\text{pin OUT output voltage (PN mode) [mVp-p]}}{500\ [\text{mVp-p}]}\ [\text{dB}]$$

④ Indicates the dissipation at 3.57MHz in relation to 200kHz.
From the output voltage at pin OUT when a 150mVp-p, 200kHz sine wave is fed to pin IN, and from the output voltage at pin OUT when a 150mVp-p, 3.57MHz sine wave is fed to same, calculation is made according to the following formula. Input bias is tested at 2.1V.

(Example of calculation)

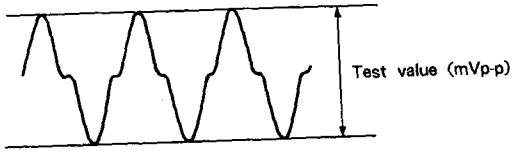
$$fPN = 20\log \frac{\text{pin OUT output voltage (PN mode, 3.57MHz) [mVp-p]}}{\text{pin OUT output voltage (PN mode, 200kHz) [mVp-p]}}\ [\text{dB}]$$

⑤ In Fig. below, differential gain (DG) and differential phase (DP) are tested with a vectorscope when the 5-staircase staircase wave is fed.

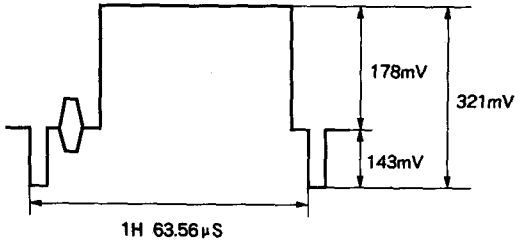


Input waveform (Input waveform of NP mode is the inverted waveform in the figure above)

⑥ Leakage of internal clock components and related high frequency components to the output signal, during no signal input. Input bias is tested at VINPN + 0.5V and VINNP for PN and NP modes respectively.



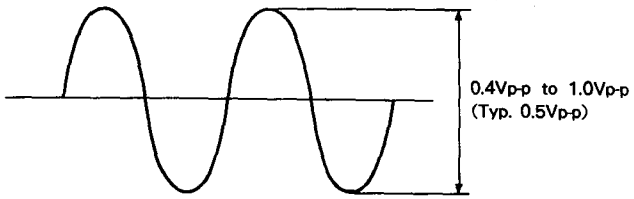
⑦ SN ratio during a 50% white video signal input shown in Fig. below is tested at a video noise meter, in BPF 100kHz to 4MHz, Sub Carrier Trap mode.



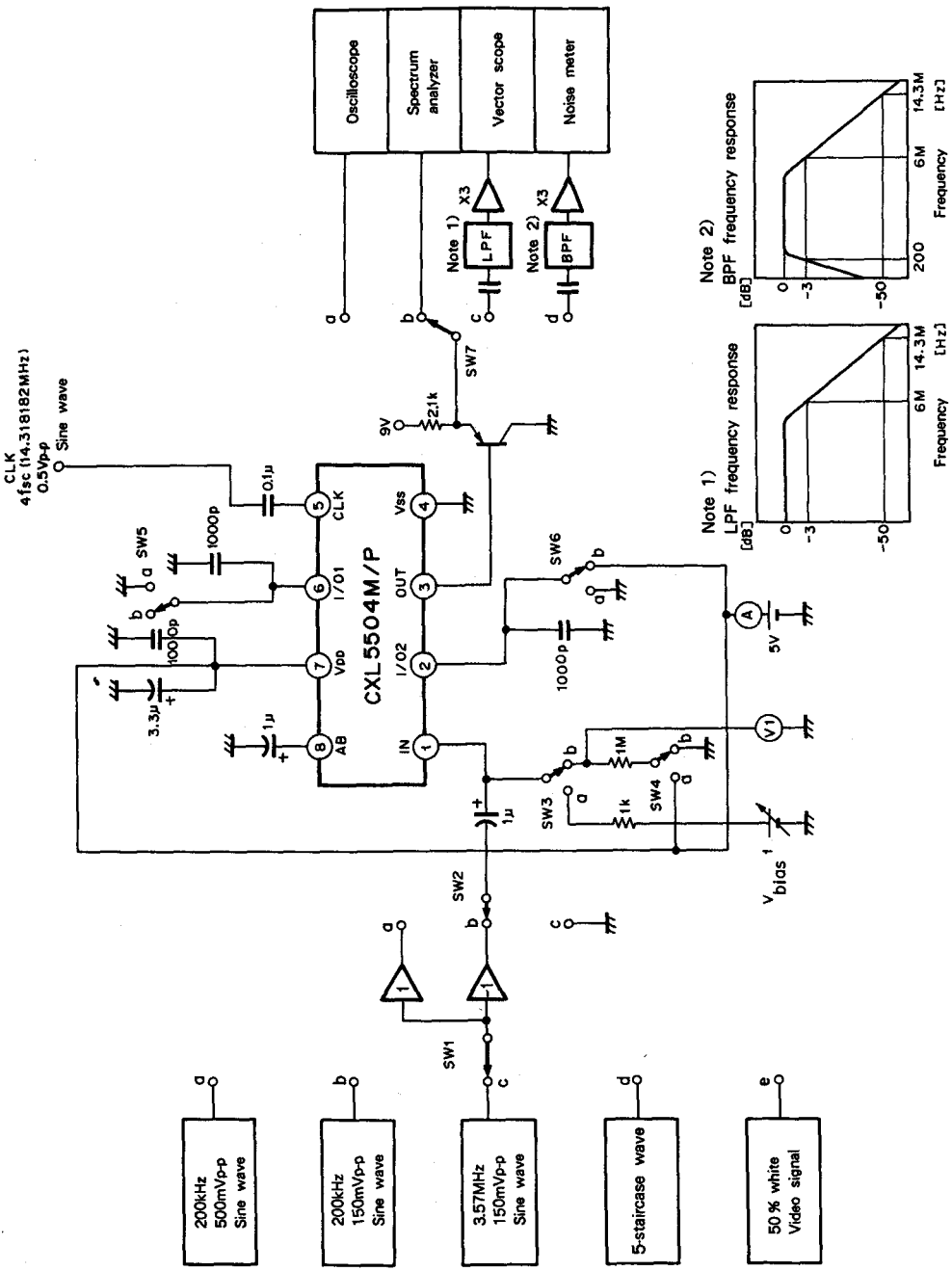
Input waveform (Input waveform of NP mode is the inverted waveform in the figure above)

CLOCK

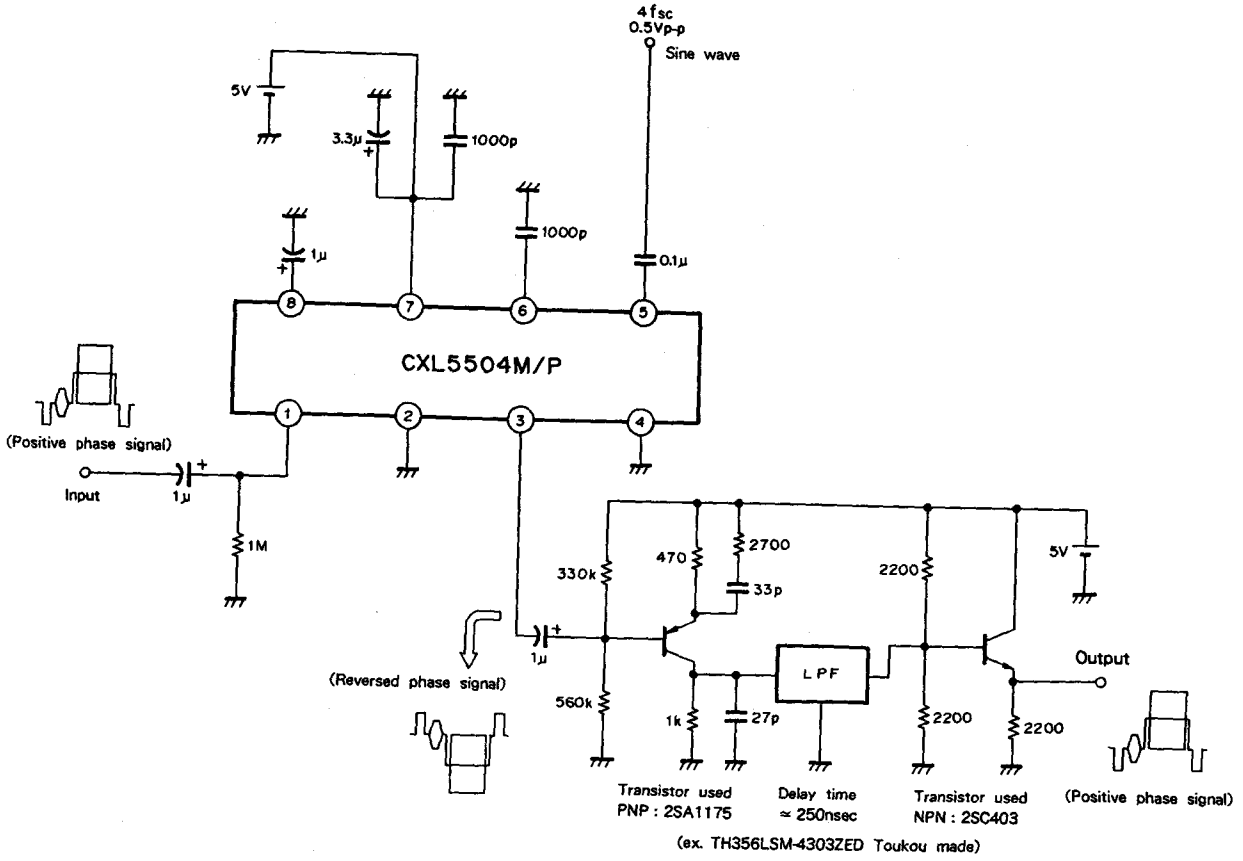
fsc (14.318182MHz) Sine wave



Electrical Characteristics Test Circuit



Application Circuit (Using PN mode)

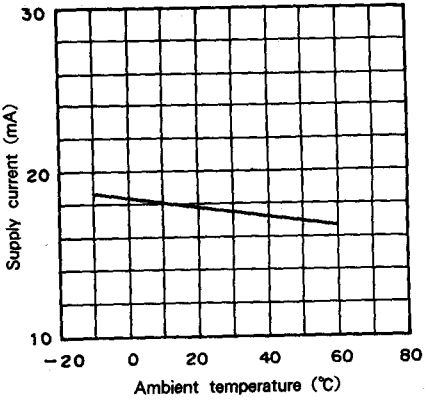


(ex. TH356LSM-4303ZED Toukou made)

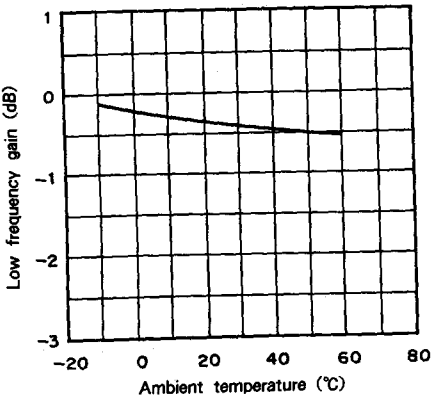
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

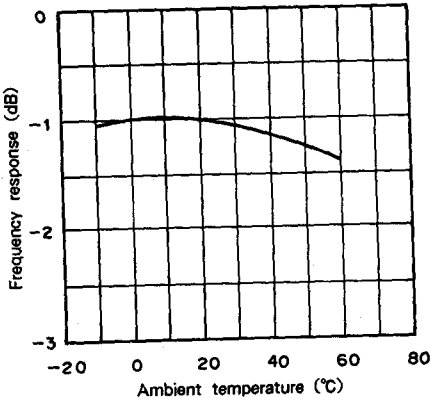
Supply current vs. Ambient temperature



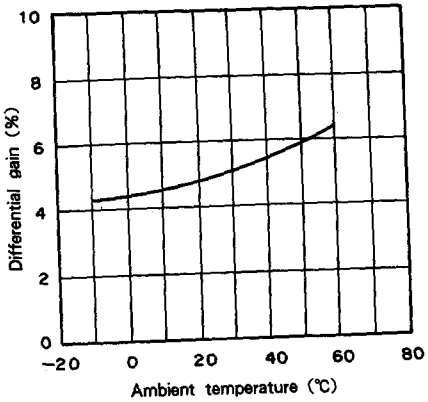
Low frequency gain vs. Ambient temperature



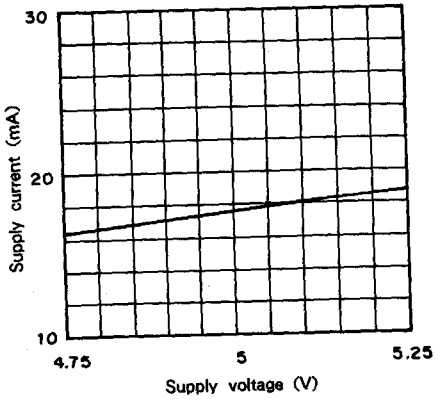
Frequency response vs. Ambient temperature



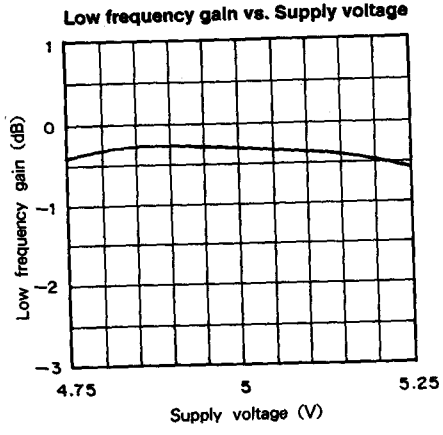
Differential gain vs. Ambient temperature



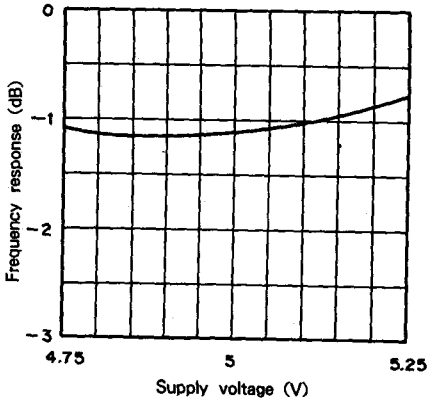
Supply current vs. Supply voltage



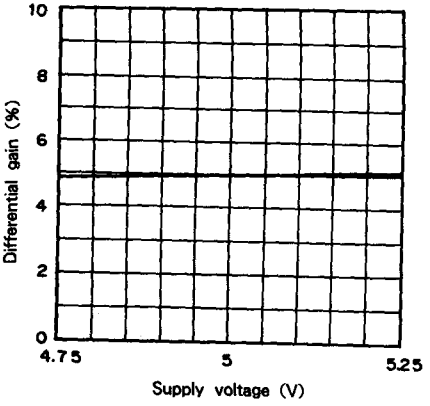
Low frequency gain vs. Supply voltage



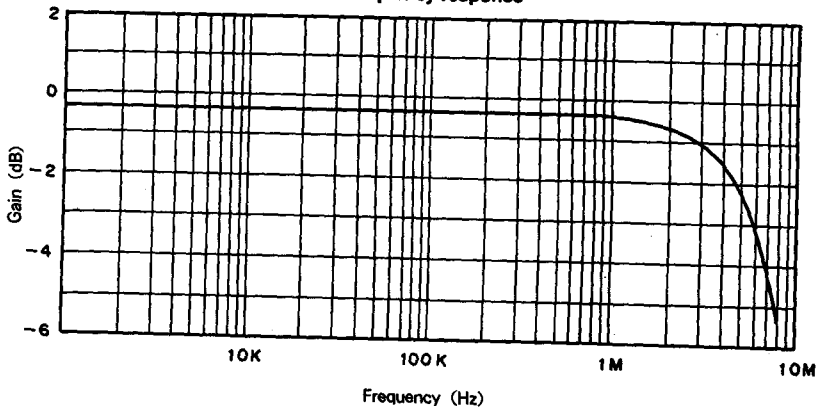
Frequency response vs. Supply voltage



Differential gain vs. Supply voltage

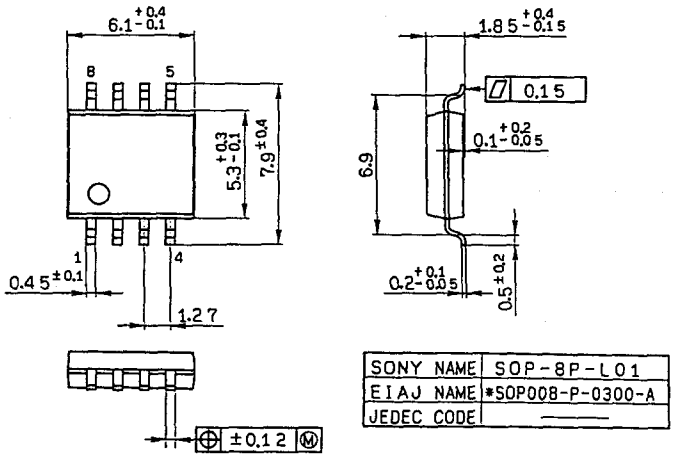


Frequency response



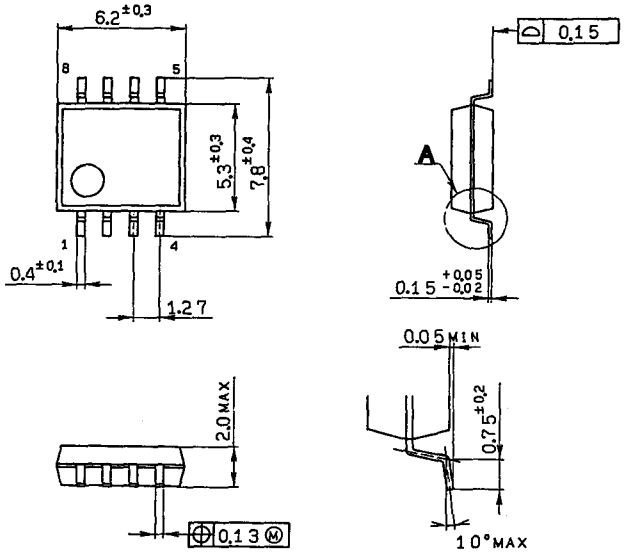
Package Outline Unit : mm

CXL5504M 8pin SOP (Plastic) 300mil 0.1g



SONY NAME	SOP-8P-L01
EIAJ NAME	*SOP008-P-0300-A
JEDEC CODE	———

8pin SOP (Plastic) 300mil

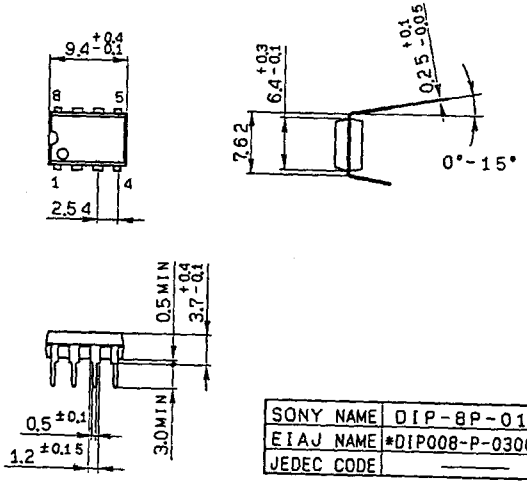


Detailed diagram of A

SONY NAME	SOP-8P-L121
EIAJ NAME	*SOP008-P-0300-AX
JEDEC CODE	———

CXL5504P

8pin DIP (Plastic) 300mil 0.5g



SONY NAME	DIP-8P-01
EIAJ NAME	*DIP008-P-0300-A
JEDEC CODE	———

CCD Delay Line

6) CCD Delay Line

Type	Applications	Functions	Page
CXL5001P/M	General purpose	3fsc, NTSC, 1H	765
CXL5002P/M		3fsc, NTSC, 1/2H	772
CXL5003P/M		3fsc, PAL, 1H	778
CXL5005P/M		3fsc, NTSC, 1H, 3 pole wiht PLL	785
CXL5502M/P		4fsc, NTSC, 1H, 4 pole with PLL	791
CXL5504M/P		4fsc, NTSC, 1H	751
CXL5505M/P		4fsc, PAL, 1H, 4 pole with PLL	802
CXL5506M/P		4fsc, PAL, 1H	811
CXL5507M/P		2fsc, NTSC, 1H	820
CXL5508M/P		2fsc, PAL, 1H	829
CXL5509M/P	1H, 2H CCD delay line for NTSC	1 input and 2 outputs (1H delay, 2H delays). Built-in quadrupre progression PLL circuit	838
CXL1009P	Video disk	TBC, 15.2 to 27.2MHz drive, 680-bit×2	846
CXL1008P/M	8mm VCR	Skew correction (3fsc, 1/2H), 359-bit, 20-bit	855
CXL1501M		4fsc, NTSC comb filter	867
CXL1502M		3fsc, PAL comb filter	878
CXL1506M		3fsc, PAL 1H/2H output, with PLL	890
CXL1503M CXL1505M	8mm VCR	301.5-bit×4 (4/3fsc, 1H) 453.5-bit×4 (2fsc, 1H)	721
CXL1504M	8mm VCR	905.5-bit (4fsc, 1H)	743
CXL1517M CXL1518M	Color video camera	452.5-bit×2, 453.5-bit×1 (2fsc, 1H)/ 300.5-bit×2, 301.5-bit×1 (4/3fsc, 1H)	729
CXL1517N CXL1518N	Color video camera		736

SONY CXL5001P/CXL5001M

CMOS-CCD 1H Delay Line for NTSC

Description

The CXL5001P/CXL5001M are general purpose CCD delay line ICs which provide 1H delay time of NTSC.

Features

- Low power dissipation 80 mW (typical)
- Small size package (8-pin DIP, MFP)
- Low differential gain DG=3% (typical)
- Input signal amplitude 180IRE (=1.28Vp-p, max.)
- Low input clock amplitude operation 150 mVp-p (min.)
- On chip peripheral circuits.

Functions

- 680 bit CCD register
- Clock drivers
- Autobias circuit
- Synchronized tip clamp circuit
- Sample and hold circuit

Absolute Maximum Ratings (Ta=25°C)

• Power supply voltage 1	V_{DD}	11	V
• Power supply voltage 2	V_{CL}	6	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	CXL5001P 480	mW
		CXL5001M 350	mW

Recommended Operating Conditions

V_{DD}	9V±5%
V_{CL}	5V±5%

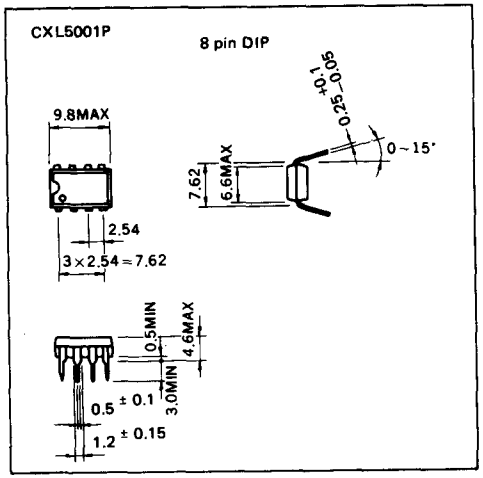
Recommended Clock Conditions

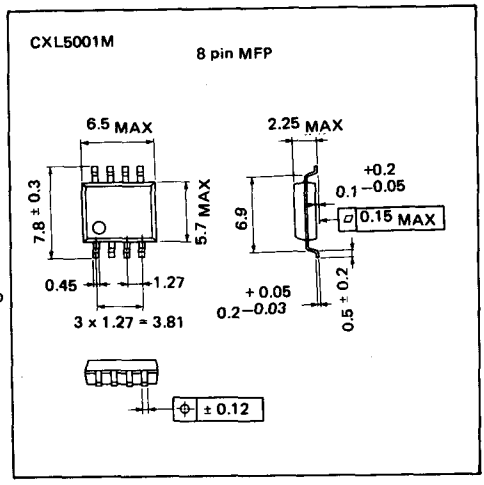
• Input clock amplitude	V_{CK}	150 mVp-p to 1.0 Vp-p (Typical 250 mVp-p)
• Clock frequency	f_{CK}	10.7 MHz

Structure

CMOS-CCD

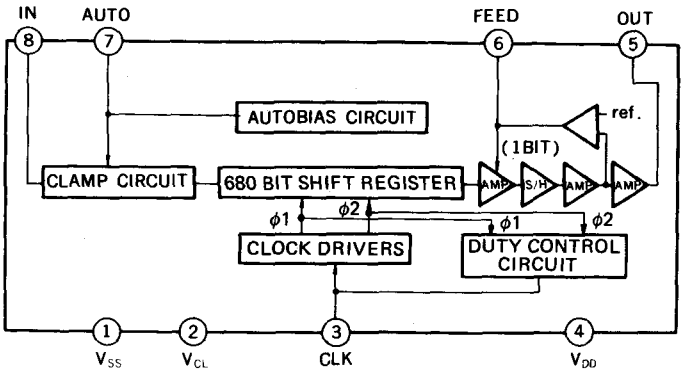
Package Outline Unit: mm





50656-ST

Block Diagram



Pin Description

Pin No.	Symbol	Description	Impedance [Ω]	Pin No.	Symbol	Description	Impedance [Ω]
1	V_{SS}	GND		5	OUT	Signal output	600 to 1k
2	V_{CL}	5V power supply		6	FEED	Feedback DC output	>100k
3	CLK	Clock input	>100k	7	AUTO	Autobias DC output	10k
4	V_{DD}	9V power supply		8	IN	Signal input	>100k

6) CCD Delay Line

Type	Applications	Functions	Page
CXL5001P/M	General purpose	3fsc, NTSC, 1H	765
CXL5002P/M		3fsc, NTSC, 1/2H	772
CXL5003P/M		3fsc, PAL, 1H	778
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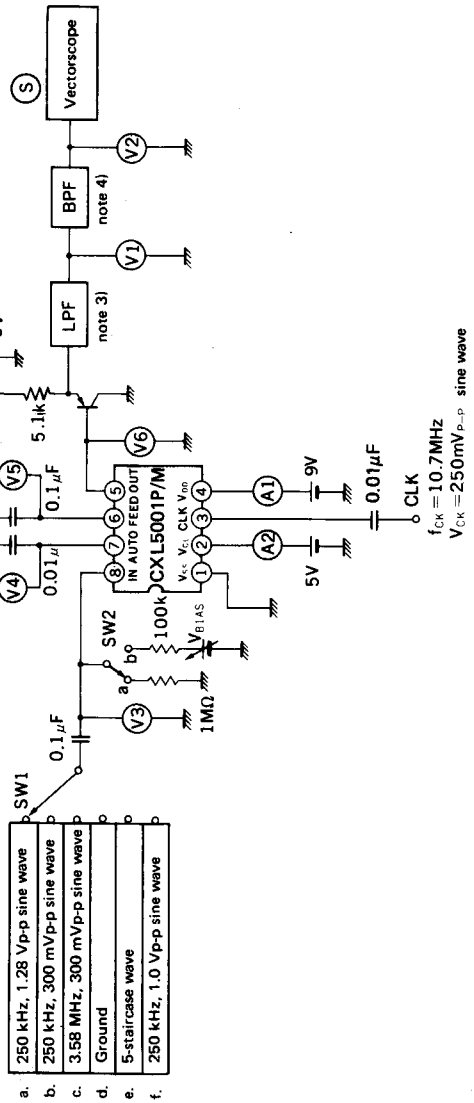
CXL5502M/P		4fsc, NTSC, 1H, 4 pole with PLL	791
CXL5504M/P		4fsc, NTSC, 1H	751
CXL5505M/P		4fsc, PAL, 1H, 4 pole with PLL	802
CXL5506M/P		4fsc, PAL, 1H	811
CXL5507M/P		2fsc, NTSC, 1H	820
CXL5508M/P		2fsc, PAL, 1H	829
CXL5509M/P	1H, 2H CCD delay line for NTSC	1 input and 2 outputs (1H delay, 2H delays). Built-in quadrupre progression PLL circuit	838
CXL1009P	Video disk	TBC, 15.2 to 27.2MHz drive, 680-bit×2	846
CXL1008P/M	8mm VCR	Skew correction (3fsc, 1/2H), 359-bit, 20-bit	855
CXL1501M		4fsc, NTSC comb filter	867
CXL1502M		3fsc, PAL comb filter	878
CXL1506M		3fsc, PAL 1H/2H output, with PLL	890
CXL1503M CXL1505M	8mm VCR	301.5-bit×4 (4/3fsc, 1H) 453.5-bit×4 (2fsc, 1H)	721
CXL1504M	8mm VCR	905.5-bit (4fsc, 1H)	743
CXL1517M CXL1518M	Color video camera	452.5-bit×2, 453.5-bit×1 (2fsc, 1H)/ 300.5-bit×2, 301.5-bit×1 (4/3fsc, 1H)	729
CXL1517N CXL1518N	Color video camera		736

Electrical Characteristics

(Ta=25°C, V_{DD}=9.0V, V_{CL}=5.0V, f_{CK}=10.7 MHz. V_{CK}=250 mVp-p sine wave, See "Electrical characteristics measuring circuit")

Item	Symbol	Measuring condition	SW condition		Measuring point	Min.	Typ.	Max.	Unit
			SW1	SW2					
Supply current	I_{DD}	INPUT=250 kHz, 1.28 Vp-p.	a	a	A1	—	4	5	mA
	I_{CL}				A2	—	9	11	mA
Insertion gain	IG	INPUT=250 kHz, 1.28 Vp-p IG=20log (Output voltage [Vp-p]/ 1.28[Vp-p])	a	a	V1	−3	0	3	dB
Frequency response	fG	fG=20log ($V_{3.58\ MHz}$/ $V_{250\ kHz}$) (Note 1)	b,c	b	V1	−3.0	−2.1	—	dB
Differential gain	DG	5-staircase wave input Y=140IRE (=1.0 Vp-p) Measure S point with vectorscope (Note 2)	e	a	S	—	3	5	%
Differential phase	DP					—	3	5	deg
Allowable input amplitude	V_{IN-AC}		—	—	—	—	—	1.28	Vp-p
Noise	S/N	S: input=250 kHz 1.0 Vp-p output (Vp-p)	f	a	V2	55	60	—	dB
		N: input=DC output (Vrms)	d	a	V2				
Output DC voltage	V_{IN-AC}		d	a	V3	3.5	5.0	6.5	V
	$V_{AUTO-DC}$				V4	3.5	5.0	6.5	V
	$V_{FEED-DC}$	INPUT=250 kHz, 1.28 Vp-p.	a	a	V5	1.3	2.3	3.3	V
	V_{OUT-DC}				V6	1.7	2.7	3.7	V

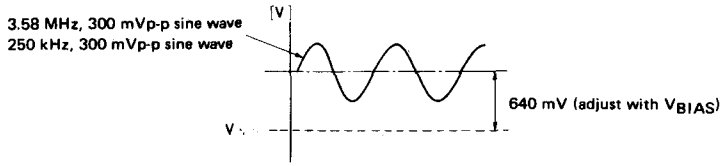
Electrical Characteristics Measuring Circuit



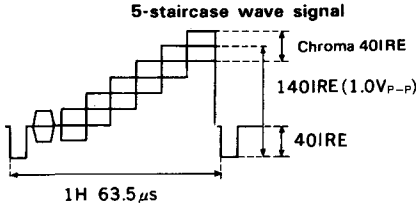
Note 1) Frequency characteristics measuring condition

$V_{3.58\,MHz}$ (Output signal voltage [Vp-p] at 3.58 MHz input)
$V_{250\,kHz}$ (Output signal voltage [Vp-p] at 250 kHz input)

Set pin 8 (IN) voltage [V] = $V_{IN\text{-}DC}$ + 640 mV.



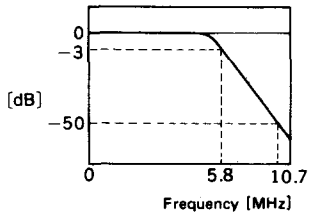
Note 2) Differential gain and differential phase measuring condition



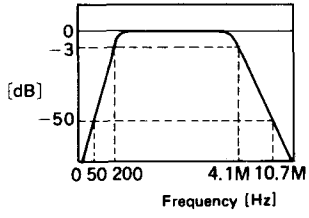
DG and DP are measured at output S point by vectorscope.

Note 3) LPF frequency characteristics

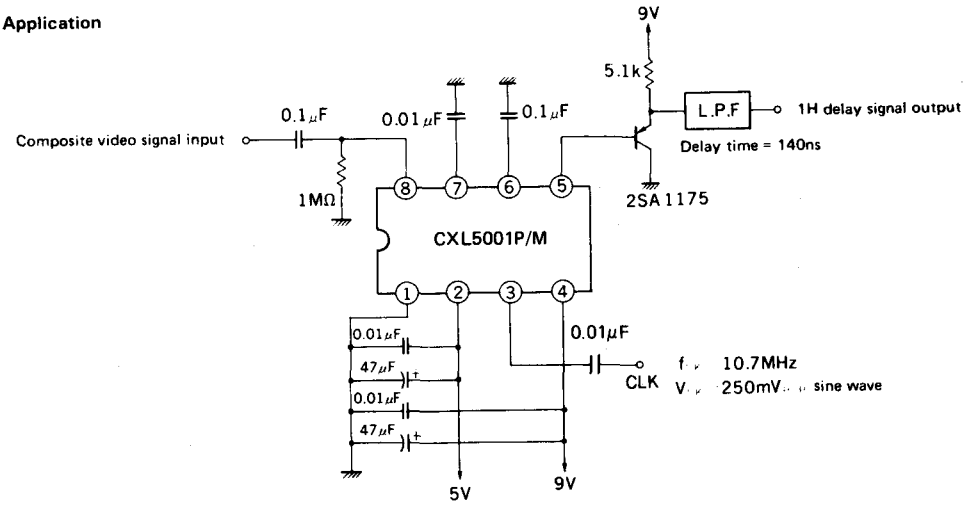
(Delay time ≃ 140ns)



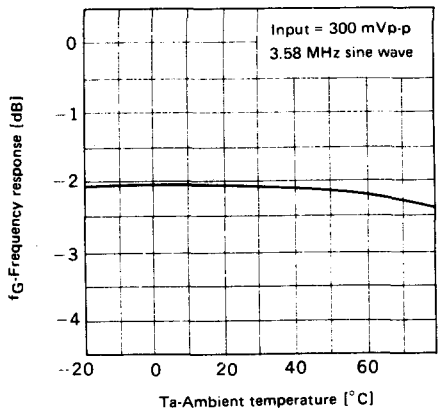
Note 4) BPF frequency characteristics



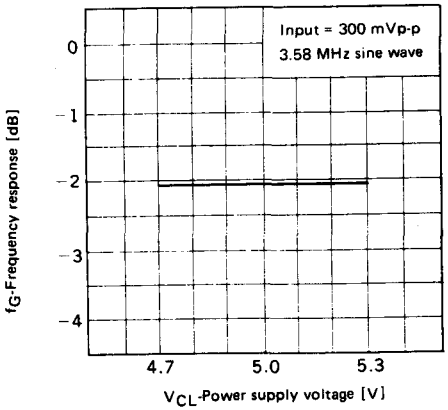
Application



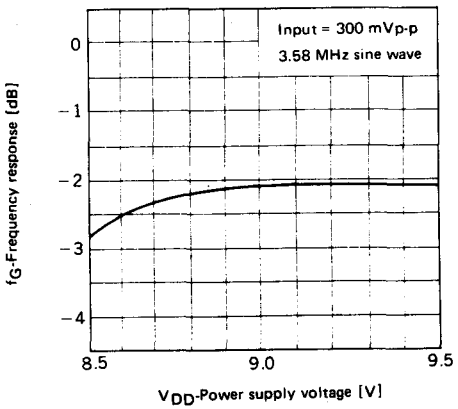
Frequency response vs. Ambient temperature



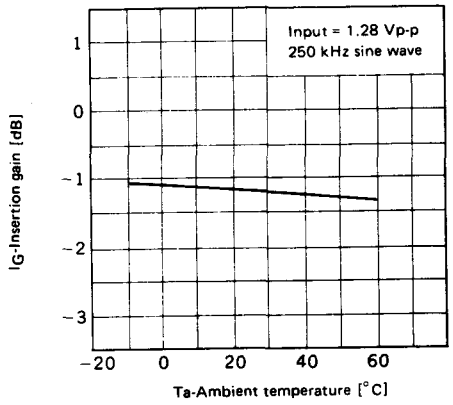
Frequency response vs. Power supply voltage



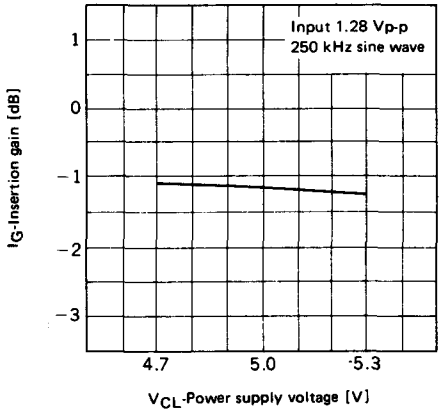
Frequency response vs. Power supply voltage



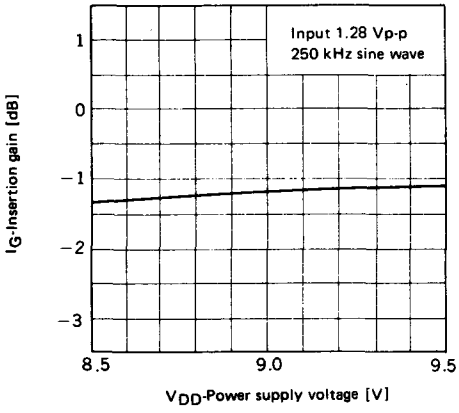
Insertion gain vs. Ambient temperature



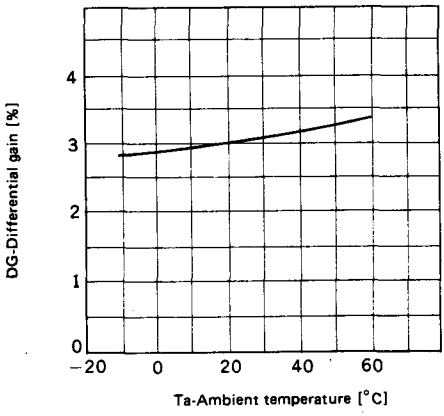
Insertion gain vs. Power supply voltage



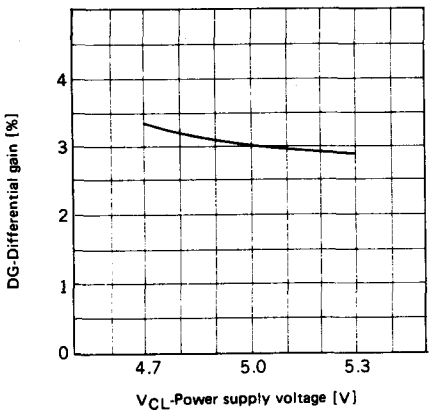
Insertion gain vs. Power supply voltage



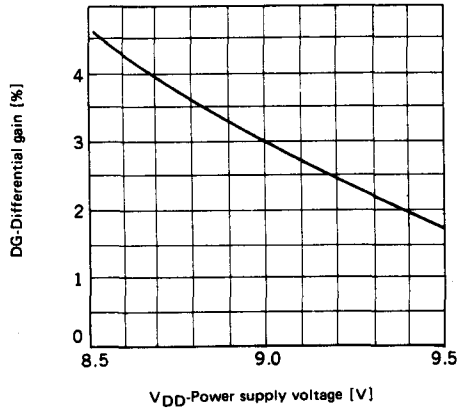
Differential gain vs. Ambient temperature



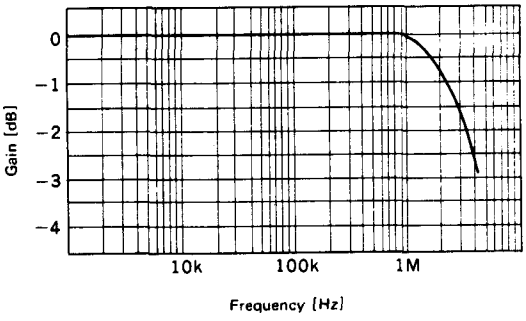
Differential gain vs. Power supply voltage



Differential gain vs. Power supply voltage



Frequency response



SONY

CXL5002P/M

CMOS-CCD 1/2H Delay Line for NTSC

Description

CXL5002P/CXL5002M are general purpose CCD delay line ICs which provide 1/2H delay time of NTSC.

Features

- Low power dissipation 70mW (Typ.)
- Small size package (8 pin DIP, SOP)
- Low differential gain DG = 3% (Typ.)
- Input signal amplitude 180IRE (= 1.28Vp-p, Max.)
- Low input clock amplitude operation 150mVp-p (Min.)
- On chip peripheral circuits.

Structure

CMOS-CCD

Functions

- 340 bit CCD register
- Clock drivers
- Autobias circuit
- Synchronous Signal tip clamp circuit
- Sample and hold circuit

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage 1	V_{DD}	11	V
• Supply voltage 2	V_{CL}	6	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation			
P_D CXL5002P		480	mW
CXL5002M		350	mW

Recommended Operating Conditions

V_{DD}	9V ± 5%
V_{CL}	5V ± 5%

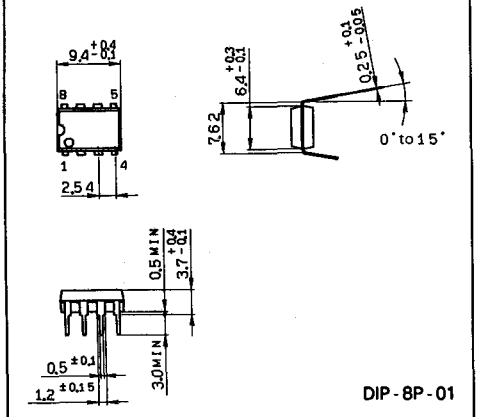
Recommended Clock Conditions

- Input clock amplitude V_{CK} 150mVp-p to 1.0Vp-p (250mVp-p Typ.)
- Clock frequency f_{CK} 10.7 MHz

Package Outline

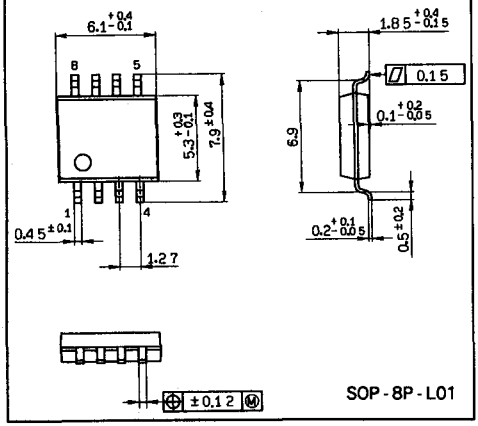
Unit : mm

CXL5002P 8 pin DIP



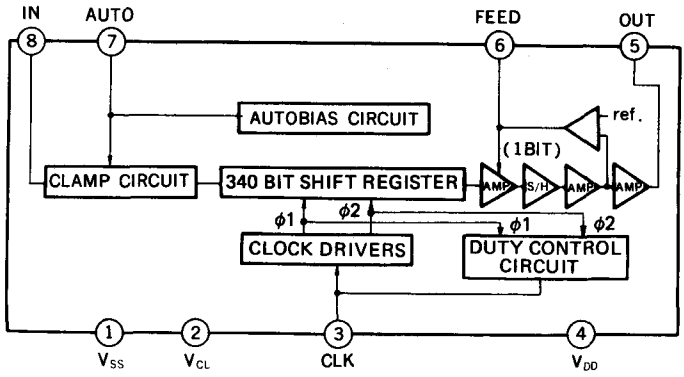
DIP-8P-01

CXL5002M 8 pin SOP



SOP-8P-L01

Block Diagram



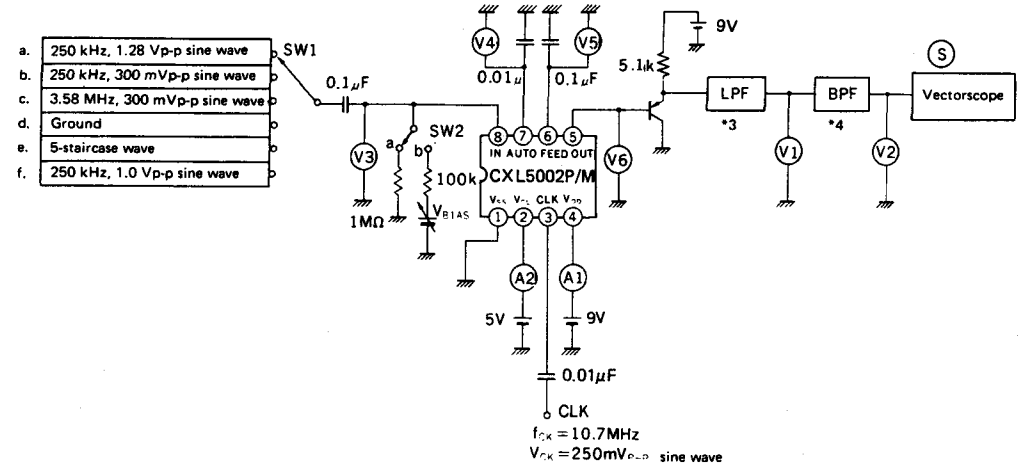
Pin Description

No.	Symbol	Description	Impedance [Ω]	No.	Symbol	Description	Impedance [Ω]
1	V_{SS}	GND		5	OUT	Signal output	600 to 1k
2	V_{CL}	5V power supply		6	FEED	Feedback DC output	>100k
3	CLK	Clock input	>100k	7	AUTO	Autobias DC output	10k
4	V_{DD}	9V power supply		8	IN	Signal input	>100k

Electrical Characteristics (Ta=25°C, V_{DD}=9.0V, V_{CL}=5.0V, f_{CK}=10.7 MHz. V_{CK}=250 mVp-p sine wave, See ,, See "Electrical characteristics test circuit")

Item	Symbol	Measuring condition	SW condition		Measuring point	Min.	Typ.	Max.	Unit
			SW1	SW2					
Supply current	I_{DD}	INPUT=250 kHz, 1.28 Vp-p.	a	a	A1	—	4	5	mA
	I_{CL}				A2	—	7	9	mA
Insertion gain	IG	INPUT=250 kHz, 1.28 Vp-p IG=20log (Output voltage [Vp-p]/ 1.28[Vp-p])	a	a	V1	−3	0	3	dB
Frequency response	fG	fG=20log ($V_{3.58\ MHz}$/ $V_{250\ kHz}$) *1	b,c	b	V1	−3.0	−2.1	—	dB
Differential gain	DG	5-staircase wave input Y=140IRE (=1.0 Vp-p) Measure S point with vectorscope *2	e	a	S	—	3	5	%
Differential phase	DP					—	3	5	deg
Allowable input amplitude	V_{IN-AC}		—	—	—	—	—	1.28	Vp-p
Noise	S/N	S: input=250 kHz 1.0 Vp-p output (Vp-p)	f	a	V2	55	60	—	dB
		N: input=DC output (Vrms)	d	a	V2				
Output DC voltage	V_{IN-AC}	INPUT=250 kHz, 1.28 Vp-p.	d	a	V3	3.5	5.0	6.5	V
	$V_{AUTO-DC}$				V4	3.5	5.0	6.5	V
	$V_{FEED-DC}$		a	a	V5	1.3	2.3	3.3	V
	V_{OUT-DC}				V6	1.7	2.7	3.7	V

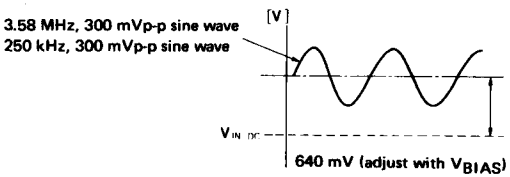
Electrial Characteristics Test Circuit



Note *1. Frequency characteristics measuring condition

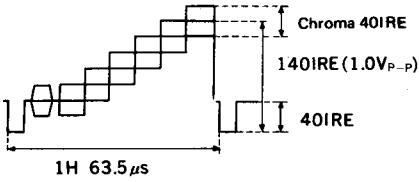
$V_{3.58\ MHz}$ (Output signal voltage [Vp-p] at 3.58 MHz input)
$V_{250\ kHz}$ (Output signal voltage [Vp-p] at 250 kHz input)

Set pin 8 (IN) voltage [V] = $V_{IN\text{-}DC}$ + 640 mV.



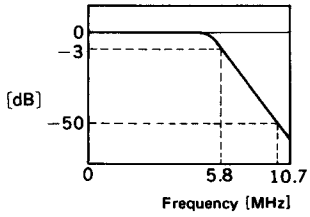
***2. Differential gain and differential measuring phase measuring condition**

5-staircase wave signal

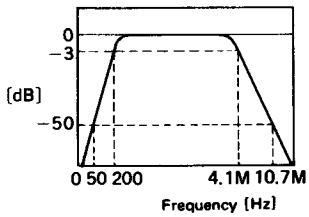


DG and DP are measured at output S point by vectorscope.

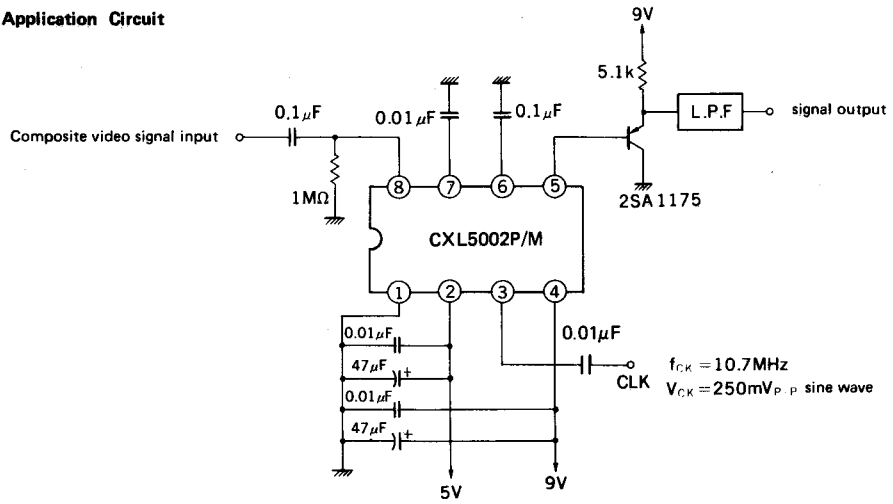
***3. LPF frequency characteristics**



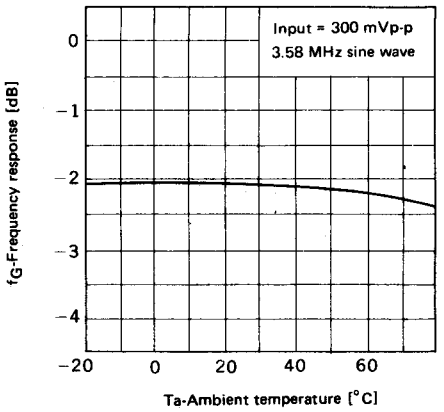
***4. BPF frequency characteristics**



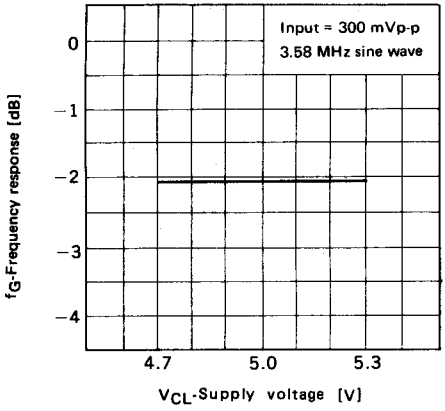
Application Circuit



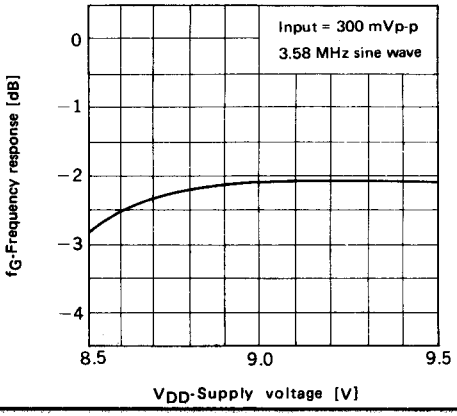
Frequency response vs. Ambient temperature



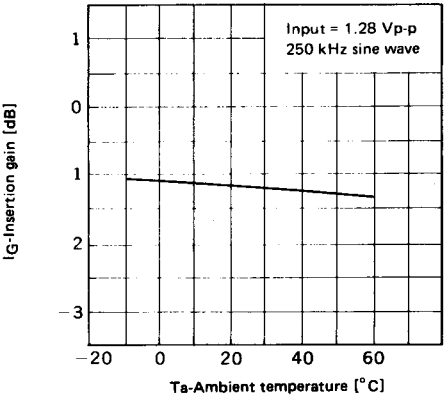
Frequency response vs. Supply voltage



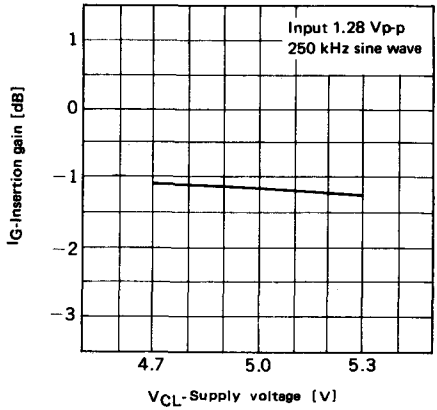
Frequency response vs. Supply voltage



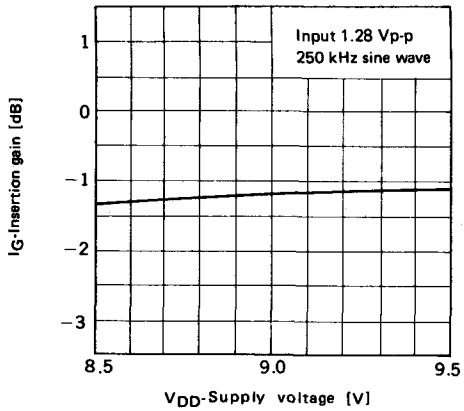
Insertion gain vs. Ambient temperature



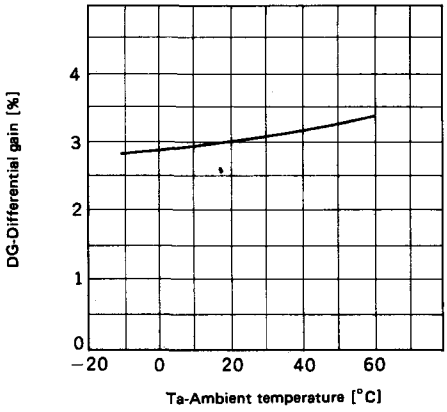
Insertion gain vs. Supply voltage



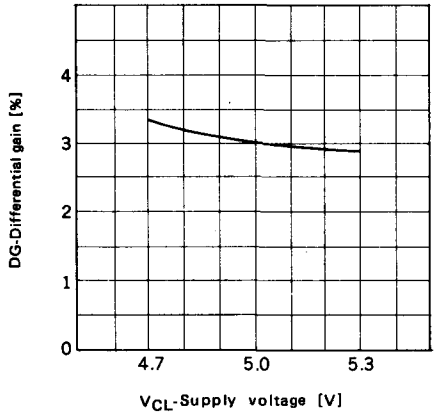
Insertion gain vs. Supply voltage



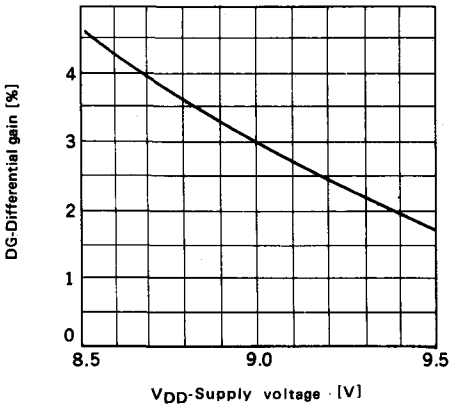
Differential gain vs. Ambient temperature



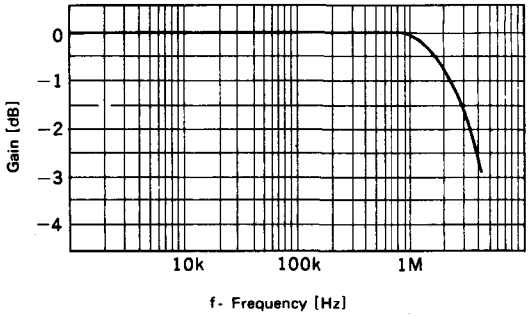
Differential gain vs. Supply voltage



Differential gain vs. Supply voltage



Frequency response



SONY

CXL5003P/M

CMOS-CCD 1H Delay Line for PAL

Description

CXL5003P/CXL5003M are general purpose CCD delay line ICs which provide 1H delay time of PAL.

Features

- Low power dissipation 110 mW (Typ.)
- Small size package (8-pin DIP, SOP)
- Low differential gain DG=3% (Typ.)
- Input signal amplitude 180IRE (=1.28 Vp-p, Max.)
- Low input clock amplitude operation 150 mVp-p (Min.)
- On chip peripheral circuits

Structure

CMOS-CCD

Functions

- 848 bit CCD register
- Clock drivers
- Autobias circuit
- Synchronized tip clamp circuit
- Sample and hold circuit

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	11	V
• Supply voltage	V_{CL}	6	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation			
	P_D CXL5003P	480	mW
	CXL5003M	350	mW

Recommended Operating Conditions

• Supply voltage	V_{DD}	9V±5%
	V_{CL}	5V±5%

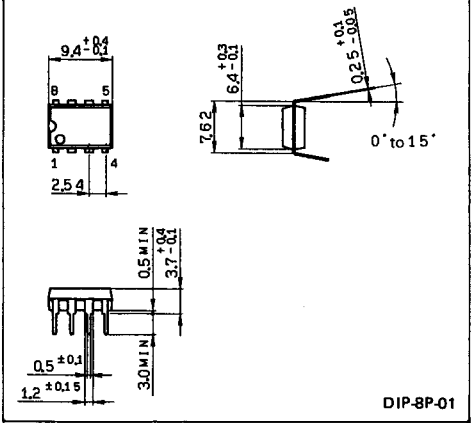
Recommended Clock Conditions

• Input clock amplitude	V_{CK}	150 mVp-p to 1.0 Vp-p (250 mVp-p Typ.)	
• Clock frequency	f_{CK}	13.3	MHz

Package Outline

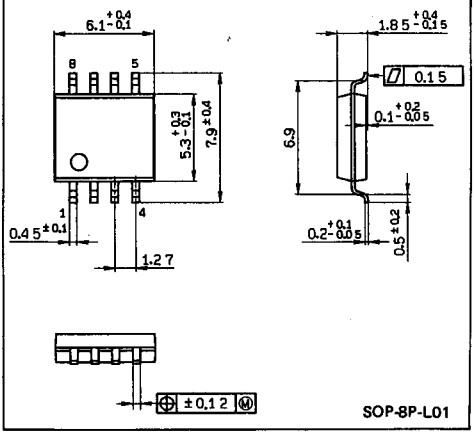
Unit: mm

CXL5003P 8 Pin DIP (Plastic)



DIP-8P-01

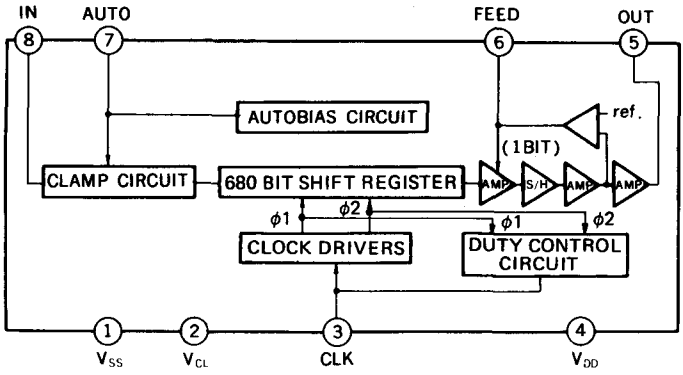
CXL5003M 8 Pin SOP (Plastic)



SOP-8P-L01

51221A-ST

Block Diagram



Pin Description

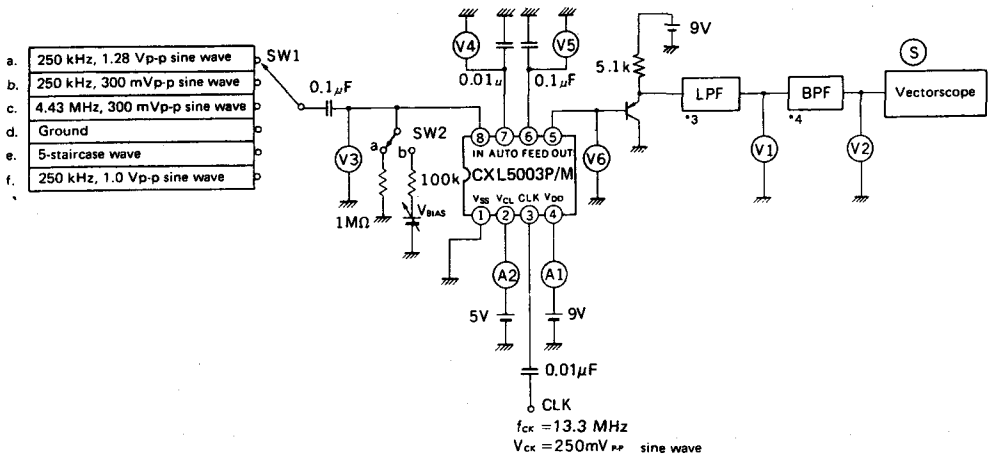
No.	Symbol	Description	Impedance [Ω]	No.	Symbol	Description	Impedance [Ω]
1	V_{SS}	GND		5	OUT	Signal output	600 to 1k
2	V_{CL}	5V power supply		6	FEED	Feedback DC output	>100k
3	CLK	Clock input	>100k	7	AUTO	Autobias DC output	10k
4	V_{DD}	9V power supply		8	IN	Signal input	>100k

Electrical Characteristics

(Ta=25°C, V_{DD}=9.0V, V_{CL}=5.0V, f_{ck}=13.3 MHz, V_{ck}=250 mVp-p sine wave, See "Electrical characteristics test circuit")

Item	Symbol	Measuring condition	SW condition		Measuring point	Min.	Typ.	Max.	Unit
			SW1	SW2					
Supply current	I_{DD}	INPUT=250 kHz, 1.28 Vp-p.	a	a	A1	—	4	5	mA
	I_{CL}				A2	—	14	16	mA
Insertion gain	IG	INPUT=250 kHz, 1.28 Vp-p IG=20log (Output voltage [Vp-p]/ 1.28[Vp-p])	a	a	V1	−3	0	3	dB
Frequency response	fG	fG=20 log ($V_{4.43\ MHz}$/ $V_{250\ kHz}$) *1	b,c	b	V1	−3.0	−2.1	—	dB
Differential gain	DG	5-staircase wave input Y=140IRE (=1.0 Vp-p) Measure S point with vectorscope *2	e	a	S	—	3	5	%
Differential phase	DP					—	3	5	deg
Allowable input amplitude	V_{IN-AC}		—	—	—	—	—	1.28	Vp-p
Noise	S/N	S: input=250 kHz 1.0 Vp-p output (Vp-p)	f	a	V2	55	60	—	dB
		N: input=DC output (Vrms)	d	a	V2				
Output DC voltage	V_{IN-AC}		d	a	V3	3.5	5.0	6.5	V
	$V_{AUTO-DC}$				V4	3.5	5.0	6.5	V
	$V_{FEED-DC}$	INPUT=250 kHz, 1.28 Vp-p.	a	a	V5	1.3	2.3	3.3	V
	V_{OUT-DC}				V6	1.7	2.7	3.7	V

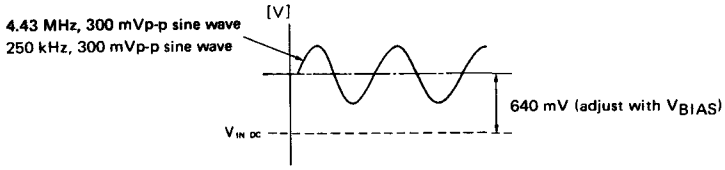
Electrical Characteristics Test Circuit



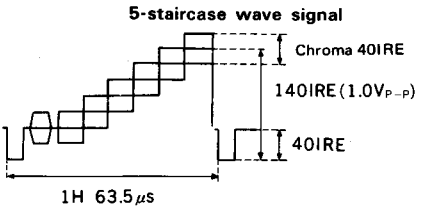
Note *1. Frequency characteristics measuring condition

$V_{4.43\ MHz}$ (Output signal voltage [Vp-p] at 4.43 MHz input)
$V_{250\ kHz}$ (Output signal voltage [Vp-p] at 250 kHz input)

Set pin 8 (IN) voltage [V] = $V_{IN\text{-}DC}$ + 640 mV.

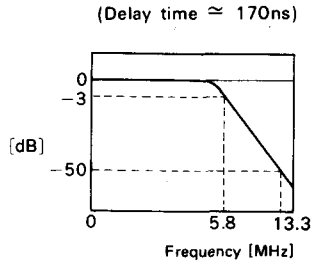


*2. Differential gain and differential phase measuring condition

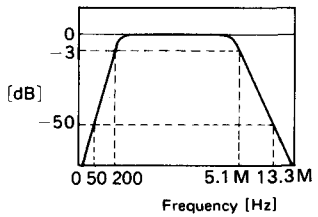


DG and DP are measured at output S point by vectorscope.

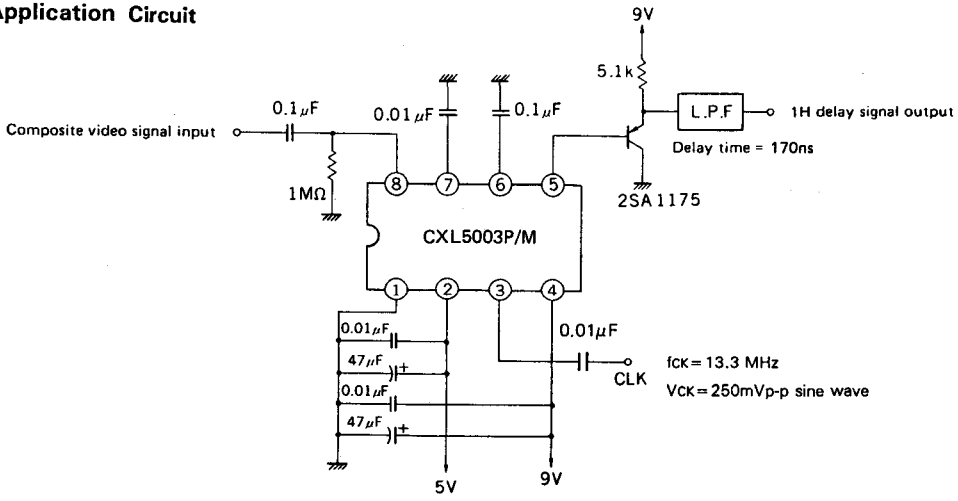
*3. LPF frequency characteristics



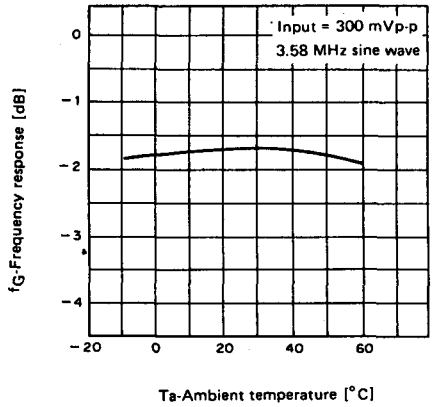
*4. BPF frequency characteristics



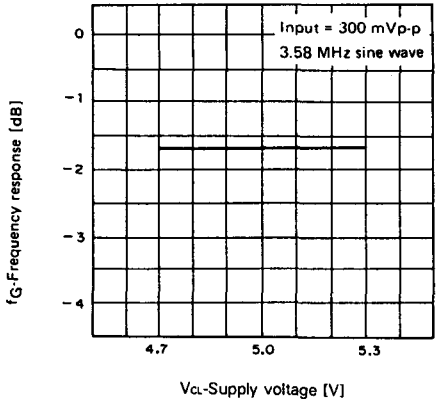
Application Circuit



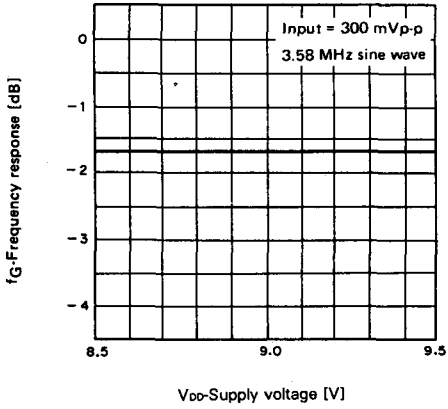
Frequency response vs. Ambient temperature



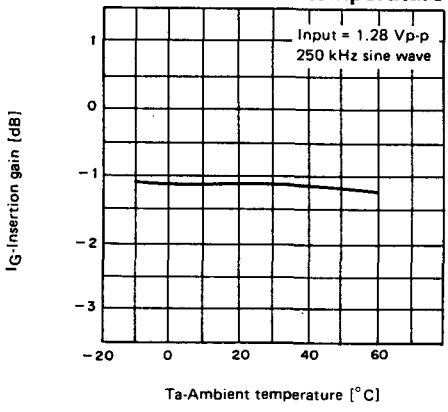
Frequency response vs. Supply voltage



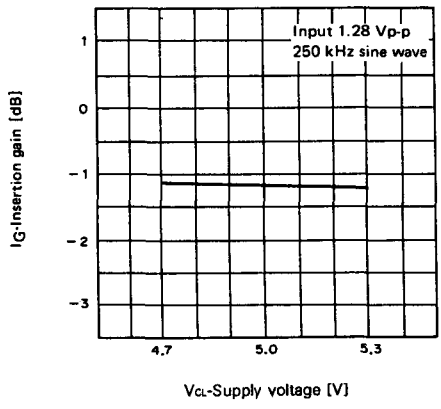
Frequency response vs. Supply voltage



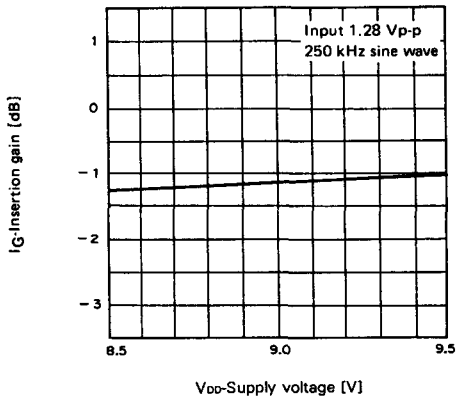
Insertion gain vs. Ambient temperature



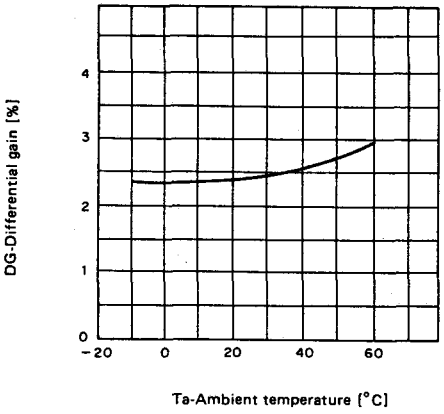
Insertion gain vs. Supply voltage



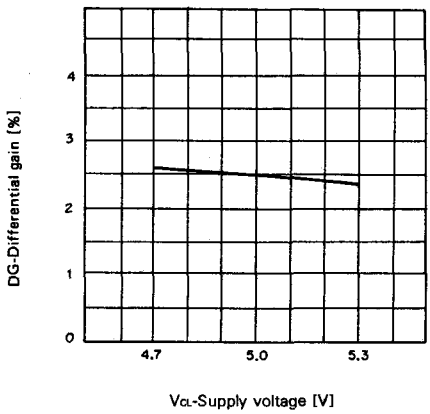
Insertion gain vs. Supply voltage



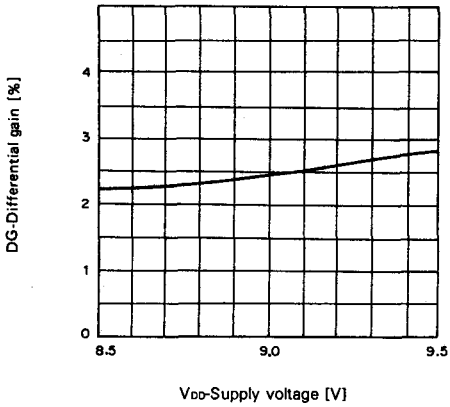
Differential gain vs. Ambient temperature



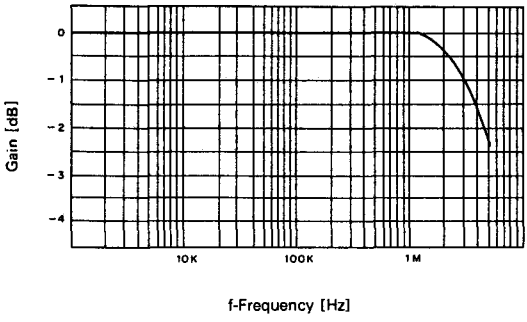
Differential gain vs. Supply voltage



Differential gain vs. Supply voltage



Frequency response



SONY CXL5005P/CXL5005M

CMOS-CCD 1H Delay Line for NTSC with PLL

Description

CXL5005P/CXL5005M are general purpose CCD delay line ICs which provide 1H delay time of NTSC.

The ICs are operative with a color sub-carrier frequency (3.58 MHz), as they contain a PLL.

Features

- Low power consumption 90 mW (Typ.)
- Small size package (14-pin DIP, SOP)
- Low differential gain DG=3% (Typ.)
- Input signal amplitude 180 IRE (=1.28 Vp-p, Max.)
- Low input clock amplitude operation 200 mVp-p (Min.)
- On chip peripheral circuits.
- 3xfsc output pin is provided.

Structure

CMOS-CCD

Functions

- 680 bit CCD resister
- Clock drivers
- Autobias circuit
- Synchronized tip clamp circuit
- Sample and hold circuit
- PLL (Phase Locked Loop)

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	11	V
• Supply voltage	V_{CL}	6	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation			
	P_D	CXL5005P 800	mW
		CXL5005M 400	mW

Recommended Operating Conditions

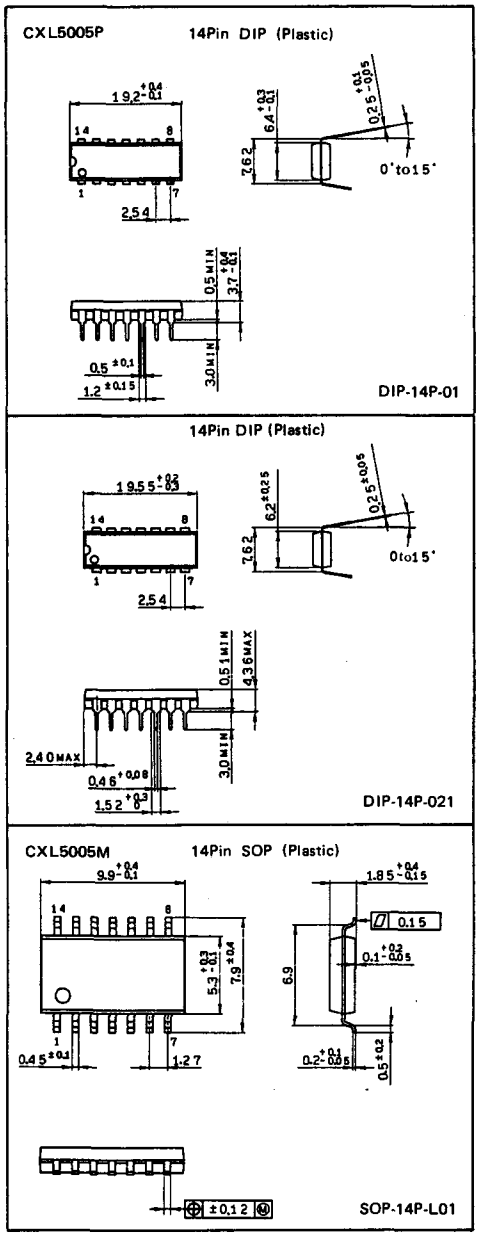
• Supply voltage	V_{DD}	9	V±5%
	V_{CL}	5	V±5%

Recommended Clock Conditions

• Input clock amplitude	V_{CLK}	200 mVp-p to 1.0 Vp-p (300mVp-p Typ.)	
• Clock frequency	f_{CLK}	3.579545	MHz

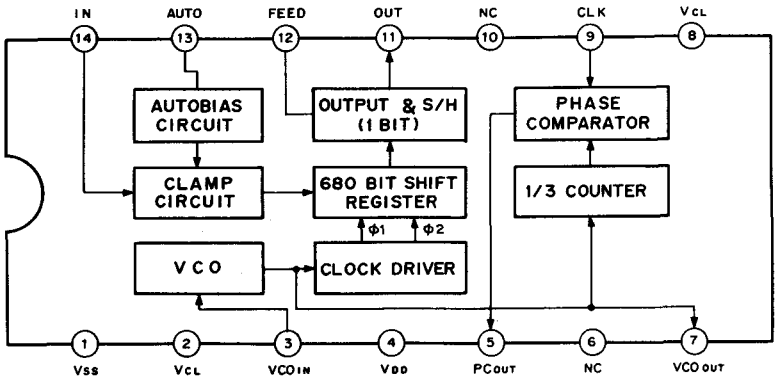
Package Outline

Unit: mm



E88Z40-ST

Block Diagram



Pin Description

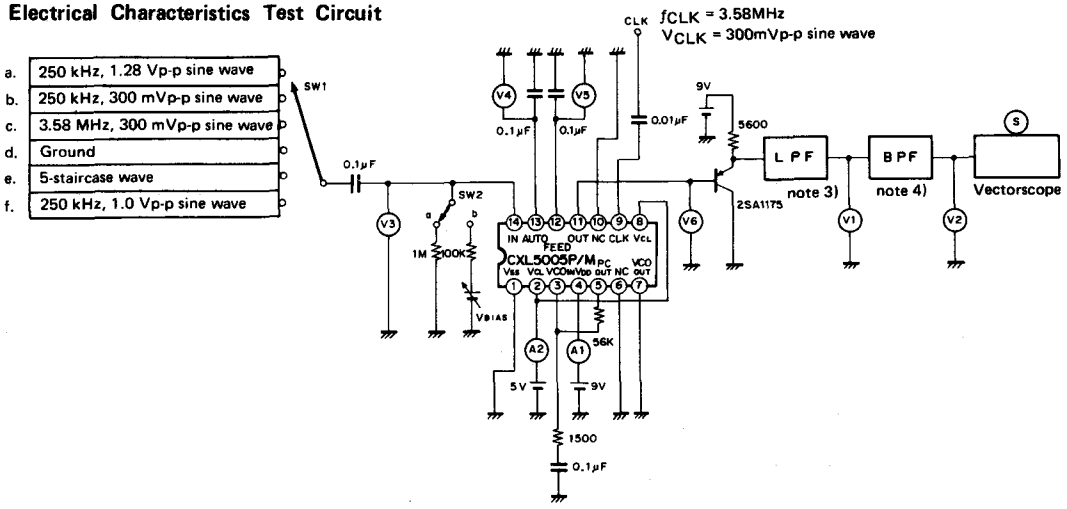
No.	Symbol	Description	Impedance [Ω]	No.	Symbol	Description	Impedance [Ω]
1	V_{SS}	GND		8	V_{CL}	5V power supply	
2	V_{CL}	5V power supply		9	CLK	Clock input	≈ 5k
3	VCO_{IN}	VCO input	>100k	10	NC		
4	V_{DD}	9V power supply		11	OUT	Signal output	600 to 1k
5	PC_{OUT}	Phase Comparator output	≈ 5k	12	FEED	Feedback DC output	>100k
6	NC			13	AUTO	Autobias DC output	10k
7	VCO_{OUT}	VCO output	≈ 5k	14	IN	Signal input	>100k

Electrical Characteristics

(Ta=25°C, V_{DD}=9.0V, V_{CL}=5.0V, f_{CK}=3.58 MHz. V_{CK}=300 mVp-p sine wave,
Test poit See"Electrcal characteristics test circuit")

Item	Symbol	Test condition	SW condition		Test point	Min.	Typ.	Max.	Unit
			SW1	SW2					
Supply current	I_{DD}	INPUT=250 kHz, 1.28 Vp-p.	a	a	A1	—	4	5	mA
	I_{CL}				A2	—	9	12	mA
Insertion gain	IG	INPUT=250 kHz, 1.28 Vp-p IG=20log (Output voltage [Vp-p]/ 1.28[Vp-p])	a	a	V1	−3	0	3	dB
Frequency response	fG	fG=20log ($V_{3.58\ MHz}$/ $V_{250\ kHz}$) (Note 1)	b,c	b	V1	−3.0	−2.1	—	dB
Differential gain	DG	5-staircase wave input Y=140IRE (=1.0 Vp-p) Measure S point with vectorscope (Note 2)	e	a	S	—	3	5	%
Differential phase	DP					—	3	5	deg
Allowable input amplitude	V_{IN-AC}		—	—	—	—	—	1.28	Vp-p
Noise	S/N	S: input=250 kHz 1.0 Vp-p output (Vp-p)	f	a	V2	55	60	—	dB
		N: input=DC output (Vrms)	d	a	V2				
Output DC voltage	V_{IN-AC}		d	a	V3	3.5	5.0	6.5	V
	$V_{AUTO-DC}$				V4	3.5	5.0	6.5	V
	$V_{FEED-DC}$	INPUT=250 kHz, 1.28 Vp-p.	a	a	V5	1.3	2.3	3.3	V
	V_{OUT-DC}				V6	1.7	2.7	3.7	V

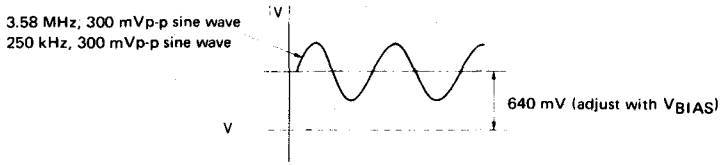
Electrical Characteristics Test Circuit



Note 1) Frequency characteristics measuring condition

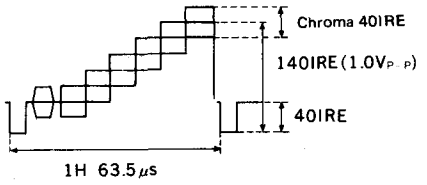
$V_{3.58\ MHz}$ (Output signal voltage [Vp-p] at 3.58 MHz input)
$V_{250\ kHz}$ (Output signal voltage [Vp-p] at 250 kHz input)

Set pin 14 (IN) voltage [V] = $V_{IN\text{-}DC}$ + 640 mV.



2) Differential gain and differential phase measuring condition

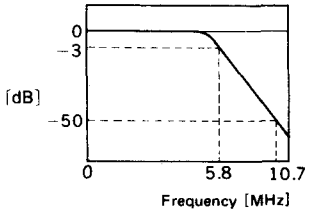
5-staircase wave signal



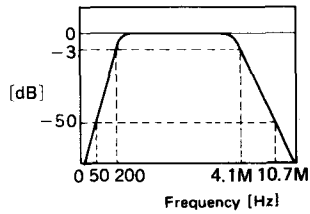
DG and DP are measured at output S point by vectorscope.

3) LPF frequency characteristics

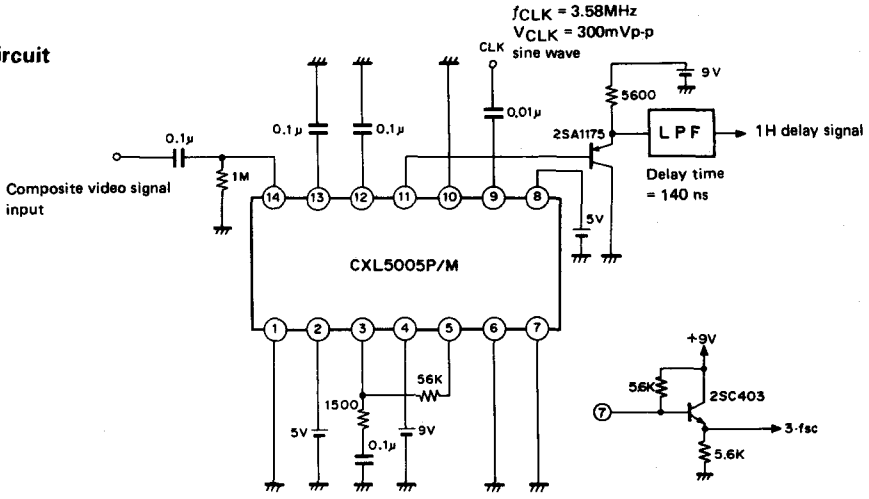
(Delay time ≃ 140ns)



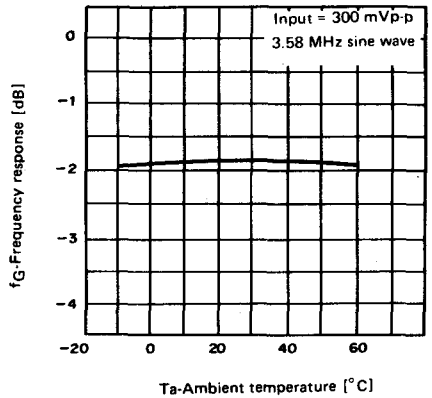
4) BPF frequency characteristics



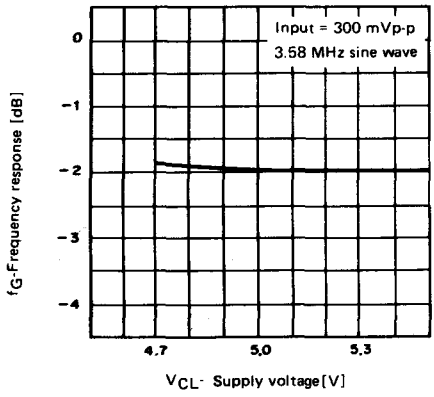
Application Circuit



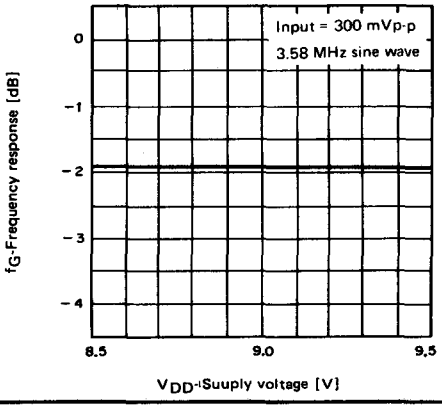
Frequency response vs. Ambient temperature



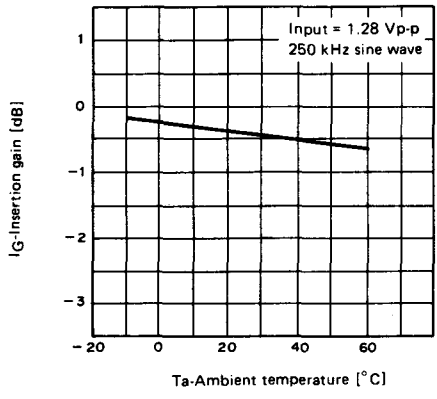
Frequency response vs. Supply voltage



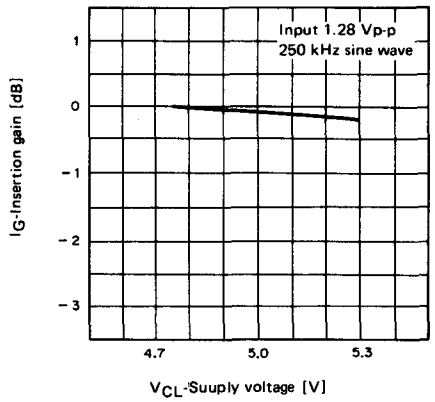
Frequency response vs. Supply voltage



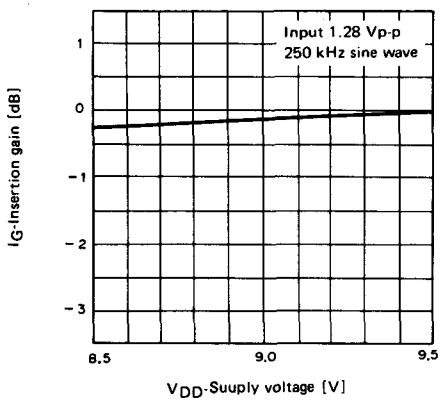
Insertion gain vs. Ambient temperature



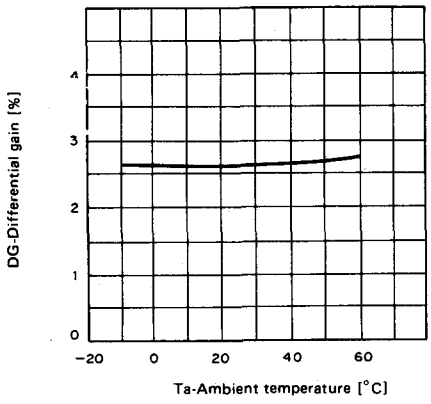
Insertion gain vs. Supply voltage



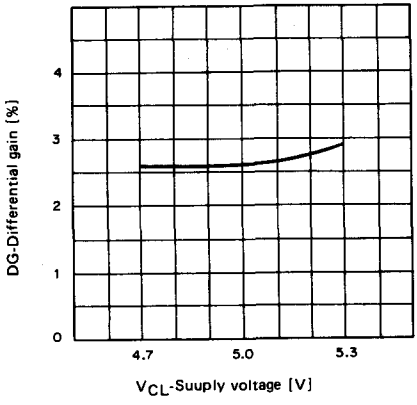
Insertion gain vs. Supply voltage



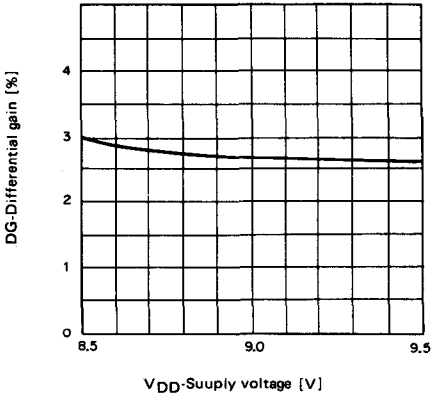
Differential gain vs. Ambient temperature



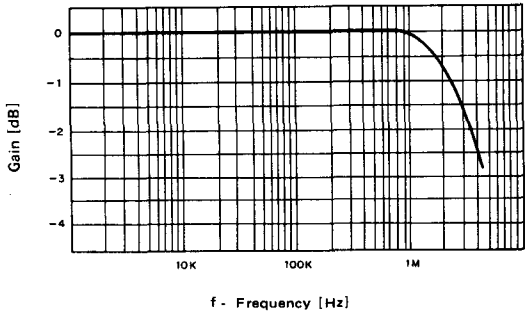
Differential gain vs. Supply voltage



Differential gain vs. Supply voltage



Frequency response



SONY

CXL5502M/P

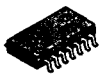
CMOS-CCD 1H Delay Line for NTSC

Description

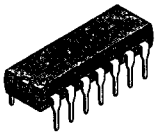
The CXL5502M/P are CMOS-CCD delay line ICs that provide 1H delay for NTSC signals including the external low pass filter.

The ICs contain a PLL circuit (quadruple progression).

CXL5502M
14 pin SOP (Plastic)



CXL5502P
14 pin DIP (Plastic)



Features

- Single power supply (5V)
- Low power consumption 95mW (Typ.)
- Built-in peripheral circuits
- Clamp level of input signal can be selected
- Built-in quadruple progression PLL circuit

Functions

- 905-bit CCD register
- Clock driver
- Autobias circuit
- Input clamp circuit
- Sample and hold circuit
- PLL circuit (quadruple progression)

Structure

CMOS-CCD

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	+6	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation			
	P_D		
	CXL5502M	400	mW
	CXL5502P	800	mW

Recommended Operating Condition (Ta = 25°C)

Supply voltage	V_{DD}	5 ± 5%	V

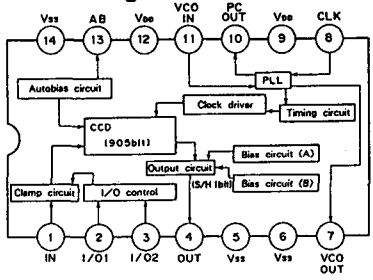
Recommended Clock Conditions (Ta = 25°C)

- Input clock amplitude V_{CLK} 0.3 to 1.0 Vp-p (0.5Vp-p Typ.)
- Clock frequency f_{CLK} 3.579545 MHz
- Input clock waveform Sine wave

Input Signal Amplitude

V_{SIG} 500mVp-p (Typ.), 572mVp-p (Max.)
(at Internal clamp condition)

Block Diagram and Pin Configuration (Top View)



E89930B12 – ST

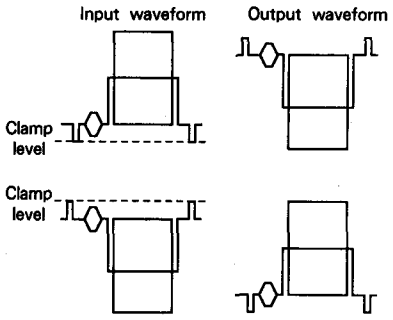
Pin Description

No.	Symbol	I/O	Description	Impedance
1	IN	I	Signal input	> 10kΩ at no clamp
2	I/O1	I	I/O control 1	
3	I/O2	I	I/O control 2	
4	OUT	O	Signal output	40 to 500 Ω
5	Vss	—	GND	
6	Vss	—	GND	
7	VCO OUT	O	VCO output	
8	CLK	I	Clock input	> 100kΩ
9	V_{DD}	—	Power supply (5V)	
10	PC OUT	O	Phase comparator output	
11	VCO IN	I	VCO input	
12	V_{DD}	—	Power supply (5V)	
13	AB	O	Autobias DC output	600 to 200kΩ
14	Vss	—	GND (SUB)	

Description of Function

In the CXL5502M/P, the condition of I/O control pins (Pins 2 and 3) control the input signal clamp condition and the mode of the output signal with relation to its input signal.

There are 2 modes for the I/O signal.



① PN mode
(Low level clamp/reverse phase output mode)

② NP mode
(High level clamp/positive phase output mode)

I/O Control Pin

① I/O1 (Pin 2)
Control of the I/O signal condition

DC open····Input signal is low level clamped and the output signal is inverted in relation to the input signal. As the pin is biased to 2.5V by means of the resistance inside the IC, a decoupling capacitor of around 1000pF is necessary.

GND·····Input signal is high level clamped and the output signal turns into an inverted signal.

② I/O2 (Pin 3)
Control of the input signal clamp condition

0V·····Internal clamp condition

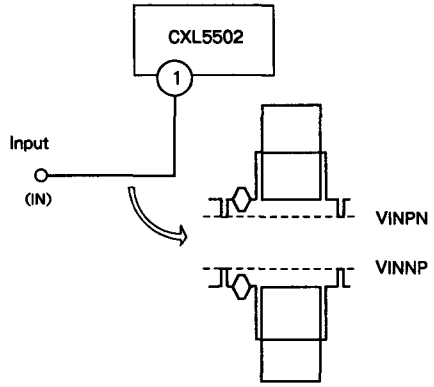
5V·····Non internal clamp condition
Center biased to approx. 2.1V by means of the IC internal resistance (several 10kΩ). Usage in this mode is limited to APL 50% signals and in this mode, the maximum input signal amplitude is 200mVp-p.

Electrical Characteristics (Ta = 25℃, V_{DD} = 5V, f_{CLK} = 3.579545MHz, V_{CLK} = 500mVp-p, Sine wave)
See "Electrical Characteristics Test Circuit"

Item	Symbol	Test condition	SW condition 1	2	3	4	5	6	7	Bias condition Vbias1 (V) (NOTE 1)	Min.	Typ.	Max.	Unit	NOTE
Supply current	IDDPN	—	—	c	b	b	b	a	—	—	10	19	28	mA	2
	IDDNP					a	a								
Low frequency gain	GLPN	200kHz 500mVp-p Sine wave	a	a	b	b	b	a	b	—	−2	0	2	dB	3
	GLNP					a	a								
Frequency response	fPN	200kHz↔3.57MHz 150mVp-p Sine wave	b ↕ c	a	a	b	b	b	b	2.1	−2	−1	0	dB	4
	fNP					a	a								
Differential gain	DGPN	5-staircase wave (See Note 5)	d	a	b	b	b	a	c	—	0	5	7	%	5
	DGNP			b		a	a								
Differential phase	DPPN	5-staircase wave (See Note 5)	d	a	b	b	b	a	c	—	0	5	7	degree	5
	DPNP			b		a	a								
S/H pulse coupling	CPPN	No signal input	—	c	a	b	b	b	a	VINPN + 0.5	—	—	350	mVp-p	6
	CPNP					a	a			VINNP					
SN ratio	SNPN	50% white video signal (See Note 7)	e	a	b	b	b	a	d	—	52	56	—	dB	7
	SNNP			b		a	a								

NOTE

① VINPN and VINNP are defined as follows.
VINPN and VINNP are the input signal clamp levels of PN and NP modes clamping the video signal sync chip level.



Testing of VINPN and VINNP is executed with a voltmeter under the following SW conditions.

Item	SW condition 1	2	3	4	5	6	7	Test point
VINPN	—	c	b	b	b	a	—	V1
VINNP	—	c	b	a	a	a	—	

② This is the IC supply current value during clock and signal input.

③ GLPN, GLNP are output gain of pin OUT when a 500mVp-p, 200kHz sine wave is fed to pin IN.

(Example of calculation)

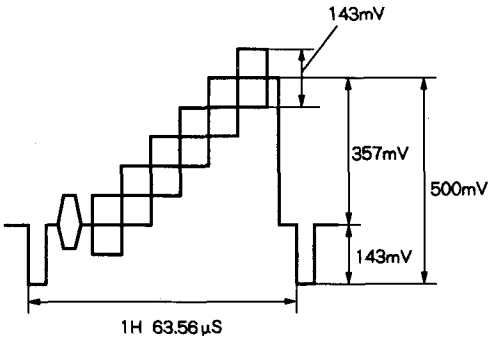
$$GLPN = 20\log \frac{\text{pin OUT output voltage (PN mode) [mVp-p]}}{500\ [\text{mVp-p}]}\ [\text{dB}]$$

④ Indicates the dissipation at 3.57MHz in relation to 200kHz.
From the output voltage at pin OUT when a 150mVp-p, 200kHz sine wave is fed to pin IN, and from the output voltage at pin OUT when a 150mVp-p, 3.57MHz sine wave is fed to same, calculation is made according to the following formula. Input bias is tested at 2.1V.

(Example of calculation)

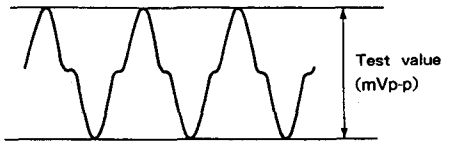
$$fPN = 20\log \frac{\text{pin OUT output voltage (PN mode, 3.57MHz) [mVp-p]}}{\text{pin OUT output voltage (PN mode, 200kHz) [mVp-p]}}\ [\text{dB}]$$

⑤ In Fig. below, differential gain (DG) and differential phase (DP) are tested with a vectorscope when the 5-staircase staircase wave is fed.

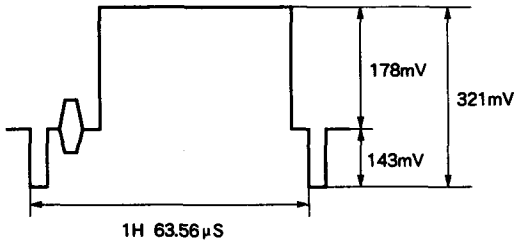


Input waveform (Input waveform of NP mode is the inverted waveform in the figure above)

⑥ Leakage of internal clock components and related high frequency components to the output signal, during no signal input. Input bias is tested at VINPN + 0.5V and VINNP for PN and NP modes respectively.



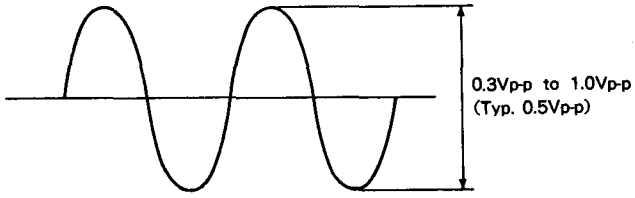
⑦ SN ratio during a 50% white video signal input shown in Fig. below is tested at a video noise meter, in BPF 100kHz to 4MHz, Sub Carrier Trap mode.



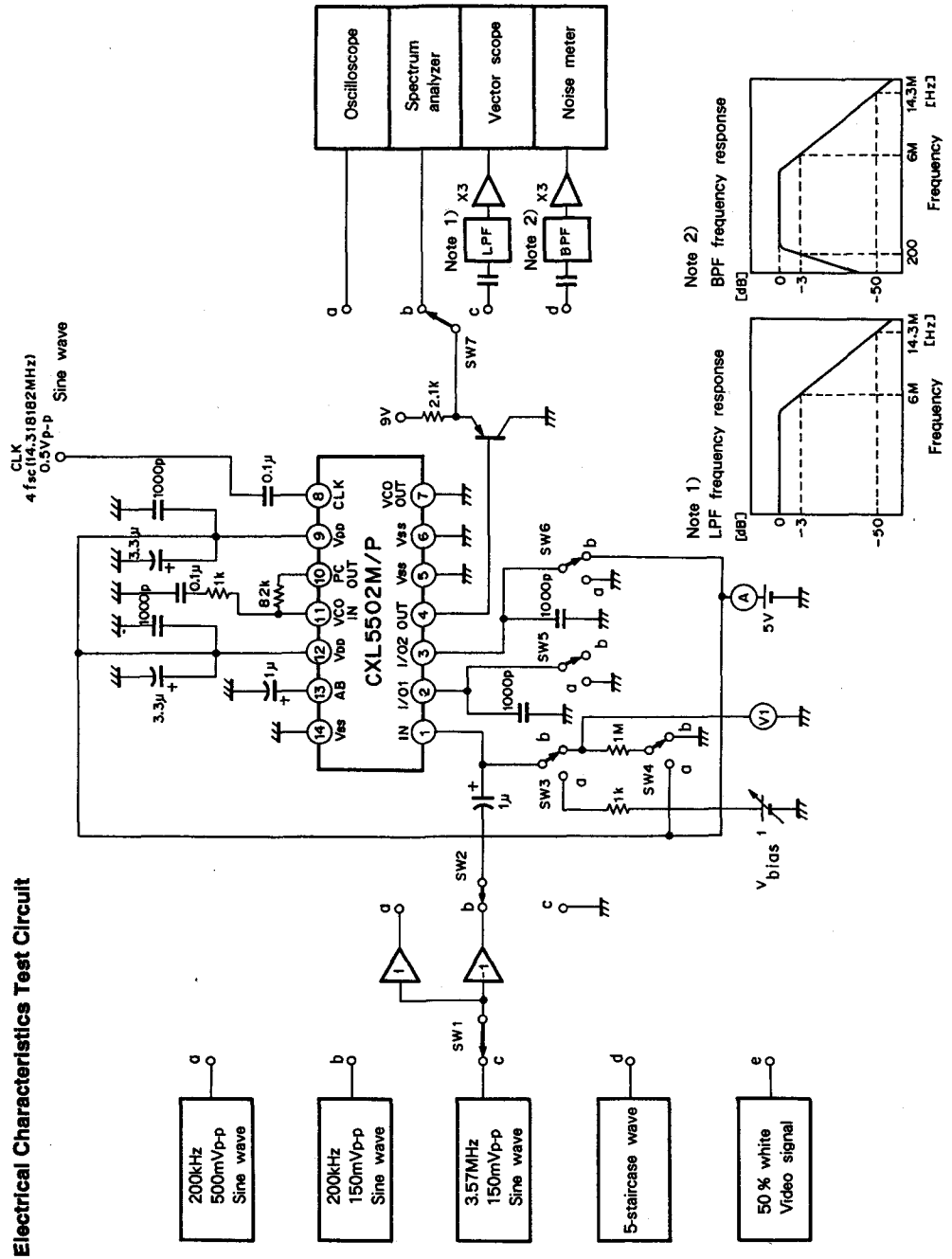
Input waveform (Input waveform of NP mode is the inverted waveform in the figure above)

CLOCK

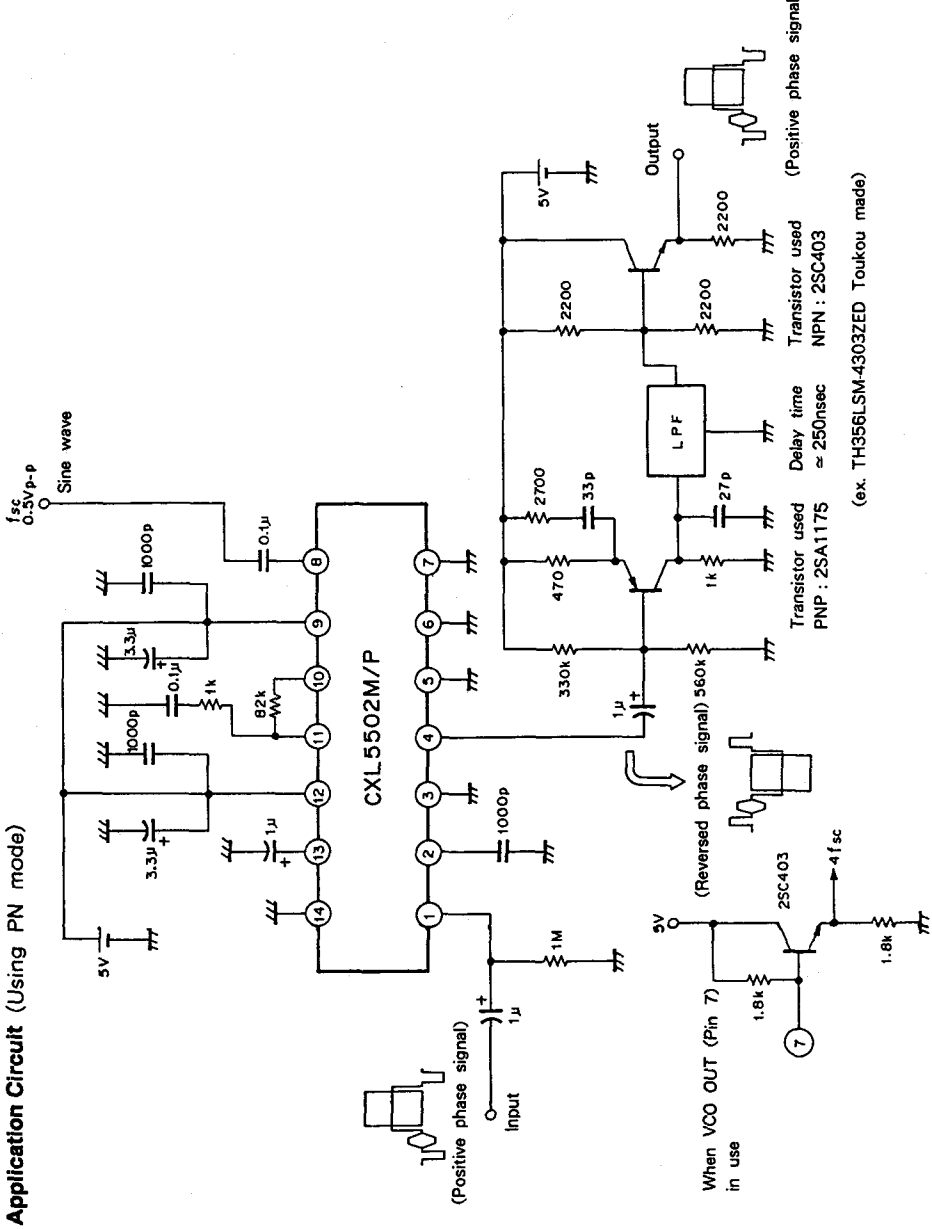
fsc (3.579545MHz) Sine wave



Electrical Characteristics Test Circuit



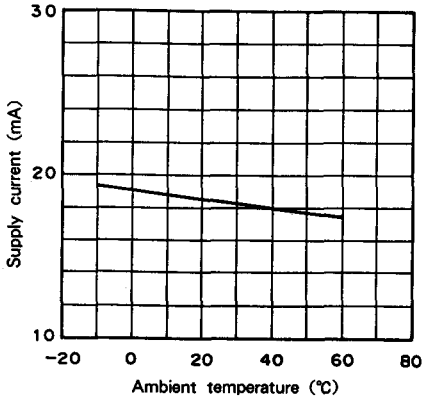
Application Circuit (Using PN mode)



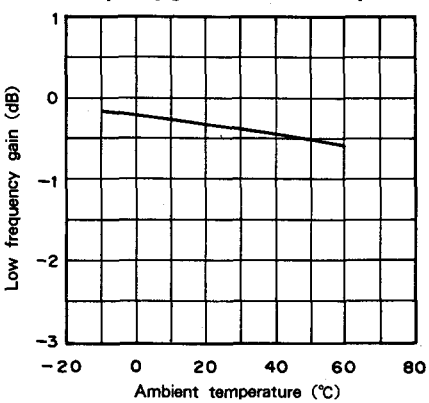
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

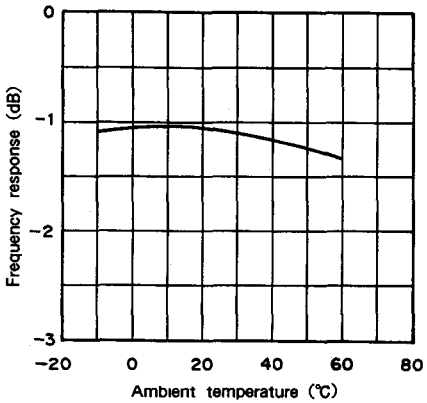
Supply current vs. Ambient temperature



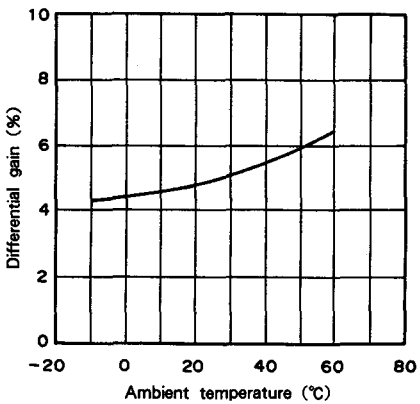
Low frequency gain vs. Ambient temperature



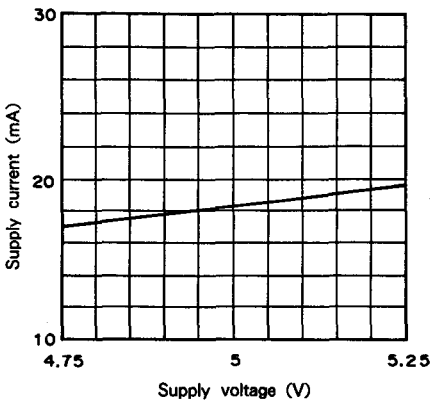
Frequency response vs. Ambient temperature



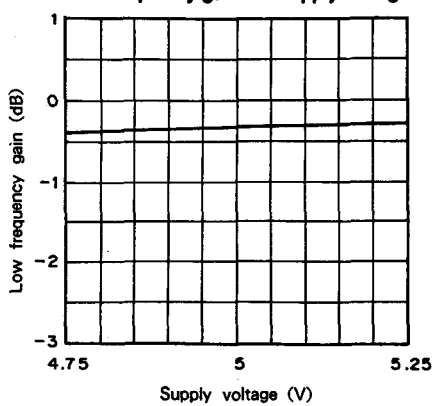
Differential gain vs. Ambient temperature



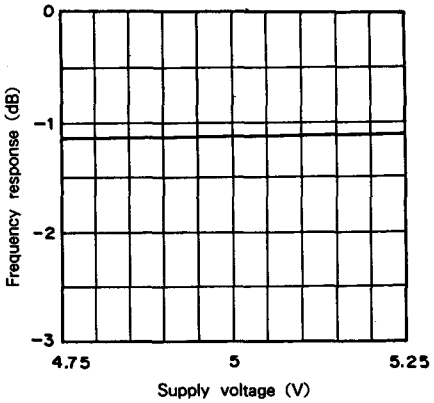
Supply current vs. Supply voltage



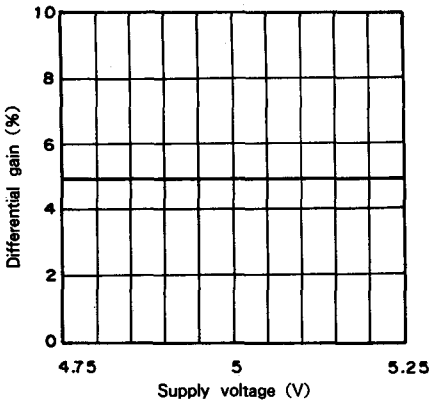
Low frequency gain vs. Supply voltage



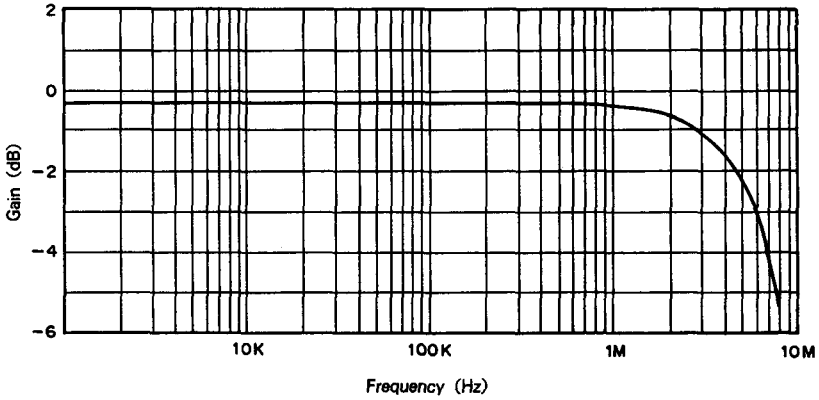
Frequency response vs. Supply voltage



Differential gain vs. Supply voltage

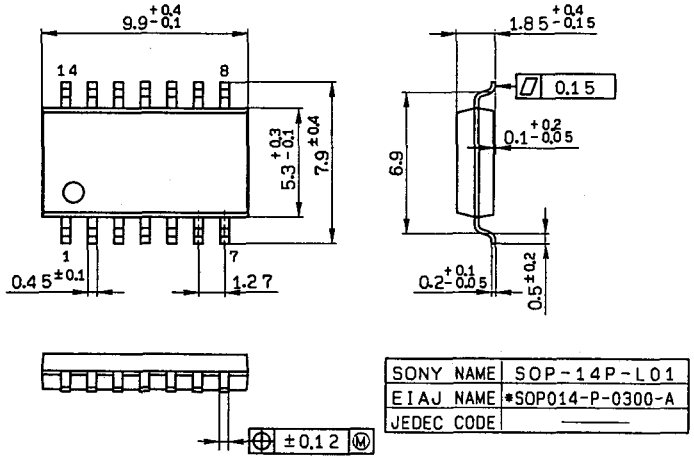


Frequency response

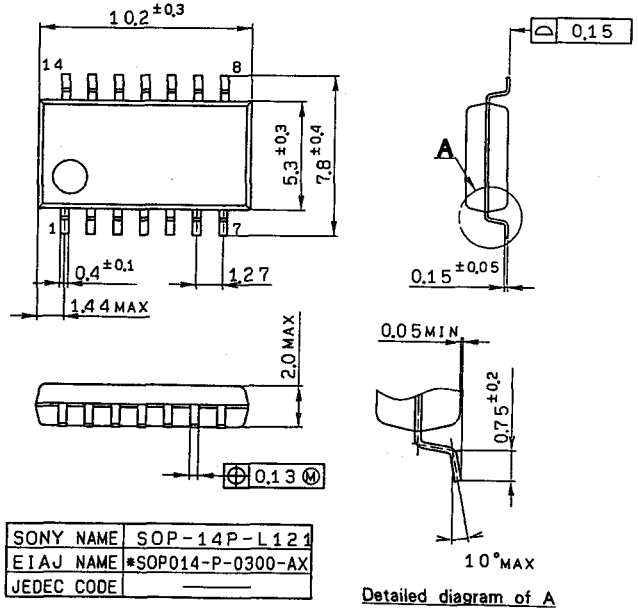


Package Outline Unit : mm

CXL5502M 14pin SOP (Plastic) 300mil 0.2g

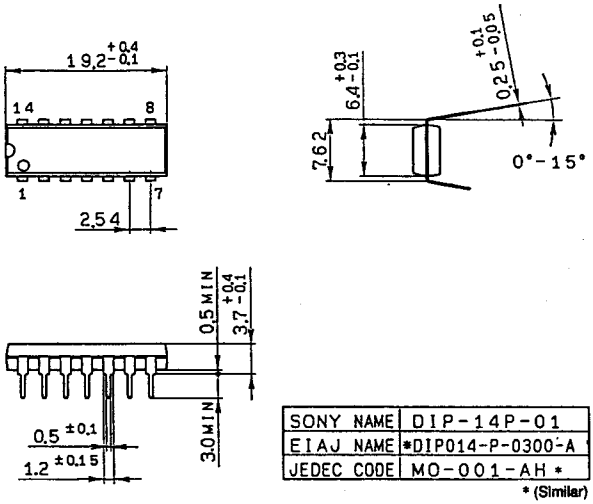


14pin SOP (Plastic) 300mil



CXL5502P

14pin DIP (Plastic) 300mil 0.9g



SONY NAME	DIP-14P-01
EIAJ NAME	*DIP014-P-0300-A
JEDEC CODE	MO-001-AH *

* (Similar)

SONY

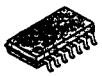
CXL5505M/P

CMOS-CCD 1H Delay Line for PAL

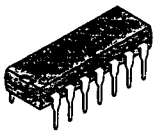
Description

The CXL5505M/P are CMOS-CCD delay line ICs that provide 1H delay for PAL signals including the external low pass filter.

CXL5505M
14 pin SOP (Plastic)



CXL5505P
14 pin DIP (Plastic)



Features

- Single 5V power supply
- Low power consumption 100mW (Typ.)
- Built-in peripheral circuits
- Built-in quadruple progression PLL circuit

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	+6	V
• Operating temperature	Topr	−10 to + 60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation			
	P_D		
	CXL5505M	400	mW
	CXL5505P	800	mW

Functions

- 1130-bit CCD register
- Clock driver
- Auto-bias circuit
- Input clamp circuit
- Sample and hold circuit
- PLL circuit

Structure

CMOS-CCD

Recommended Operating Condition (Ta=25°C)

Supply voltage V_{DD} 5V ± 5%

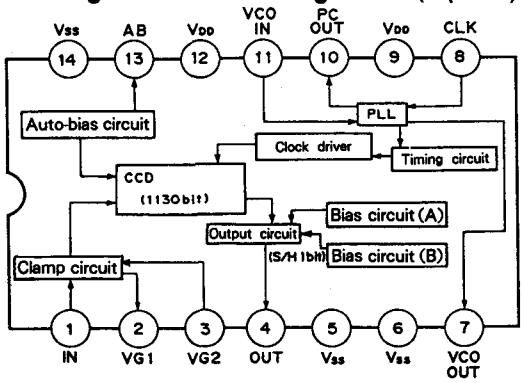
Recommended Clock Conditions (Ta=25°C)

• Input clock amplitude	V_{CLK}	0.3 to 1.0	Vp-p (0.5Vp-p Typ.)
• Clock frequency	f_{CLK}	4.433619	MHz
• Input clock waveform	Sine wave		

Input Signal Amplitude

V_{SIG} 575mVp-p (Max.) (at internal clamp condition)

Block Diagram and Pin Configuration (Top View)

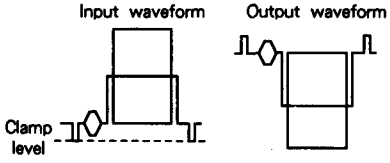


E90731A0Z – ST

Pin Description

Pin No.	Symbol	I/O	Description	Impedance
1	IN	I	Signal input	>10kΩ at no clamp
2	VG1	O	Gate bias 1 DC output	
*3	VG2	I	Gate bias 2 DC input	
4	OUT	O	Signal output	40 to 500 Ω
5	Vss	—	GND	
6	Vss	—	GND	
7	VCO OUT	O	VCO output	
8	CLK	I	Clock input	>10kΩ
9	V_{DD}	—	Power supply (5V)	
10	PC OUT	O	Phase comparator output	
11	VCO IN	I	VCO input	
12	V_{DD}	—	Power supply (5V)	
13	AB	O	Auto-bias DC output	600 to 200kΩ
14	Vss	—	GND (SUB)	

* Pin 3 (VG2)
Control of the input signal clamp condition
0V·····Sync tip clamp condition
5V·····Center bias condition
Center biased to approx. 2.1V by means of the IC internal resistance (approx. 10kΩ).
Usage in this mode is limited to APL 50% signals and in this mode, the maximum input signal amplitude is 200mVp-p.



Electrical Characteristics

(Ta=25℃, V_{DD}=5V, f_{CLK}=4.433619MHz, V_{CLK}=500mVp-p, Sine wave)
See "Electrical Characteristics Test Circuit",

Item	Symbol	Test condition	SW condition			Min.	Typ.	Max.	Unit	Note
			1	2	3					
Supply current	IDD	—	a	a	—	11	20	29	mA	1
Low frequency gain	GL	200kHz 500mVp-p Sine wave	a	a	b	–2	0	2	dB	2
Frequency response characteristics	fR	200kHz↔4.43MHz 150mVp-p Sine wave	b ↕ c	b	b	–2	–1	0	dB	3
Differential gain	DG	5-staircase wave (See Note 4)	d	a	c	0	3	5	%	4
Differential phase	DP	5-staircase wave (See Note 4)	d	a	c	0	3	5	degree	4
S/H pulse coupling	CP	No signal input	f	b	a	—	—	350	mVp-p	5
S/N ratio	SN	50% white video signal (See Note 6)	e	a	d	52	56	—	dB	6

Note

① This is the IC supply current value during clock and signal input.

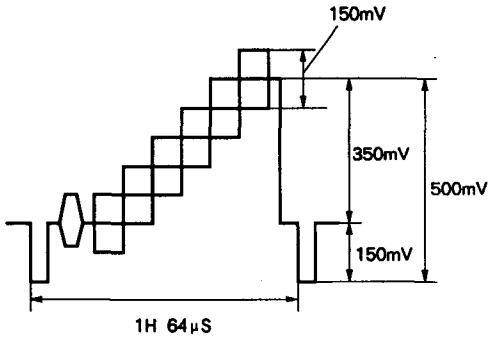
② GL is output gain of pin OUT when a 500mVp-p, 200kHz sine wave is fed to pin IN.

$$GL=20\log \frac{\text{pin OUT output voltage [mVp-p]}}{500\text{[mVp-p]}} \text{ [dB]}$$

③ Indicates the dissipation at 4.43MHz in relation to 200kHz.
From the output voltage at pin OUT when a 150mVp-p, 200kHz sine wave is fed to pin IN, and from the output voltage at pin OUT when a 150mVp-p, 4.43MHz sine wave is fed to same, calculation is made according to the following formula.

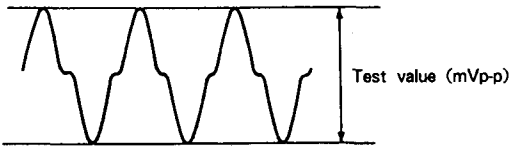
$$fR=20\log \frac{\text{pin OUT output voltage (4.43MHz) [mVp-p]}}{\text{pin OUT output voltage (200kHz)[mVp-p]}} \text{ [dB]}$$

④ In Fig. below, differential gain (DG) and differential phase (DP) are tested with a vector scope when the 5-staircase wave is fed.

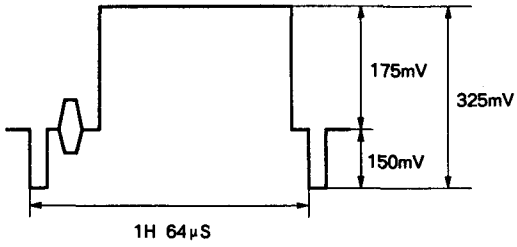


Input waveform

⑤ Leakage of internal clock components and related high frequency components to the output signal, during no signal input, is tested.



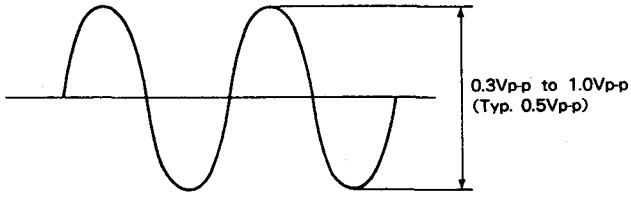
⑥ S/N ratio during a 50% white video signal input shown in Fig. below is tested at a video noise meter, in BPF 100kHz to 5MHz, Sub Carrier Trap mode.



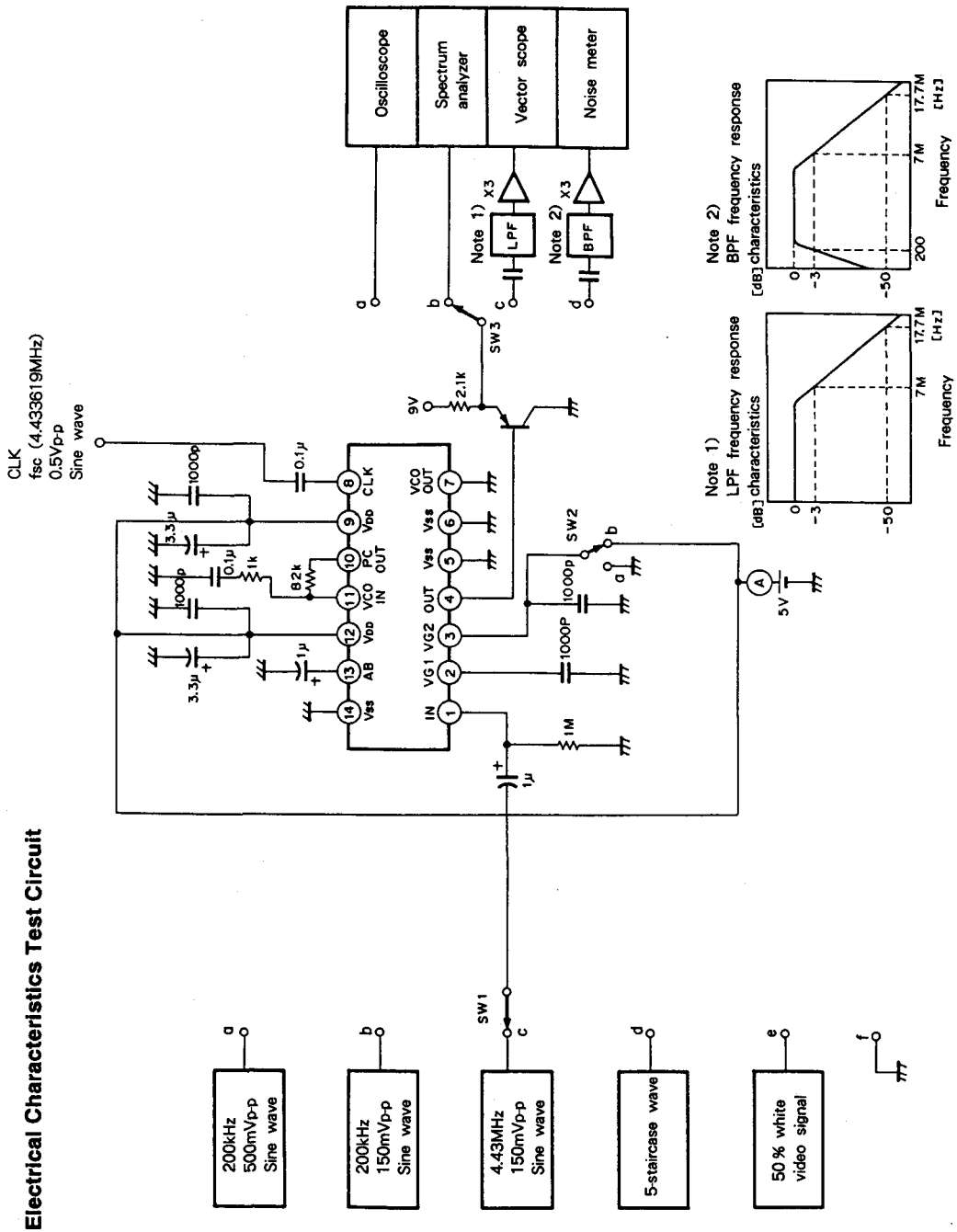
Input waveform

Clock

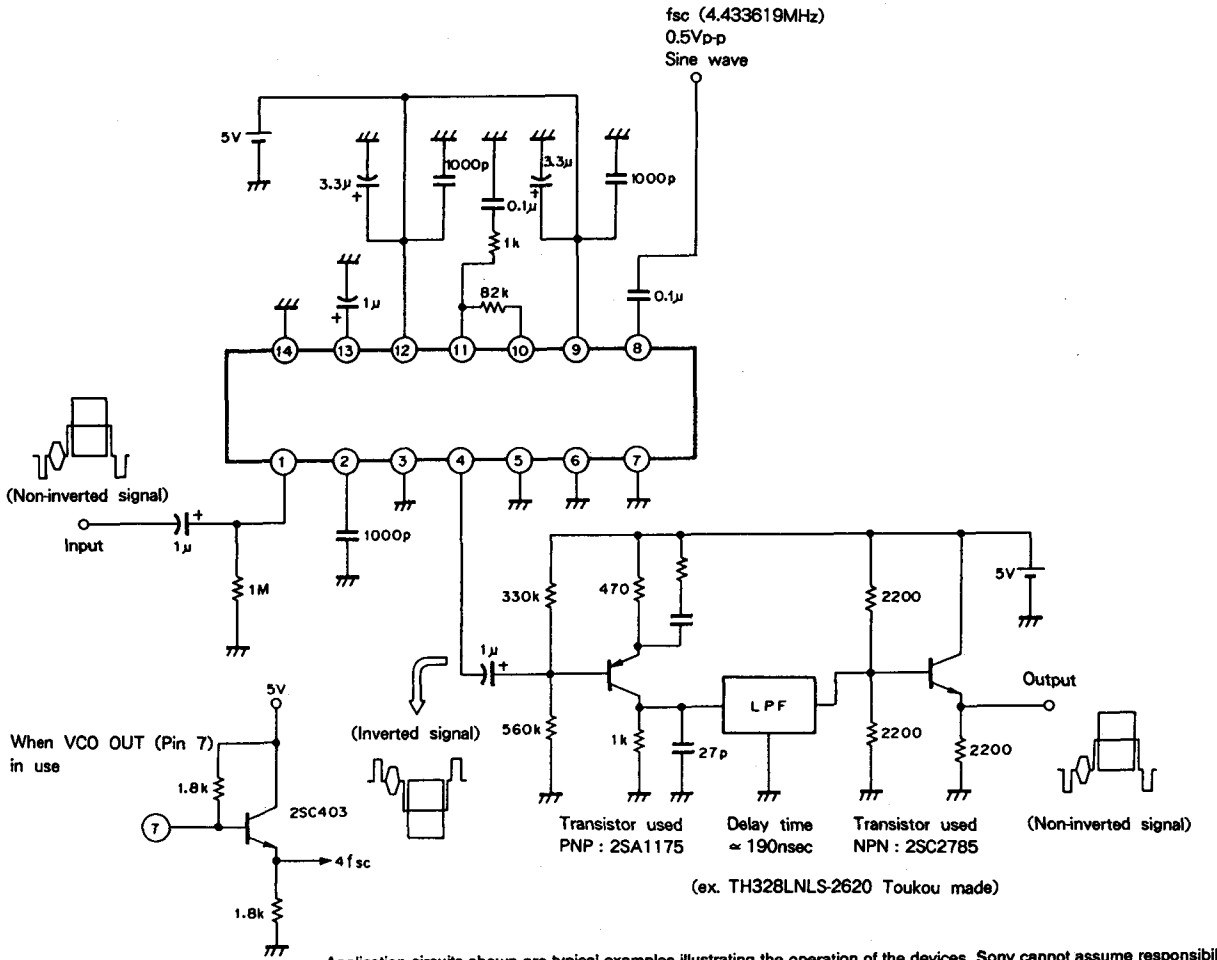
4fsc (4.433619MHz) Sine wave



Electrical Characteristics Test Circuit



Application Circuit



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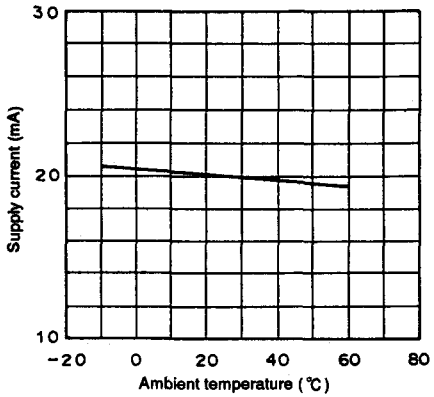
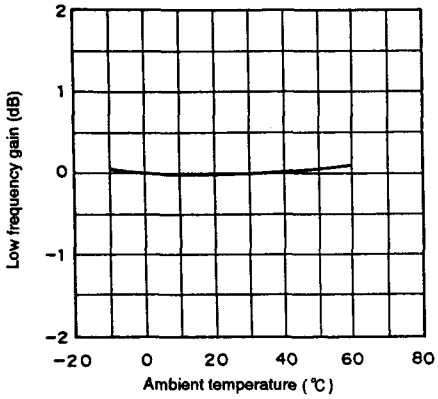
Example of Representative Characteristics

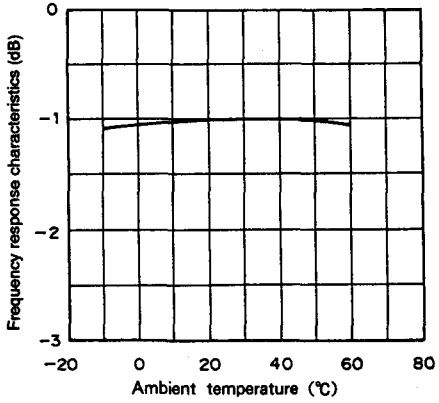
Supply current vs. Ambient temperature



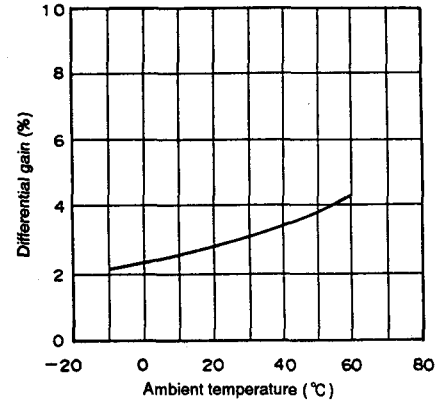
Low frequency gain vs. Ambient temperature



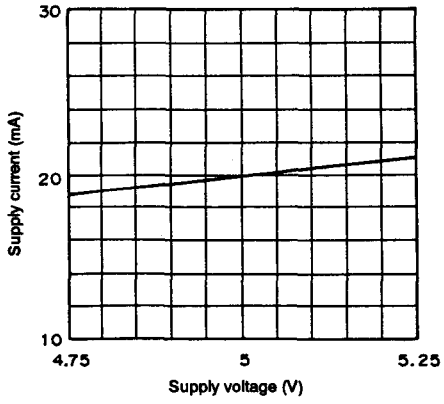
Frequency response characteristics vs. Ambient temperature



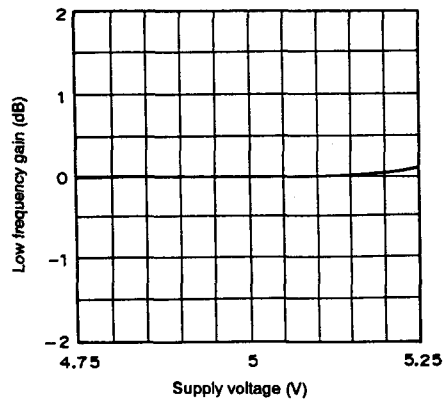
Differential gain vs. Ambient temperature



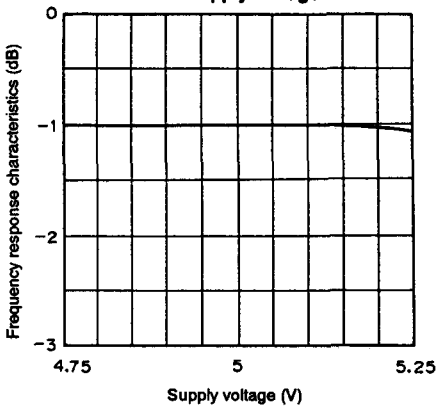
Supply current vs. Supply voltage



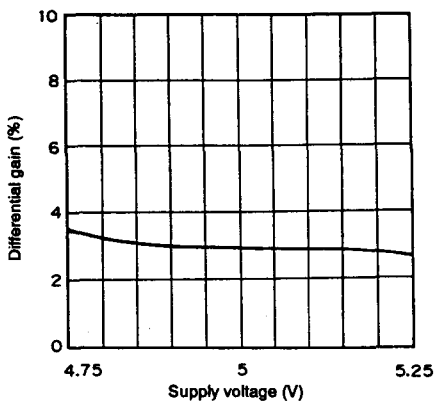
Low frequency gain vs. Supply voltage



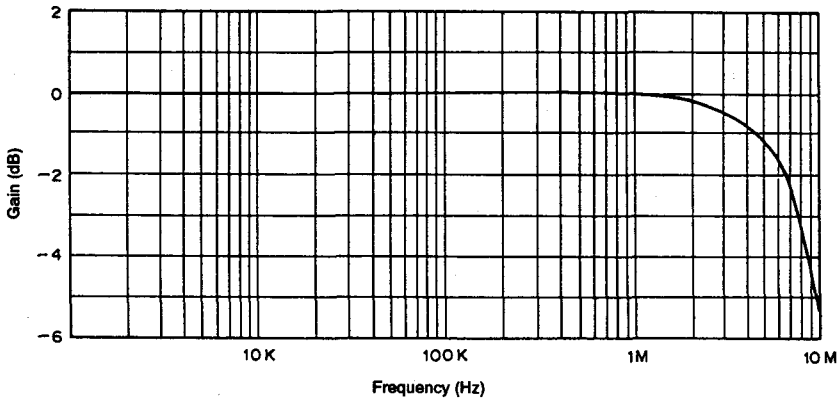
Frequency response characteristics vs. Supply voltage



Differential gain vs. Supply voltage

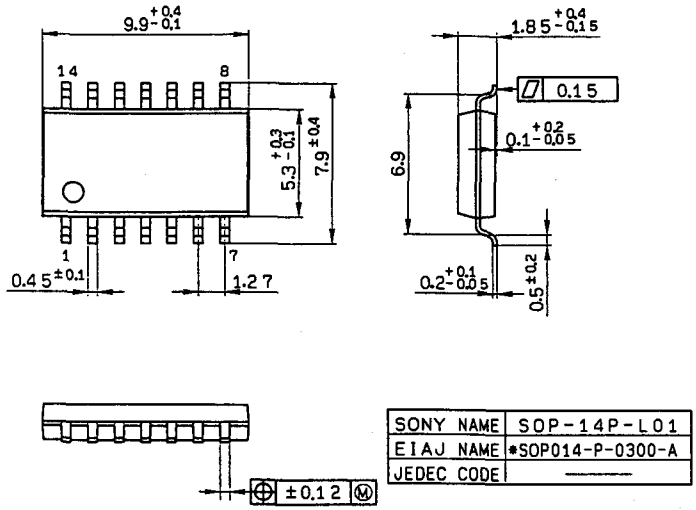


Frequency response characteristics



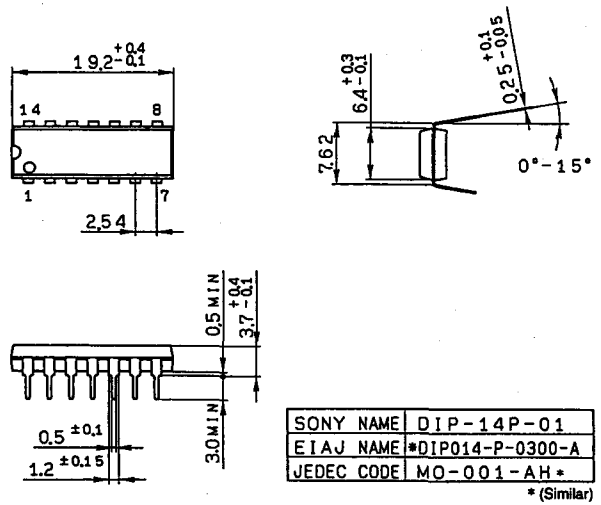
Package Outline Unit : mm

CXL5505M 14 pin SOP (Plastic) 300mil 0.1g



SONY NAME	SOP-14P-L01
EIAJ NAME	*SOP014-P-0300-A
JEDEC CODE	———

CXL5505P 14 pin DIP (Plastic) 300mil 0.5g



SONY NAME	DIP-14P-01
EIAJ NAME	*DIP014-P-0300-A
JEDEC CODE	MO-001-AH*

* (Similar)

SONY

CXL5506M/P

CMOS-CCD 1H Delay Line for PAL

Description

The CXL5506M/P are CMOS-CCD delay line ICs that provide 1H delay for PAL signals including the external low pass filter.

CXL5506M
8 pin SOP (Plastic)

CXL5506P
8 pin DIP (Plastic)

Features

- Single 5V power supply
- Low power consumption 95mW (Typ.)
- Built-in peripheral circuits

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	+6	V
• Operating temperature	Topr	−10 to + 60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D		
	CXL5506M	350	mW
	CXL5506P	480	mW

Functions

- 1130-bit CCD register
- Clock driver
- Auto-bias circuit
- Input clamp circuit
- Sample and hold circuit

Structure

CMOS-CCD

Recommended Operating Condition (Ta=25°C)

Supply voltage	V_{DD}	5V ± 5%

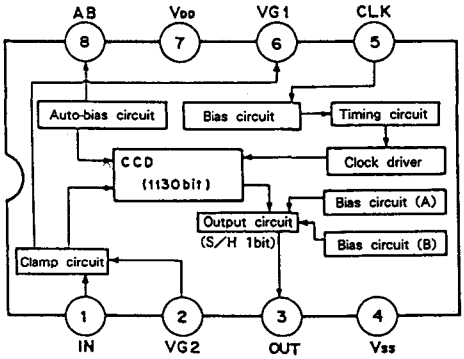
Recommended Clock Conditions (Ta=25°C)

• Input clock amplitude	V_{CLK}	0.3 to 1.0	Vp-p (0.5Vp-p Typ.)
• Clock frequency	f_{CLK}	17.734475	MHz
• Input clock waveform	Sine wave		

Input Signal Amplitude

V_{SIG} 575mVp-p (Max.) (at internal clamp condition)

Block Diagram and Pin Configuration (Top View)



E90632A0Z – ST

Pin Description

Pin No.	Symbol	I/O	Description	Impedance
1	IN	I	Signal input	>10kΩ at no clamp
*2	VG2	I	Gate bias 2 DC input	
3	OUT	O	Signal output	40 to 500 Ω
4	Vss	—	GND	
5	CLK	I	Clock input	>10kΩ
6	VG1	O	Gate bias 1 DC output	
7	V_{DD}	—	Power supply (5V)	
8	AB	O	Auto-bias DC output	600 to 200kΩ

* Pin 2 (VG2)

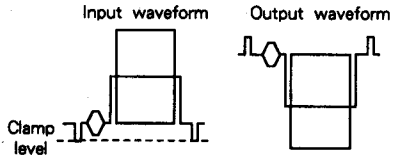
Control of the input signal clamp condition

0V·····Sync tip clamp condition

5V·····Center bias condition

Center biased to approx. 2.1V by means of the IC internal resistance (approx. 10kΩ).

Usage in this mode is limited to APL 50% signals and in this mode, the maximum input signal amplitude is 200mVp-p.



Electrical Characteristics

(Ta=25°C, V_{DD}=5V, f_{CLK}=17.734475MHz, V_{CLK}=500mVp-p, Sine wave)
See "Electrical Characteristics Test Circuit",

Item	Symbol	Test condition	SW condition			Min.	Typ.	Max.	Unit	Note
			1	2	3					
Supply current	IDD	—	a	a	—	10	19	28	mA	1
Low frequency gain	GL	200kHz 500mVp-p Sine wave	a	a	b	–2	0	2	dB	2
Frequency response characteristics	fR	200kHz ↔ 4.43MHz 150mVp-p Sine wave	b ↕ c	b	b	–2	–1	0	dB	3
Differential gain	DG	5-staircase wave (See Note 4)	d	a	c	0	3	5	%	4
Differential phase	DP	5-staircase wave (See Note 4)	d	a	c	0	3	5	degree	4
S/H pulse coupling	CP	No signal input	f	b	a	—	—	350	mVp-p	5
S/N ratio	SN	50% white video signal (See Note 6)	e	a	d	52	56	———	dB	6

Note

① This is the IC supply current value during clock and signal input.

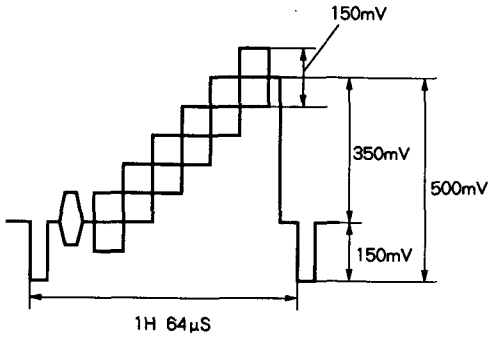
② GL is output gain of pin OUT when a 500mVp-p, 200kHz sine wave is fed to pin IN.

$$GL=20\log \frac{\text{pin OUT output voltage [mVp-p]}}{\text{500[mVp-p]}} \text{ [dB]}$$

③ Indicates the dissipation at 4.43MHz in relation to 200kHz.
From the output voltage at pin OUT when a 150mVp-p, 200kHz sine wave is fed to pin IN, and from the output voltage at pin OUT when a 150mVp-p, 4.43MHz sine wave is fed to same, calculation is made according to the following formula.

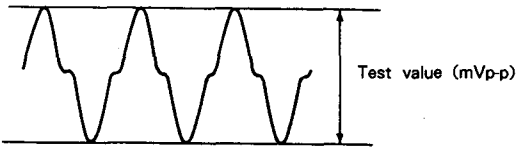
$$fR=20\log \frac{\text{pin OUT output voltage (4.43MHz) [mVp-p]}}{\text{pin OUT output voltage (200kHz)[mVp-p]}} \text{ [dB]}$$

④ In Fig. below, differential gain (DG) and differential phase (DP) are tested with a vector scope when the 5-staircase wave is fed.

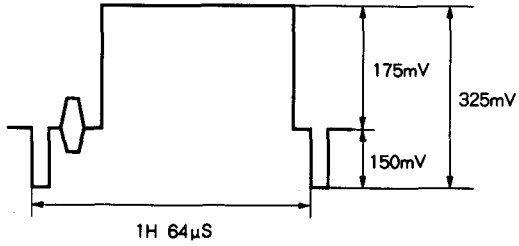


Input waveform

⑤ Leakage of internal clock components and related high frequency components to the output signal, during no signal input, is tested.



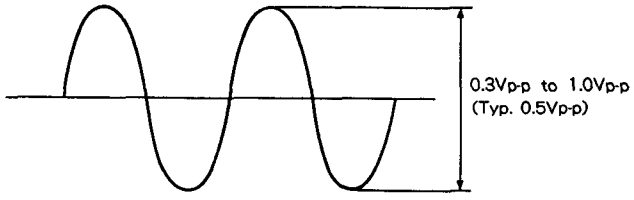
⑥ S/N ratio during a 50% white video signal input shown in Fig. below is tested at a video noise meter, in BPF 100kHz to 5MHz, Sub Carrier Trap mode.



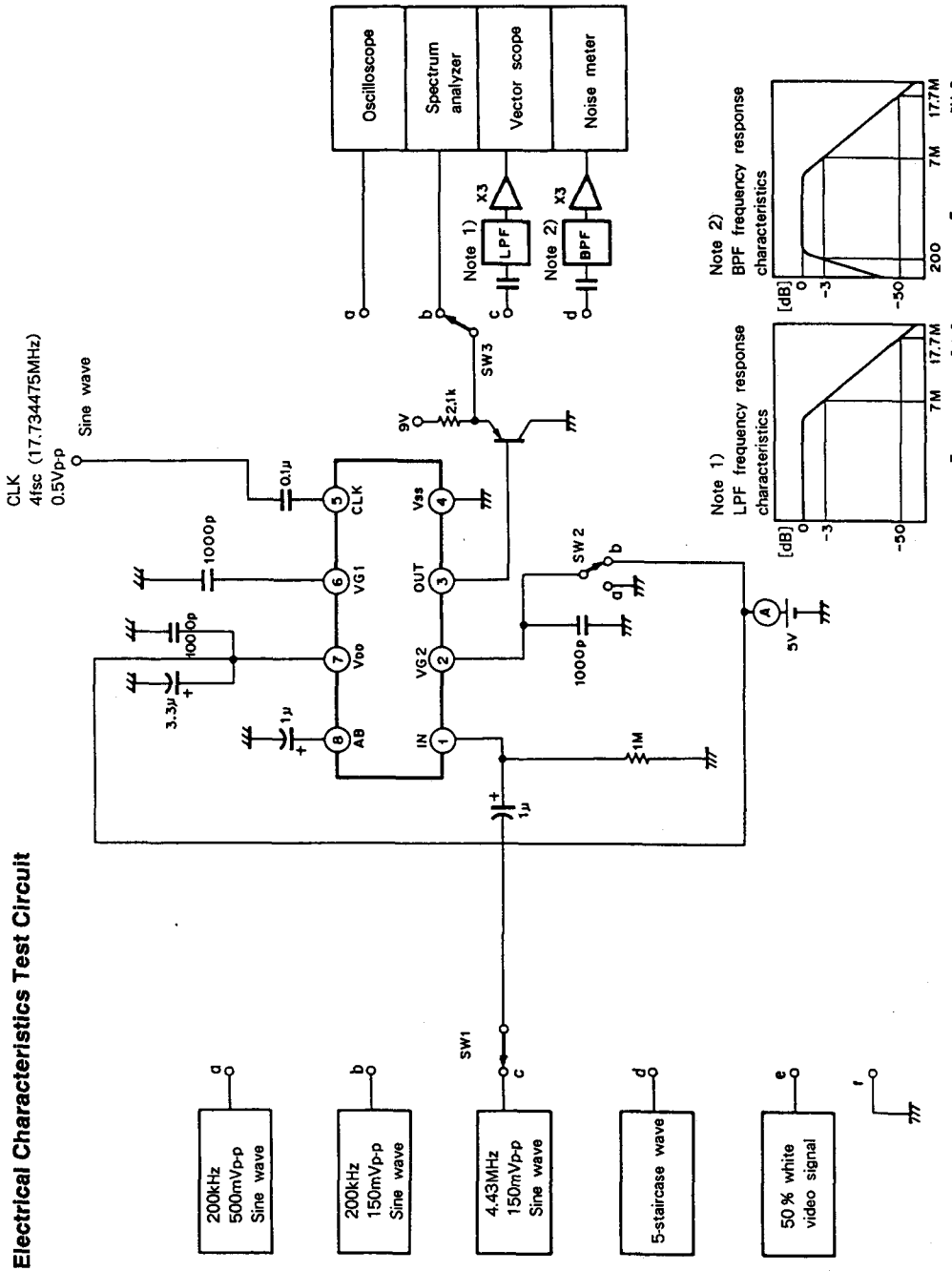
Input waveform

Clock

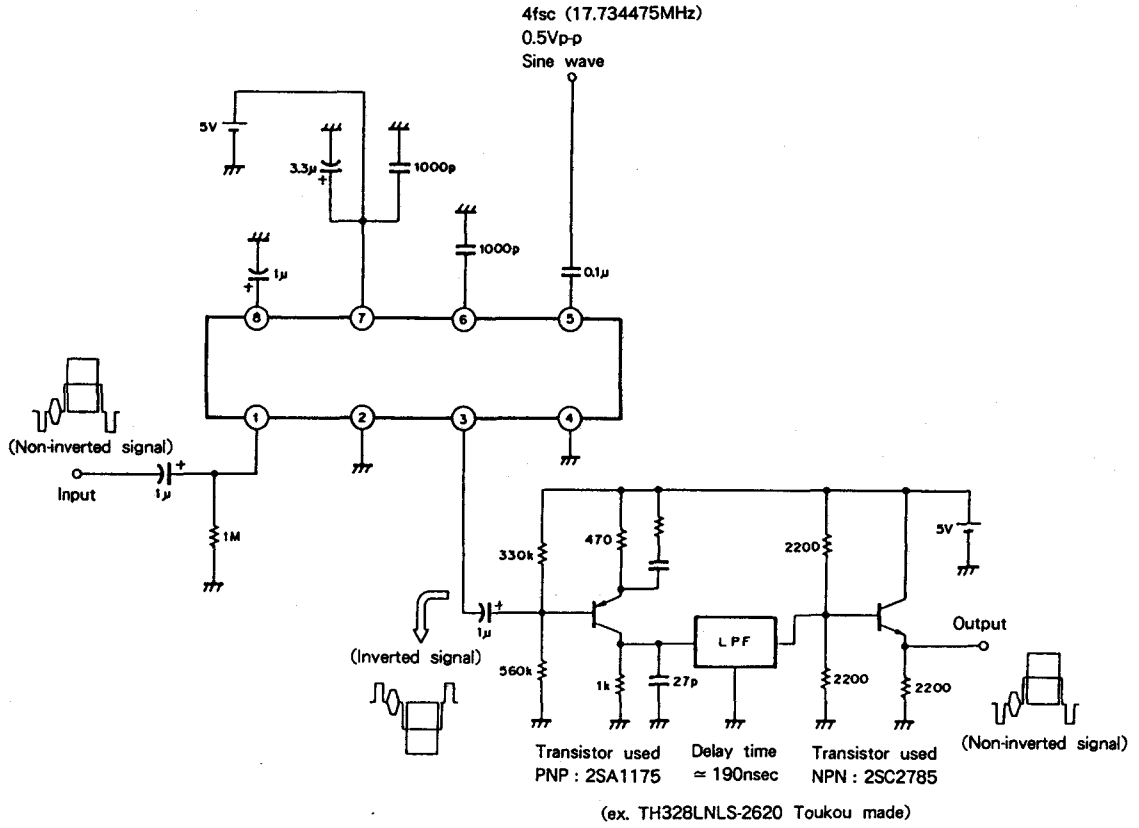
4fsc (17.734475MHz) Sine wave



Electrical Characteristics Test Circuit



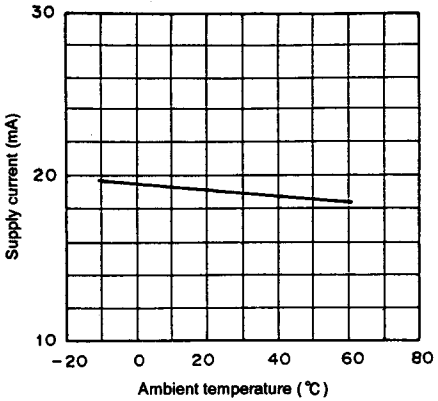
Application Circuit



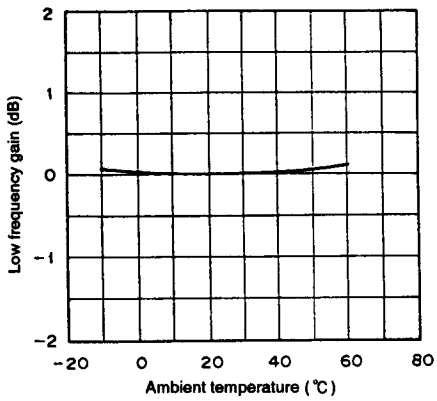
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

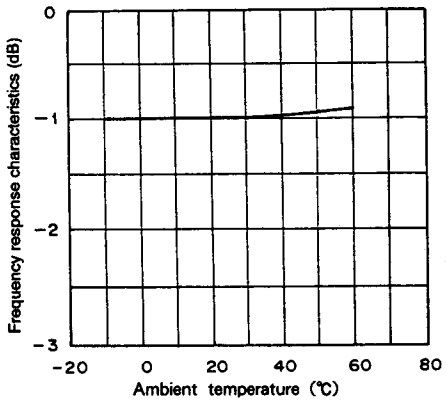
Supply current vs. Ambient temperature



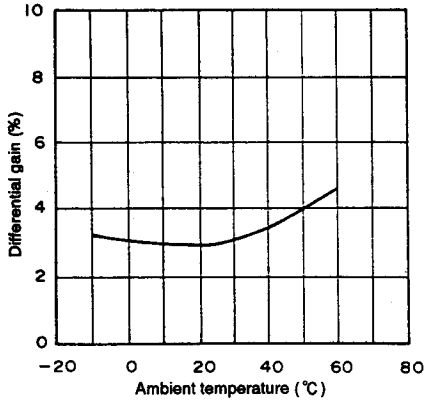
Low frequency gain vs. Ambient temperature



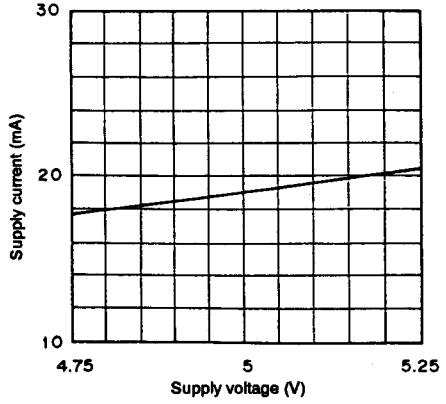
Frequency response characteristics vs. Ambient temperature



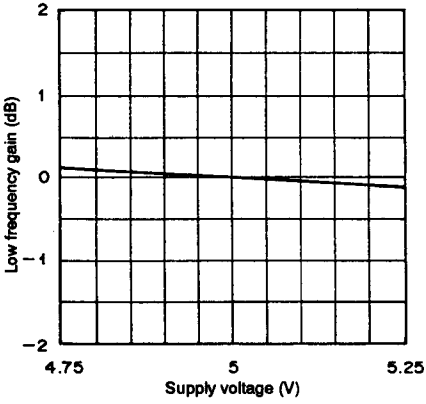
Differential gain vs. Ambient temperature



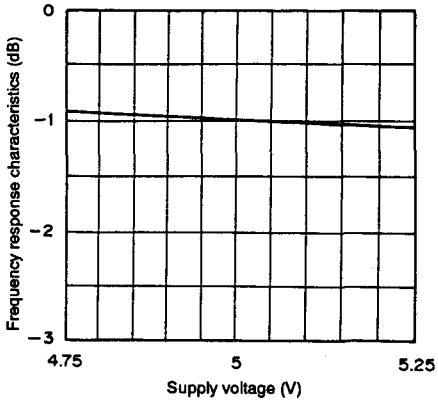
Supply current vs. Supply voltage



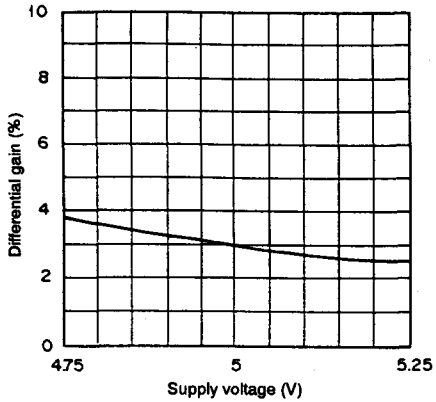
Low frequency gain vs. Supply voltage



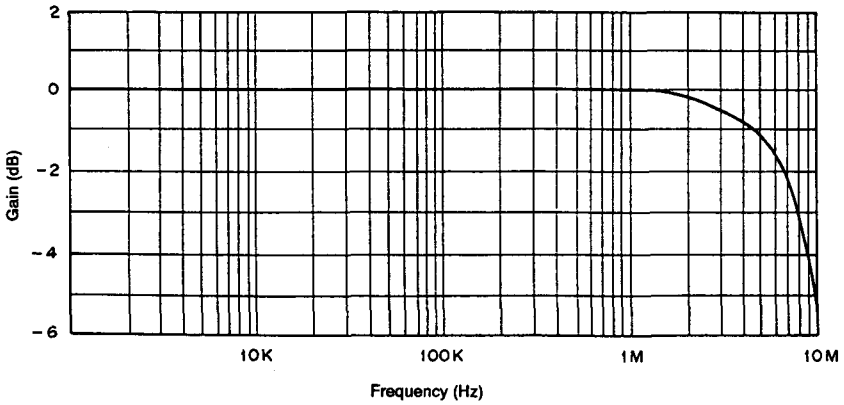
Frequency response characteristics vs. Supply voltage



Differential gain vs. Supply voltage

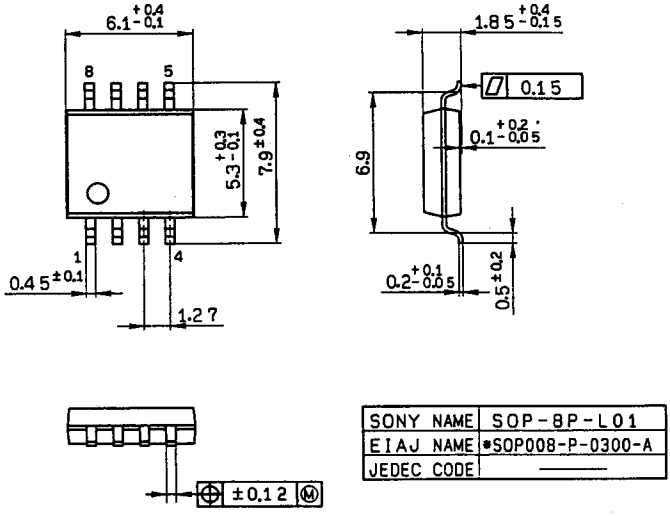


Frequency response characteristics



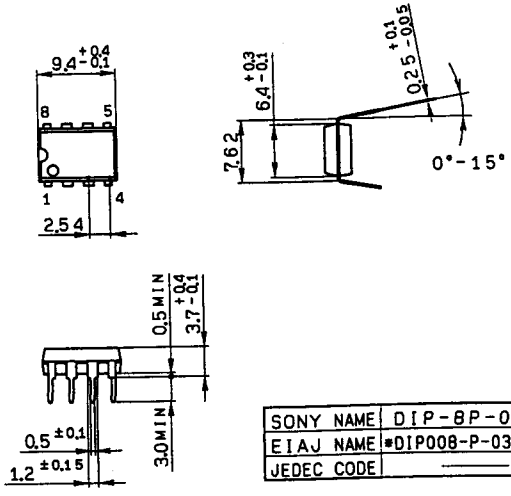
Package Outline Unit : mm

CXL5506M 8 pin SOP (Plastic) 300mil 0.1g



SONY NAME	SOP-8P-L01
EIAJ NAME	*SOP008-P-0300-A
JEDEC CODE	———

CXL5506P 8 pin DIP (Plastic) 300mil 0.5g



SONY NAME	DIP-8P-01
EIAJ NAME	*DIP008-P-0300-A
JEDEC CODE	———

SONY

CXL5507M/P

CMOS-CCD 1H Delay Line for NTSC

Description

The CXL5507M/P CMOS-CCD delay line ICs provide 1H delay for NTSC signals, including the external low pass filter.

CXL5507M
8 pin SOP (Plastic)

CXL5507P
8 pin DIP (Plastic)

Features

- Single 5V power supply
- Low power consumption 50mW (Typ.)
- Built-in peripheral circuits

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	+6	V
• Operating temperature	Topr	−10 to + 60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D		
	CXL5507M	350	mW
	CXL5507P	480	mW

Functions

- 453-bit CCD register
- Clock driver
- Auto-bias circuit
- Input clamp circuit
- Sample and hold circuit

Recommended Operating Conditions (Ta=25°C)

Supply voltage	V_{DD}	5V ± 5%

Structure

CMOS-CCD

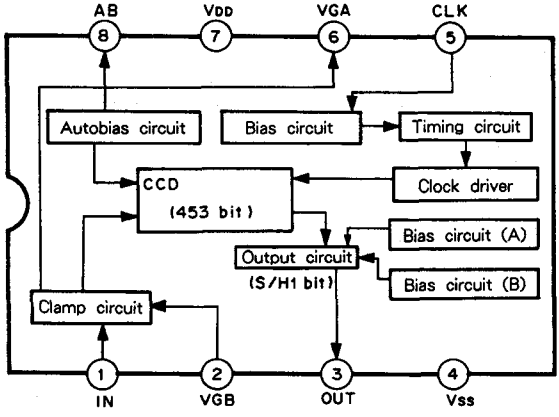
Recommended Clock Conditions (Ta=25°C)

• Input clock amplitude	V_{CLK}	0.3 to 1.0	Vp-p (0.5Vp-p Typ.)
• Clock frequency	f_{CLK}	7.159090	MHz
• Input clock waveform	Sine wave		

Input Signal Amplitude

V_{SIG} 500mVp-p (Typ.), 527mVp-p (Max.) (at internal clamp condition)

Block Diagram and Pin Configuration (Top View)



E90908 – ST

Pin Description

Pin No.	Symbol	I/O	Description	Impedance
1	IN	I	Signal input	>10kΩ at no clamp
2	VGB	I	Gate control B	
3	OUT	O	Signal output	40 to 500 Ω
4	Vss	——	GND	
5	CLK	I	Clock input	>100kΩ
6	VGA	O	Gate control A	
7	V_{DD}	——	Power supply (5V)	
8	AB	O	Auto-bias DC output	600 to 200kΩ

I/O Signals

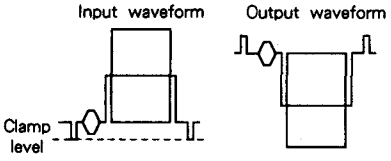
Input signals are low level clamped and output signals are inverted in relation to the input signals. Also, the clamp condition of input signals are controlled by VGB (Pin 2) conditions.

0V·····Internal clamp condition

5V·····Non internal clamp condition

Center biased to approx. 2.1V by means of the IC internal resistance (approx. 10kΩ).

Usage in this mode is limited to APL 50% signals and the maximum input signal amplitude is 200mVp-p.



Electrical Characteristics

(Ta=25 °C , V_{DD}=5V, f_{CLK}=7.159090MHz, V_{CLK}=500mVp-p, Sine wave)
See "Electrical Characteristics Test Circuit"

Item	Symbol	Test conditions	SW conditions 1	2	3	4	5	Biasing conditions V1 (V)	Min.	Typ.	Max.	Unit	Note
Supply current	IDD	——	a	a	b	a	—		5	10	15	mA	1
Low frequency gain	GL	200kHz 500mVp-p Sine wave	a	a	b	a	b		–2	0	2	dB	2
Frequency response	fg	200kHz↔2MHz 150mVp-p Sine wave	b c	a	a	b	b	2.1	–2	–1	0	dB	3
S/H pulse coupling	CP	No signal input	—	b	a	b	a	2.1	——	——	350	mVp-p	4
SN ratio	SN	No signal input	—	b	a	b	c		54	56	——	dB	5
Linearity	LIS	5 staircase wave (For luminance signals only)	b	a	b	a	a	——	37	40	43	%	6
	LIL		b	a	b	a	a		18	20	22		
	LIC		b	a	b	a	a		56	60	64		

Note

① This is the IC supply current value during clock and signal input.

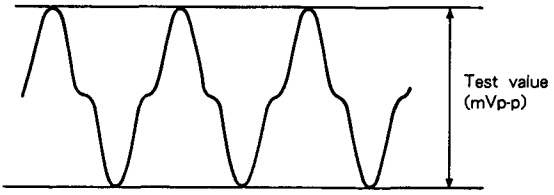
② GL is the output gain of pin OUT when a 500mVp-p, 200kHz sine wave is fed to pin IN.

$$GL=20\log \frac{\text{Pin OUT output voltage [mVp-p]}}{\text{500 [mVp-p]}} \text{ [dB]}$$

③ Indicates the dissipation at 2MHz in relation to 200kHz.
From the output voltage at pin OUT when a 150mVp-p, 200kHz sine wave is fed to pin IN, and from the output voltage at pin OUT when a 150mVp-p, 2MHz sine wave is fed to same, calculation is made according to the following formula. Input bias is tested at 2.1V.

$$fg=20\log \frac{\text{Pin OUT output voltage (2MHz) [mVp-p]}}{\text{Pin OUT output voltage (200kHz) [mVp-p]}} \text{ [dB]}$$

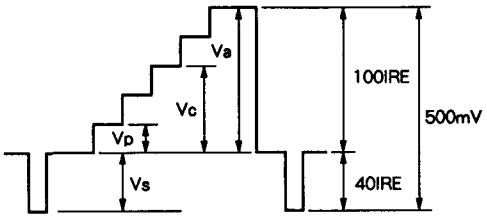
④ Leakage of internal clock components and related high frequency components to the output signal, during no signal input, is tested. Input bias is tested at 2.1V.



⑤ Input no signal noise components are tested with the video noise meter at BPF 10kHz to 3MHz. This is calculated from the output gain (GL), at the input of 200kHz, 500mVp-p and according to the following formula.

$$SN=-20 \cdot \log \frac{\text{Noise (mVrms)}}{0.5 \cdot 10^{GL/20}} \text{ [dB]}$$

⑥ Respective outputs are tested at the input of the 5 staircase waves seen in the Fig. below (luminance signals only) and calculated according to the formula below.
(However, output signals become inverted with regards to input.)



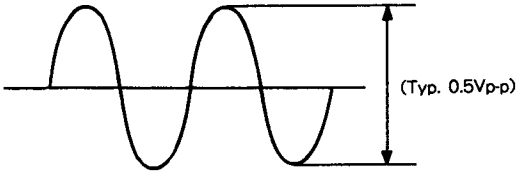
$$LIS = \frac{Vs}{Va} \times 100\ (\%)$$

$$LIL = \frac{Vp}{Va} \times 100\ (\%)$$

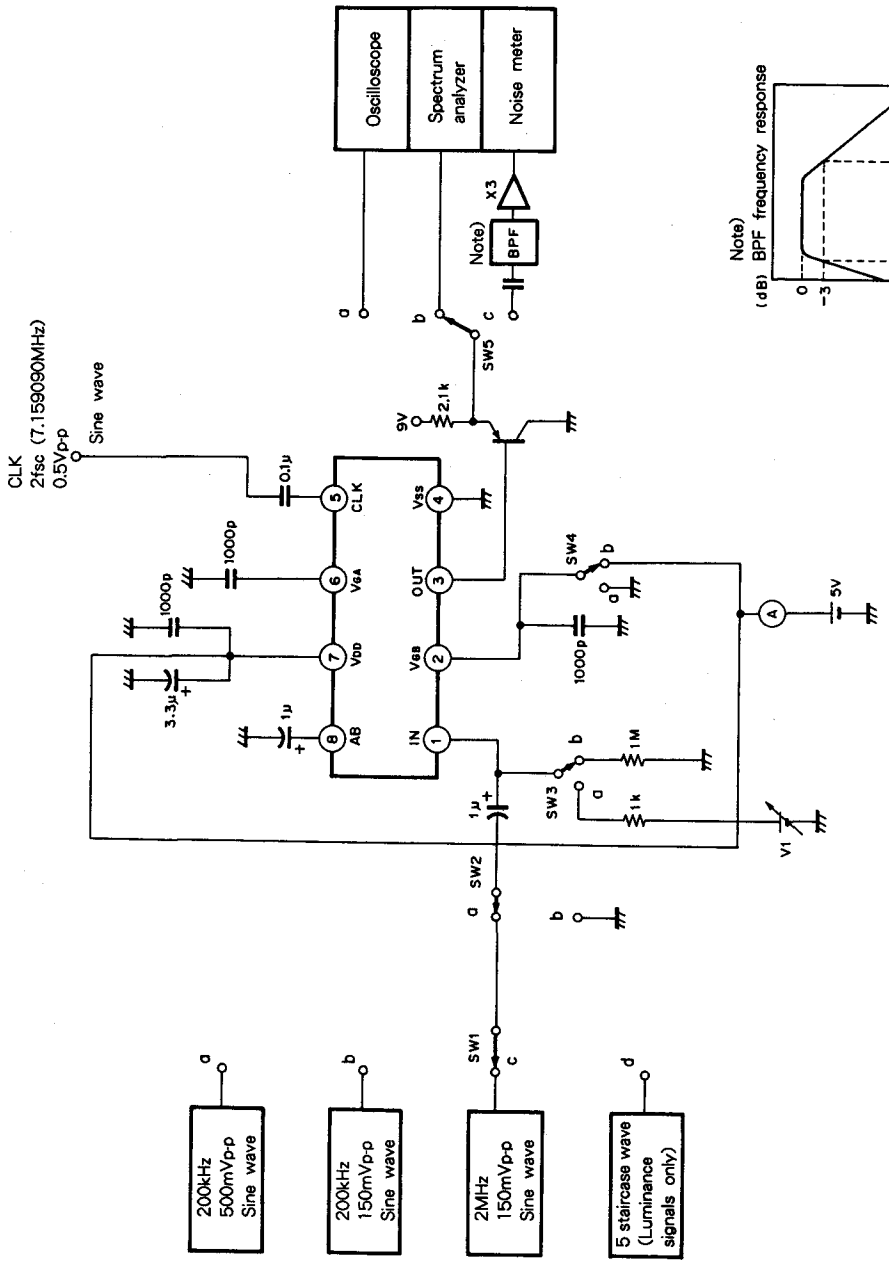
$$LIC = \frac{Vc}{Va} \times 100\ (\%)$$

Clock

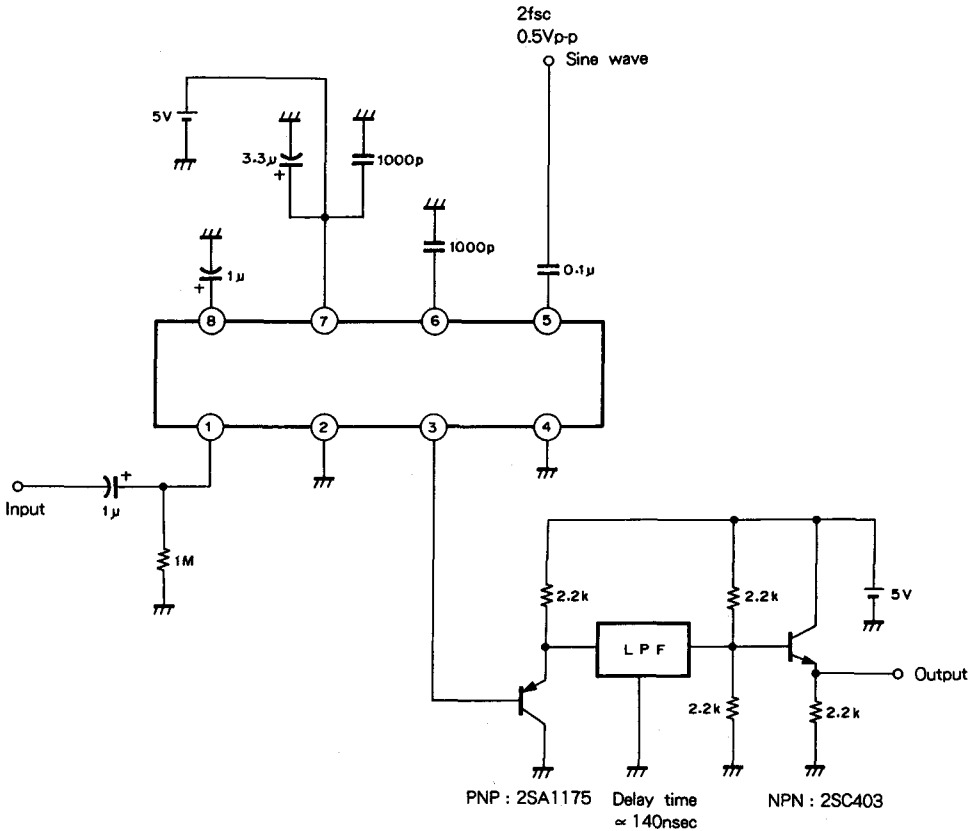
2fsc (7.159090MHz) Sine wave



Electrical Characteristics Test Circuit



Application Circuit



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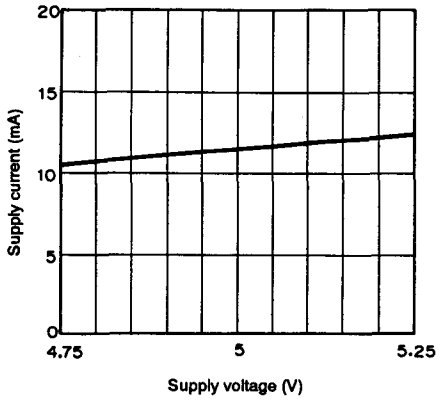
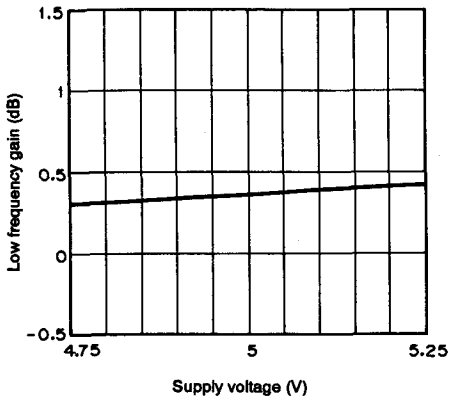
Example of Representative Characteristics

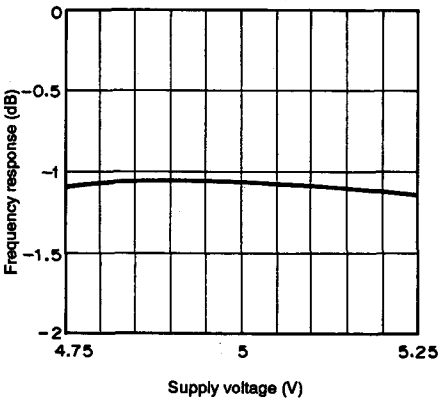
Supply current vs. Supply voltage



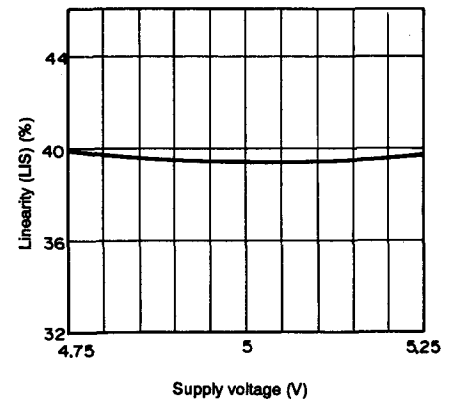
Low frequency gain vs. Supply voltage



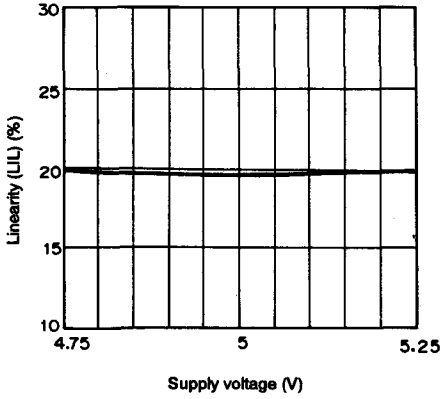
Frequency response vs. Supply voltage



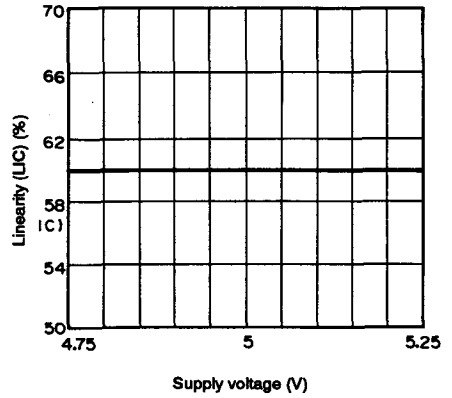
Linearity (LIS) vs. Supply voltage



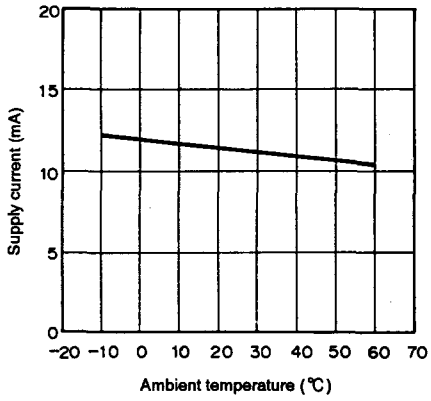
Linearity (LIL) vs. Supply voltage



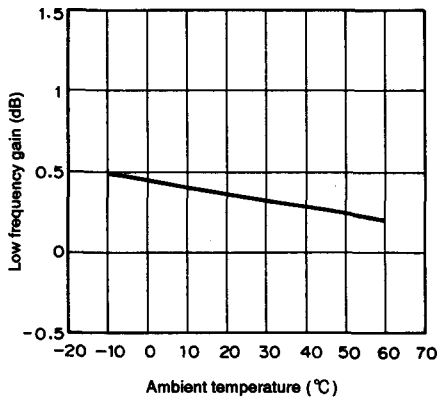
Linearity (LIC) vs. Supply current



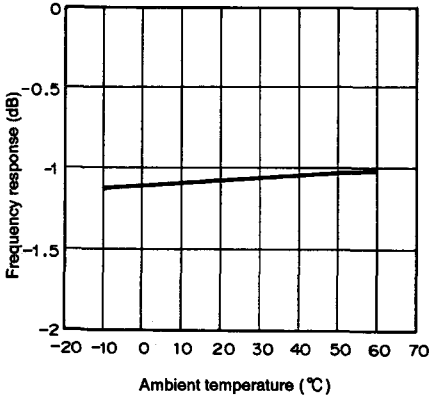
Supply current vs. Ambient temperature



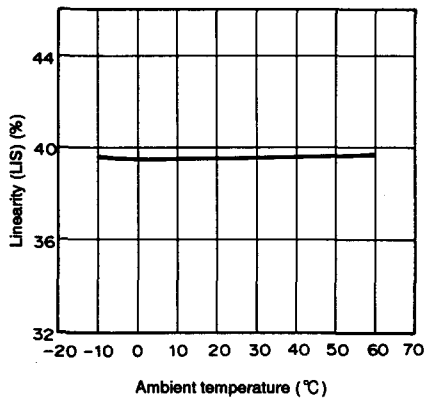
Low frequency gain vs. Ambient temperature



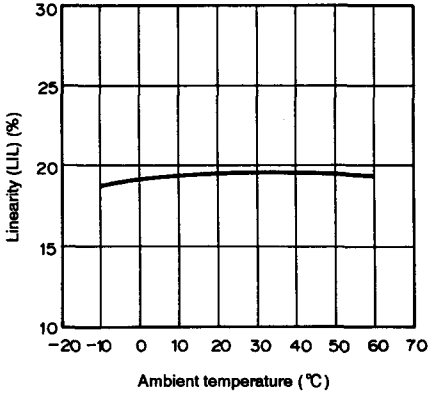
Frequency response vs. Ambient temperature



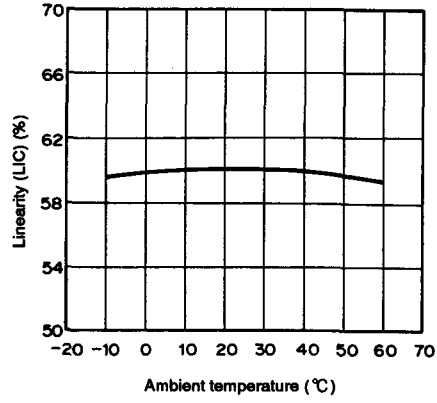
Linearity (LIS) vs. Ambient temperature



Linearity (LIL) vs. Ambient temperature

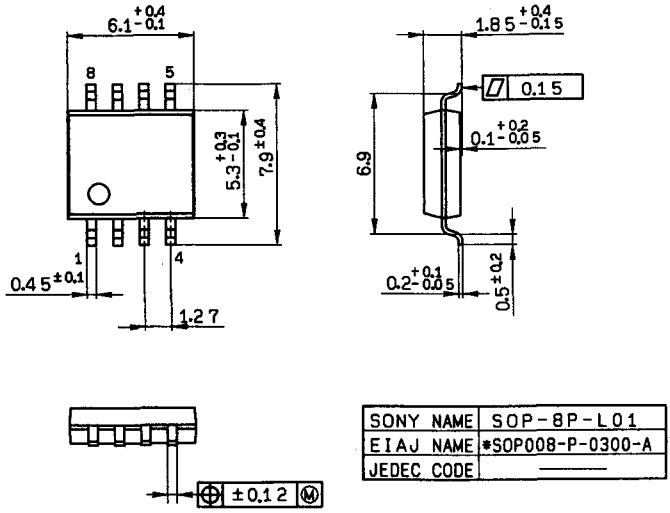


Linearity (LIC) vs. Ambient temperature



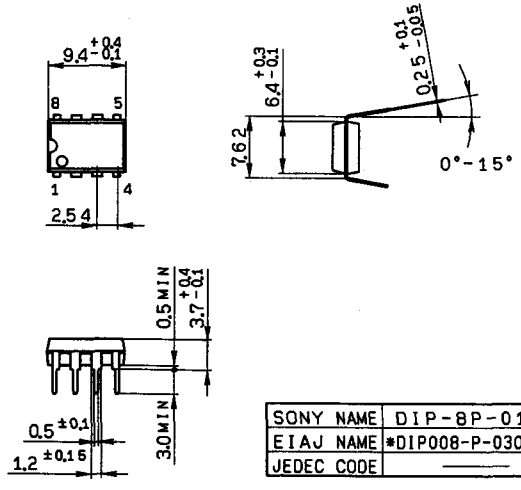
Package Outline Unit : mm

CXL5507M 8pin SOP (Plastic) 300mil 0.1g



SONY NAME	SOP-8P-L01
EIAJ NAME	*SOP008-P-0300-A
JEDEC CODE	———

CXL5507P 8pin DIP (Plastic) 300mil 0.5g



SONY NAME	DIP-8P-01
EIAJ NAME	*DIP008-P-0300-A
JEDEC CODE	———

SONY

CXL5508M/P

CMOS-CCD 1H Delay Line for PAL

Description

The CXL5508M/P CMOS-CCD delay line ICs provide 1H delay for PAL signals, including the external low pass filter.

CXL5508M	CXL5508P
8 pin SOP (Plastic)	8 pin DIP (Plastic)

Features

- Single 5V power supply
- Low power consumption 60mW (Typ.)
- Built-in peripheral circuits

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	+6	V
• Operating temperature	Topr	−10 to + 60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D		
	CXL5508M	350	mW
	CXL5508P	480	mW

Recommended Operating Conditions (Ta=25°C)

Supply voltage	V_{DD}	5V ± 5%

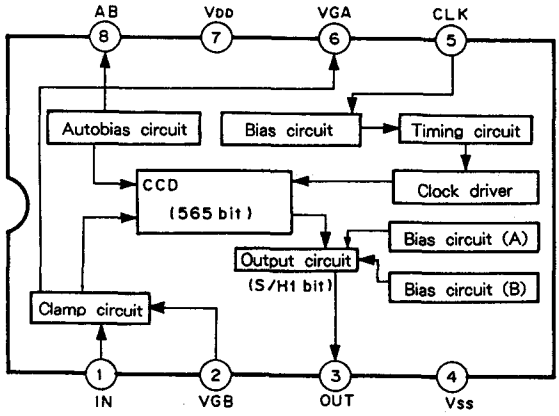
Recommended Clock Conditions (Ta=25°C)

• Input clock amplitude	V_{CLK}	0.3 to 1.0	Vp-p (0.5Vp-p Typ.)
• Clock frequency	f_{CLK}	8.867238	MHz
• Input clock waveform	Sine wave		

Input Signal Amplitude

V_{SIG} 500mVp-p (Typ.), 527mVp-p (Max.) (at internal clamp condition)

Block Diagram and Pin Configuration (Top View)



Functions

- 565-bit CCD register
- Clock driver
- Auto-bias circuit
- Input clamp circuit
- Sample and hold circuit

Structure

CMOS-CCD

E91101 – ST

Pin Description

Pin No.	Symbol	I/O	Description	Impedance
1	IN	I	Signal input	>10kΩ at no clamp
2	VGB	I	Gate control B	
3	OUT	O	Signal output	40 to 500 Ω
4	Vss	——	GND	
5	CLK	I	Clock input	>100kΩ
6	VGA	O	Gate control A	
7	V_{DD}	——	Power supply (5V)	
8	AB	O	Auto-bias DC output	600 to 200kΩ

I/O Signals

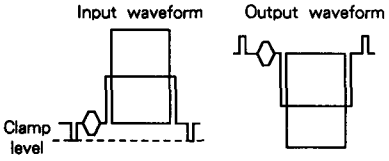
Input signals are low level clamped and output signals are inverted in relation to the input signals. Also, the clamp condition of input signals are controlled by VGB (Pin 2) conditions.

0V·····Internal clamp condition

5V·····Non internal clamp condition

Center biased to approx. 2.1V by means of the IC internal resistance (approx. 10kΩ).

Usage in this mode is limited to APL 50% signals and the maximum input signal amplitude is 200mVp-p.



Electrical Characteristics

(Ta=25℃, V_{DD}=5V, f_{CLK}=8.867238MHz, V_{CLK}=500mVp-p, Sine wave)

See "Electrical Characteristics Test Circuit"

Item	Symbol	Test conditions	SW conditions 1	2	3	4	5	Biasing conditions V1 (V)	Min.	Typ.	Max.	Unit	Note
Supply current	IDD	——	a	a	b	a	—		7	12	17	mA	1
Low frequency gain	GL	200kHz 500mVp-p Sine wave	a	a	b	a	b		–2	0	2	dB	2
Frequency response	fg	200kHz↔2MHz 150mVp-p Sine wave	b c	a	a	b	b	2.1	–1.8	–1.8	0	dB	3
S/H pulse coupling	CP	No signal input	—	b	a	b	a	2.1	——	——	350	mVp-p	4
SN ratio	SN	No signal input	—	b	a	b	c		54	56	——	dB	5
Linearity	LIS	5 staircase wave (For luminance signals only)	b	a	b	a	a	——	37	40	43	%	6
	LIL		b	a	b	a	a		18	20	22		
	LIC		b	a	b	a	a		56	60	64		

Note

① This is the IC supply current value during clock and signal input.

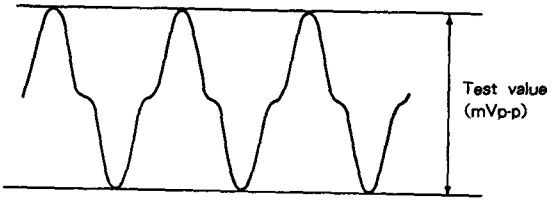
② GL is the output gain of pin OUT when a 500mVp-p, 200kHz sine wave is fed to pin IN.

$$GL=20\log \frac{\text{Pin OUT output voltage [mVp-p]}}{\text{500 [mVp-p]}} \text{ [dB]}$$

③ Indicates the dissipation at 2MHz in relation to 200kHz.
From the output voltage at pin OUT when a 150mVp-p, 200kHz sine wave is fed to pin IN, and from the output voltage at pin OUT when a 150mVp-p, 2MHz sine wave is fed to same, calculation is made according to the following formula. Input bias is tested at 2.1V.

$$fg=20\log \frac{\text{Pin OUT output voltage (2MHz) [mVp-p]}}{\text{Pin OUT output voltage (200kHz) [mVp-p]}} \text{ [dB]}$$

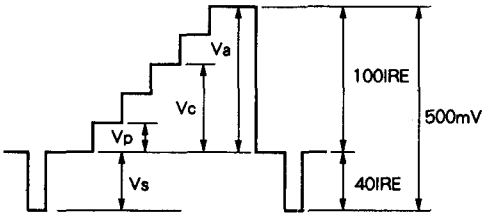
④ Leakage of internal clock components and related high frequency components to the output signal, during no signal input, is tested. Input bias is tested at 2.1V.



⑤ Input no signal noise components are tested with the video noise meter at BPF 10kHz to 3MHz. This is calculated from the output gain (GL), at the input of 200kHz, 500mVp-p and according to the following formula.

$$SN=-20 \cdot \log \frac{\text{Noise (mVrms)}}{0.5 \cdot 10^{GL/20}} \text{ [dB]}$$

⑥ Respective outputs are tested at the input of the 5 staircase waves seen in the Fig. below (luminance signals only) and calculated according to the formula below.
(However, output signals become inverted with regards to input.)



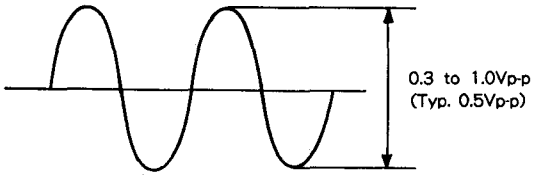
$$LIS = \frac{Vs}{Va} \times 100\ (\%)$$

$$LIL = \frac{Vp}{Va} \times 100\ (\%)$$

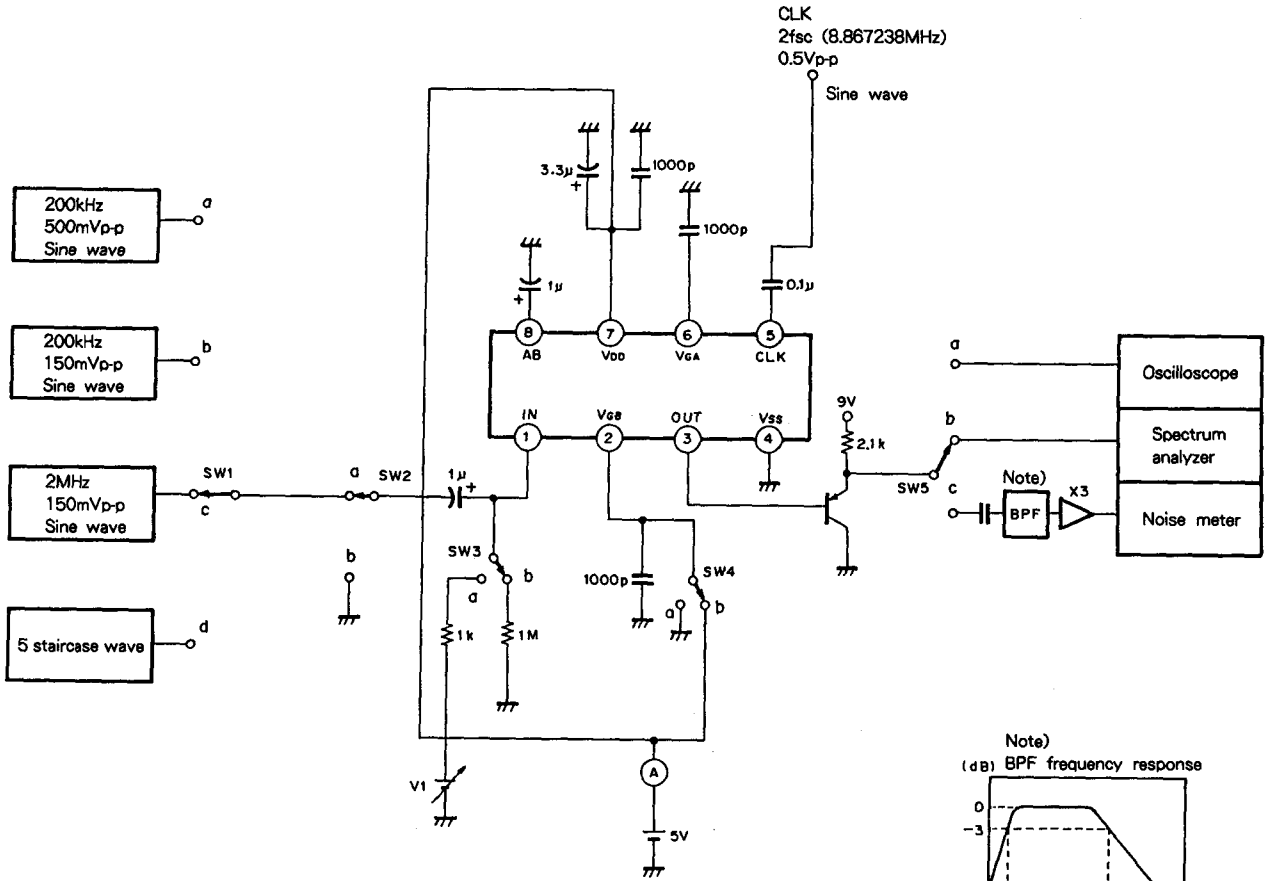
$$LIC = \frac{Vc}{Va} \times 100\ (\%)$$

Clock

2fsc (8.867238MHz) Sine wave



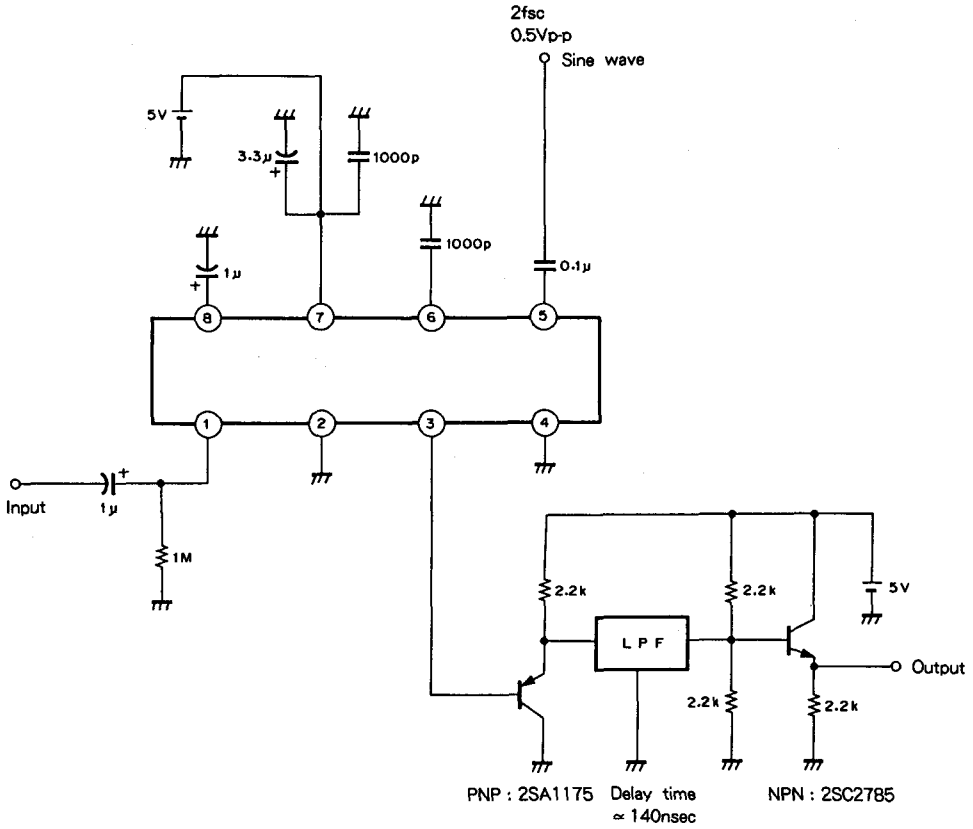
Electrical Characteristics Test Circuit



SONY

CXL5508M/P

Application Circuit



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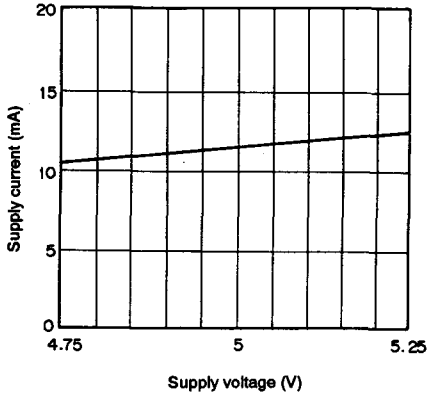
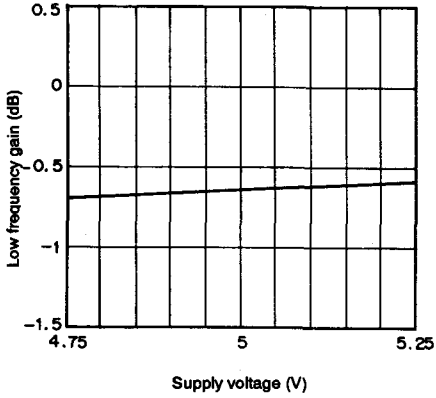
Example of Representative Characteristics

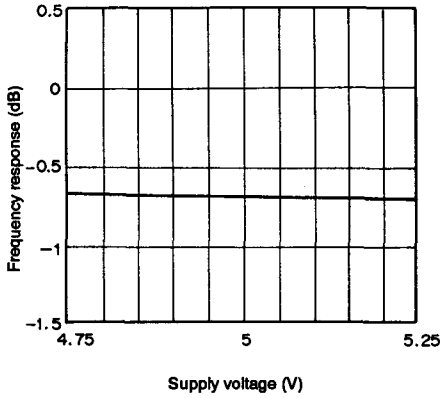
Supply current vs. Supply voltage



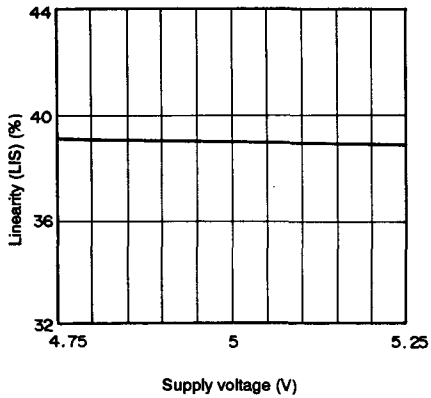
Low frequency gain vs. Supply voltage



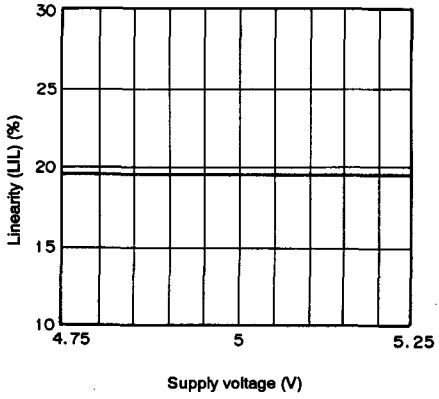
Frequency response vs. Supply voltage



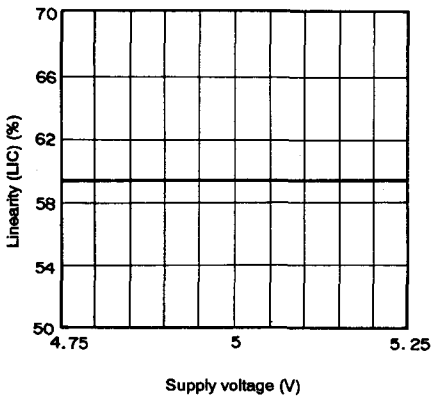
Linearity (LIS) vs. Supply voltage



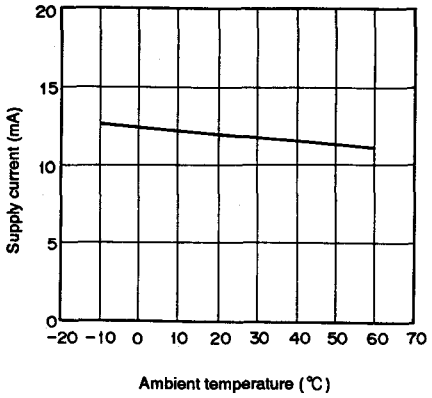
Linearity (LIL) vs. Supply voltage



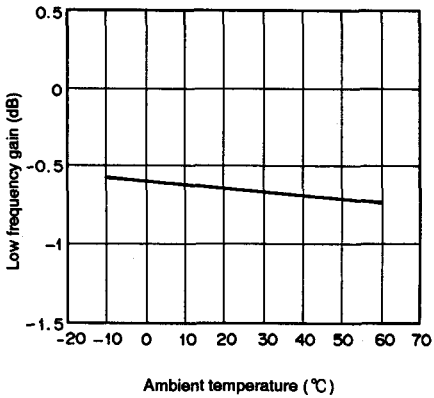
Linearity (LIC) vs. Supply current



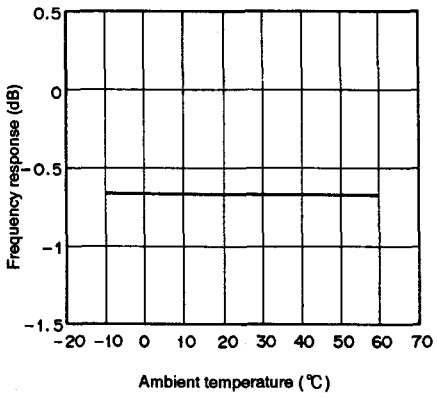
Supply current vs. Ambient temperature



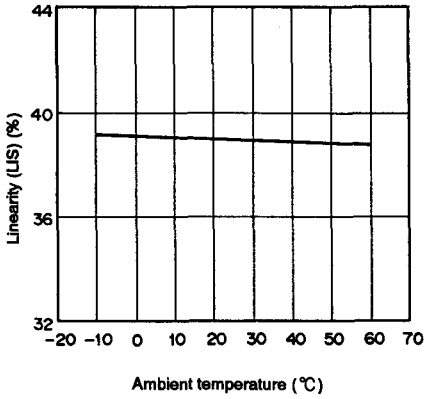
Low frequency gain vs. Ambient temperature



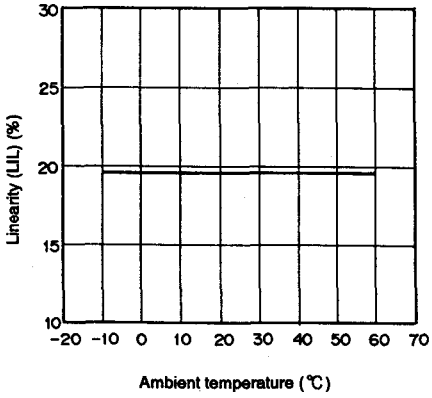
Frequency response vs. Ambient temperature



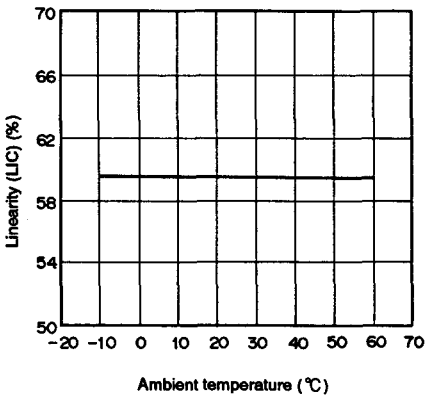
Linearity (LIS) vs. Ambient temperature



Linearity (LIL) vs. Ambient temperature

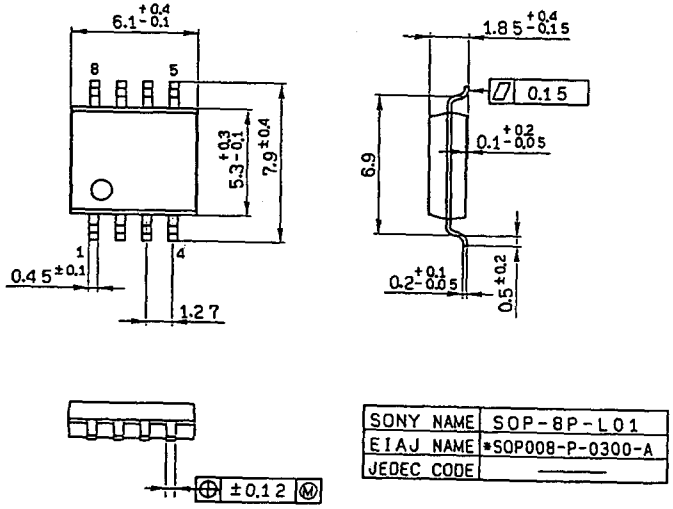


Linearity (LIC) vs. Ambient temperature



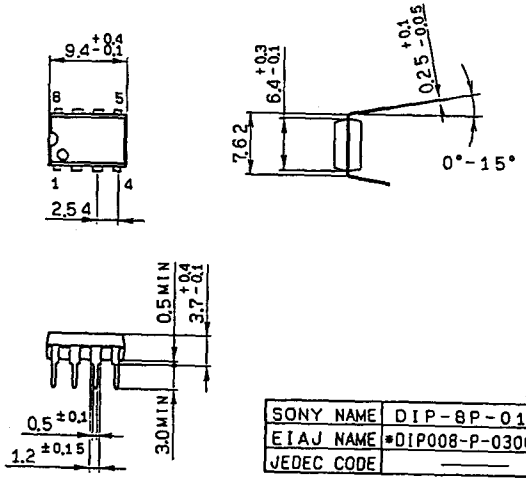
Package Outline Unit : mm

CXL5508M 8pin SOP (Plastic) 300mil 0.1g



SONY NAME	SOP-8P-L01
EIAJ NAME	*SOP008-P-0300-A
JEDEC CODE	———

CXL5508P 8pin DIP (Plastic) 300mil 0.5g



SONY NAME	DIP-8P-01
EIAJ NAME	*DIP008-P-0300-A
JEDEC CODE	———

SONY

CXL5509M/P

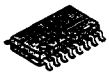
CMOS-CCD 1H/2H Delay Line for NTSC

Preliminary

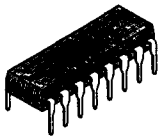
Description

CXL5509M/P is a CMOS-CCD delay line developed for video signal processing. Usage in conjunction with an external low pass filter provide 1H and 2H delay signals simultaneously (For NTSC signals).

CXL5509M
16 pin SOP (Plastic)



CXL5509P
16 pin DIP (Plastic)



Features

- Single power supply (5V)
- Low power consumption 130mW (Typ.)
- Built-in peripheral circuits
- Built-in quadruple progression PLL circuit
- For NTSC signals
- 1 input and 2 outputs
  (Outputs for both 1H and 2H delays)

Functions

- 906-bit (1H) and 1816-bit (2H) CCD register
- Clock driver
- Autobias circuit
- Sync tip clamp circuit
- Sample and hold circuit
- Quadruple progression PLL circuit

Absolute Maximum Ratings (Ta=25℃)

• Supply voltage	V_{DD}	+6	V
• Operating temperature	Topr	−10 to +60	℃
• Storage temperature	Tstg	−55 to +150	℃
• Allowable power dissipation			
	P_D	CXL5509M 400	mW
		CXL5509P 800	mW

Structure

CMOS-CCD

Recommended Operating Voltage (Ta=25℃)

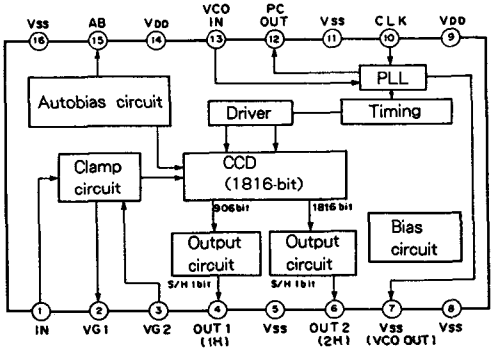
V_{DD} 5V ± 5 %

Recommended Clock Conditions (Ta=25℃)

- Input clock amplitude V_{CLK} 0.3 to 1.0Vp-p (0.5Vp-p Typ.)
- Input clock frequency f_{CLK} 3.579545 MHz
- Input clock waveform sine wave

Input Signal Amplitude V_{SIG} 571 (MAX.) mVp-p (at internal clamp condition)

Block Diagram



PE91401 – ST

Pin Description

No.	Symbol	I/O	Description	Impedance (Ω)
1	IN	I	Signal input (Non-inverted signal)	>10kΩ (at no clamp)
2	VG1	O	Gate bias 1 DC output	
Note) 3	VG2	I	Gate bias 2 DC input	
4	OUT1	O	1H signal output (Inverted signal)	40 to 500 Ω
5	Vss	——	GND	
6	OUT2	O	2H signal output (Inverted signal)	40 to 500 Ω
7	Vss (VCOOUT)	(O)	GND or VCO output (4fsc)	
8	Vss	——	GND	
9	V_{DD}	——	Power supply (5V)	
10	CLK	I	Clock input (fsc)	>10kΩ
11	Vss	——	GND	
12	PC OUT	O	Phase comparator output	
13	VCO IN	I	VCO input	
14	V_{DD}	——	Power supply (5V)	
15	AB	O	Autobias DC output	600 to 200kΩ
16	Vss	——	GND	

Note) Description of Pin 3 (VG2)

Control of input signal clamp condition

0V·····Sync chip clamp condition

5V·····Center bias condition

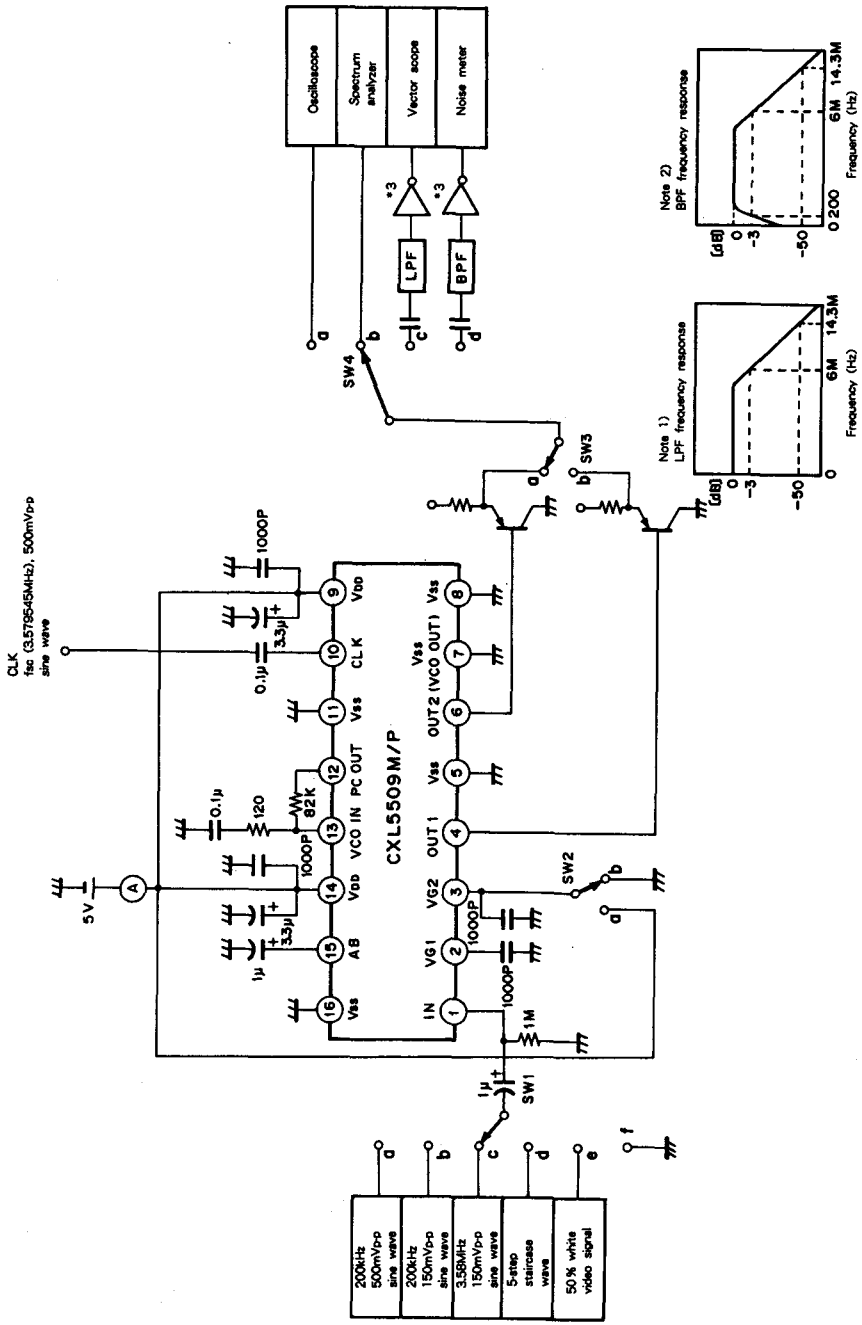
The input signal is biased to approx. 2.1V by means of the IC internal resistance (approx. 10kΩ). In this mode the input signal is limited to the APL 50% and the maximum input signal amplitude is at 200mVp-p.

Electrical Characteristics

(Ta=25°C, V_{DD}=5V, f_{CLK}=3.579545MHz, V_{CLK}=500mVp-p sine wave)
See Electrical Characteristics Test Circuit

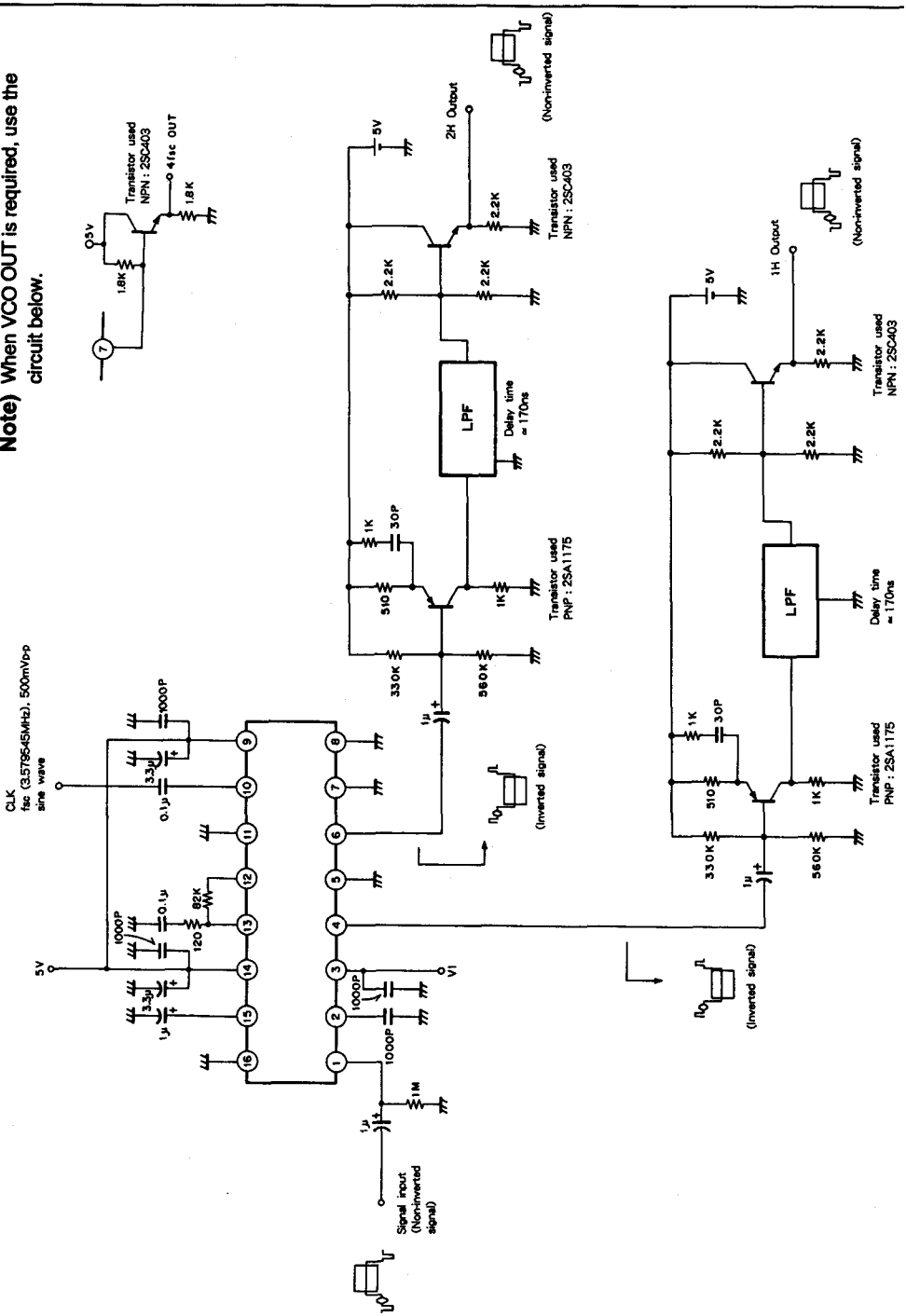
Item	Symbol	Test conditions (NOTE 1)	SW conditions 1	2	3	4	Min.	Typ.	Max.	Unit	NOTE
Supply current	I_{DD}	—	a	b	a	a	16	26	36	mA	2
Low frequency gain	GL1	200kHz 500mVp-p sine wave	a	b	a	b	–2	0	2	dB	3
	GL2		a	b	b	b	–2	0	2		
Frequency response	fR1	200kHz↔3.58MHz 150mVp-p sine wave	b↔c	a	a	b	–2.0	–1.0	0	dB	4
	fR2		b↔c	a	b	b	–2.0	–1.0	0		
Differential gain	DG1	5 staircase wave	d	b	a	c	—	3	5	%	5
	DG2		d	b	b	c	—	3	5		
Differential phase	DP1	5 staircase wave	d	b	a	c	—	3	5	degree	5
	DP2		d	b	b	c	—	3	5		
SN ratio	SN1	50% white video signal	e	b	a	d	52	56	—	dB	6
	SN2		e	b	b	d	52	56	—		
S/H pulse feed through	CP1	No signal input	f	b	a	a	—	—	350	mVp-p	7
	CP2		f	b	b	a	—	—	350		

Electrical Characteristics Test Circuit



Application Circuit

Note) When VCO OUT is required, use the circuit below.



NOTE)

1) By switching SW2, input condition turns out as follows.

SW2 condition	Input condition
a	Center bias condition (approx. 2.1V) Approx. 2.1V bias is applied internally to the input signal
b	Sync chip and clamp conditions

2) This is the supply current value during IC operation. Here the signal is input.

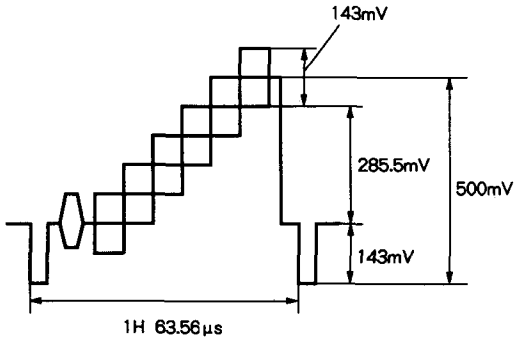
3) GL is the output gain of pin OUT when a 500mVp-p, 200kHz sine wave is fed to pin IN.

$$GL=20\log \frac{\text{pin OUT output voltage [mVp-p]}}{\text{500 [mVp-p] [dB]}} \text{ [dB]}$$

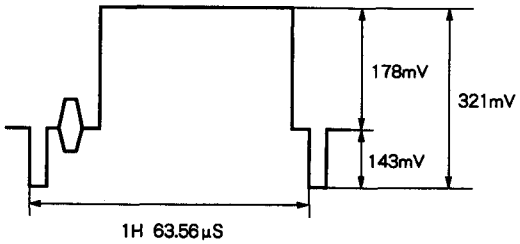
4) Indicates the dissipation at 3.58MHz in relation to 200kHz. From the output voltage at pin OUT when a 150mVp-p, 200kHz sine wave is fed to pin IN, and from the output voltage at pin OUT when a 150mVp-p, 3.58MHz sine wave is fed to same, calculation is made according to the following formula.

$$fR=20\log \frac{\text{pin OUT output voltage (3.58MHz) [mVp-p]}}{\text{pin OUT output voltage (200kHz) [mVp-p]}} \text{ [dB]}$$

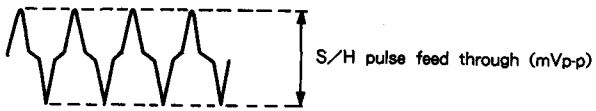
5) The differential gain (DG) and the differential phase (DP), when the 5-step staircase wave in the following figure is fed, are tested with a vector scope:



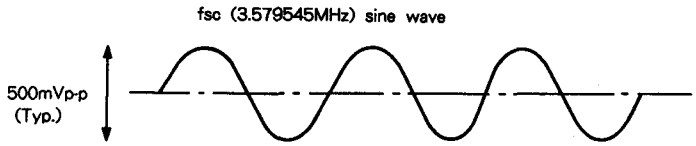
6) S/N ratio during 50% white video signal input shown in Fig. below is tested at video noise meter, in BPF 100kHz to 4MHz, Sub Carrier Trap mode.



7) The internal clock component to the output signal during no-signal input and the leakage of that high harmonic component are tested.

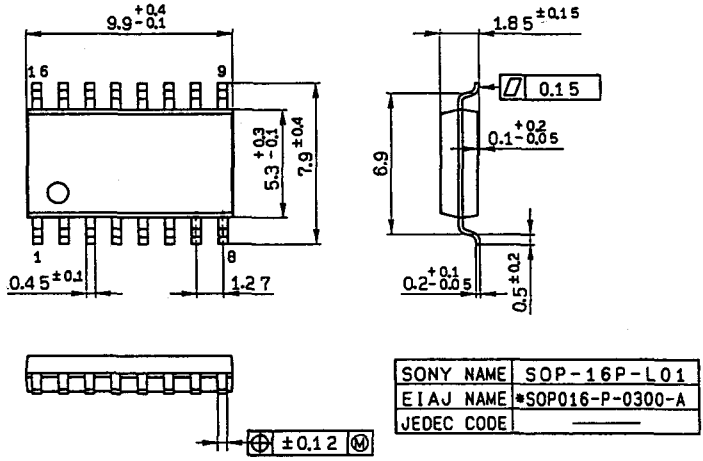


CLOCK



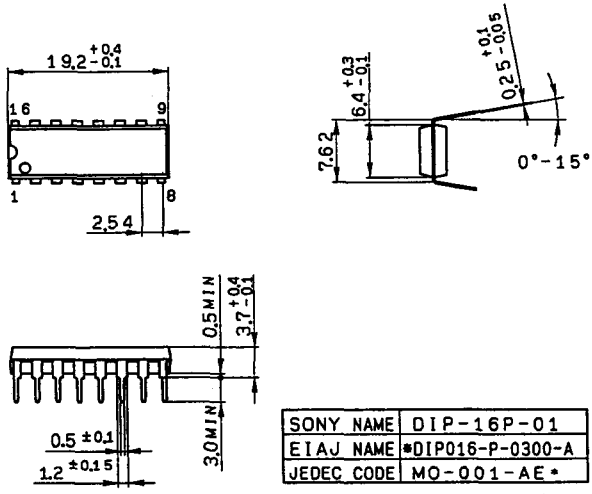
Package Outline Unit : mm

16pin SOP (Plastic) 300mil 0.2g



SONY NAME	SOP-16P-L01
EIAJ NAME	*SOP016-P-0300-A
JEDEC CODE	———

16pin DIP (Plastic) 300mil 1.0g



SONY NAME	DIP-16P-01
EIAJ NAME	*DIP016-P-0300-A
JEDEC CODE	MO-001-AE*

* (Similar)

SONY

CXL1009P

CMOS-CCD Signal Processor for TBC

Description

CXL1009P is a CMOS-CCD signal processor developed for Time Base Corrector (TBC).

Features

- Low power consumption 160 mW (Typ.)
- Wide variable frequency range (15.2 to 27.2 MHz)
- Built-in peripheral circuits

Functions

- 680 bit CCD register x 2
- Clock drivers
- Autobias circuit (For Audio/Video)
- Sync tip clamp circuit
- T-type flip-flop circuit
- Timing generator circuit
- Output feedback circuit

Structure

CMOS-CCD

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	11		V
• Supply voltage	V_{CL}	6		V
• Operating temperature	Topr	−10 to	+60	°C
• Storage temperature	Tstg	−55 to	+150	°C
• Allowable power dissipation	P_D	1		W

Recommended Operating Conditions

• Supply voltage	V_{DD}	9	V ±5%
• Supply voltage	V_{CL}	9	V ±5%

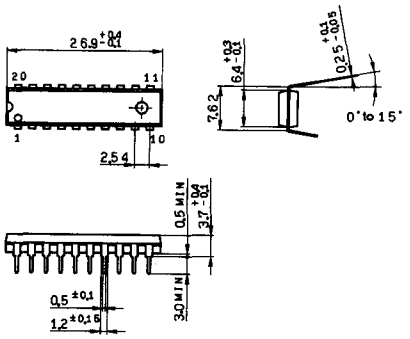
Recommended Input Signal Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Input amplitude	V_{INP-P}	–	1.0	1.28	Vp-p

Package Outline

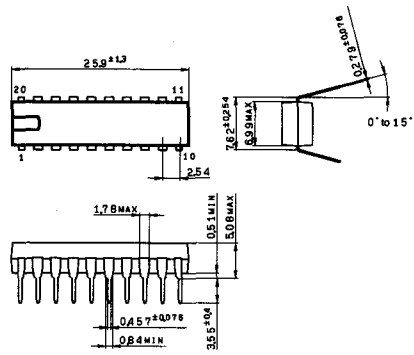
Unit: mm

20 pin DIP (Plastic)



DIP-20P-02

20 pin DIP (Plastic)



DIP-20P-121

Recommended Clock Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Clock frequency	f_{CK}	15.2	21.4	27.2	MHz	Pulse or Sinewave*
Clock amplitude	V_{CKP-P}	1.0	2.0	4.0	Vp-p	
Duty (during pulse)	Dy	40	50	60	%	

***Note)** During pulse the clock requires a pulse as shown in Fig. 1.

E88Z37-YA

Recommended Clock Waveform (Pulse)

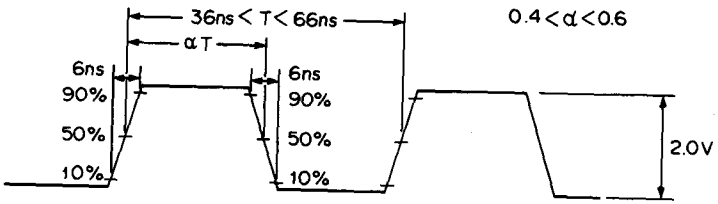
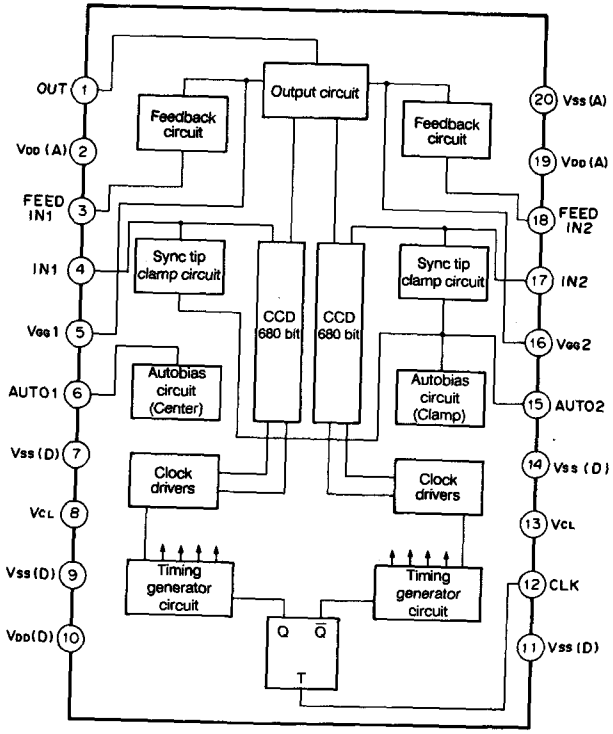


Fig. 1

Block Diagram and Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	OUT	O	Output
2	V_{DD} (A)		Power supply 1 (Analog)
3	FEED IN1	I	Feedback input 1
4	IN1	I	Input 1
5	V_{GG} 1	I	Gate1
6	AUTO1	O	Autobias 1
7	V_{SS} (D)		GND (Digital)
8	V_{CL}		Power supply 2 (Digital)
9	V_{SS} (D)		GND (Digital)
10	V_{DD} (D)		Power supply 1 (Digital)
11	V_{SS} (D)		GND (Digital)
12	CLK	I	Clock input
13	V_{CL}		Power supply 2 (Digital)
14	V_{SS} (D)		GND (Digital)
15	AUTO2	O	Autobias 2
16	V_{GG} 2	I	Gate 2
17	IN2	I	Input 2
18	FEED IN2	I	Feedback input 2
19	V_{DD} (A)		Power supply 1 (Analog)
20	V_{SS} (A)		GND (Analog)

Electrical Characteristics 1

Ta = 25°C, V_{DD} = 9.0V, V_{CL} = 5.0V, See the Electrical Characteristics Test Circuit.

Item	Symbol	Test conditions	SW condition				Test point	Min.	Typ.	Max.	Unit
			SW1	SW2	SW3	SW4					
Pin voltage	$V_{AUTO1-DC}$	Pin 6 voltage	b	a	a	a	V6	4.0	5.5	7.0	V
	$V_{AUTO2-DC}$	Pin 15 voltage	b	a	a	a	V5	3.5	5.0	6.5	V
	V_{IN-DC}	Pins 4 and 17 voltage	b	b	a	a	V7	3.5	5.0	6.5	V
	V_{GG-DC}	Pins 5 and 16 voltage	a	a	a	a	V8	1.0	2.0	3.0	V
			b								
			c								

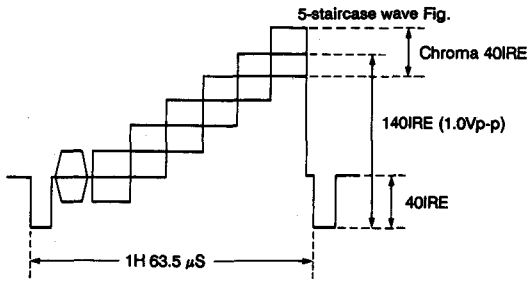
Electrical Characteristics 2

Ta = 25°C, V_{DD} = 9.0V, V_{CL} = 5.0V, See the Electrical Characteristics Test Circuit.
Test conditions: Set the voltage of pins E1 and E2 as follows:
E1 = $V_{GG\text{-}DC}$, E2 = $V_{AUTO2\text{-}DC}$ + 0.65V or $V_{AUTO1\text{-}DC}$

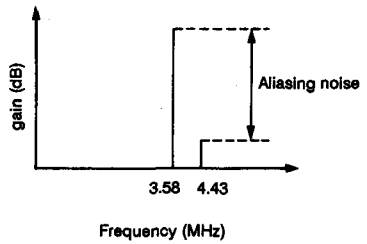
Item	Symbol	Test conditions	SW condition				Test point	Min.	Typ.	Max.	Unit
			SW1	SW2	SW3	SW4					
Supply current	I_{DD}	250 kHz, 1.0Vp-p sine wave input	b	a	a	a	A1	–	7	12	mA
	I_{CL}						A2	–	20	28	mA
Insertion gain	IG	250 kHz, 1.0Vp-p sine wave input $IG = 20\log\left[\frac{\text{Output voltage (Vp-p)}}{\text{1Vp-p}}\right]$	a to c	a	a	b	V2	–3	0	3	dB
Frequency response	f_G	Dissipation at 3.58 MHz vs. 250 kHz $f_G = 20\log(V_{3.58MHz}/V_{250kMz})$ $V_{3.58MHz}$: Output signal voltage during 3.58 MHz input V_{250kMz}: Output signal voltage during 250 kHz input	a to c	a	b	b	V2	–3	–1	0	dB
Differential gain	DG	5-staircase wave (See Fig.) input Y = 140IRE (= 1.0Vp-p) Measuring with vectorscope.*1	a to c	a	c	b	S	–	3	5	%
Differential phase	DP							–	3	5	Deg
Noise	S/N1	S: Input = 250 kHz, 1.0Vp-p sine wave	b	a	a	c	V3	50	55	–	dB
		N: Input = Alternating grounding point (rms)	b	a	d	c					
Aliasing noise	S/N2	Input = 3.58 MHz, 1.0Vp-p sine wave *2	d	a	b	d	SA	35	50	–	dB
Insertion gain difference	ΔIG	250 kHz, 1.0Vp-p sine wave *3	a to c	a	a	b	V2	–	1	2.4	%
DC output voltage difference	$\Delta V_{O\text{-}DC}$	250 kHz, 1.0Vp-p sine wave *4	a to c	a	a	a	V1	–	–	0.3	V

Note)

*1. Differential gain and differential phase conditions.



*2. Aliasing noise
Measure with a spectrum analyzer the 4.43 MHz output signal voltage at 3.58 MHz input (clock frequency 16.02 MHz).



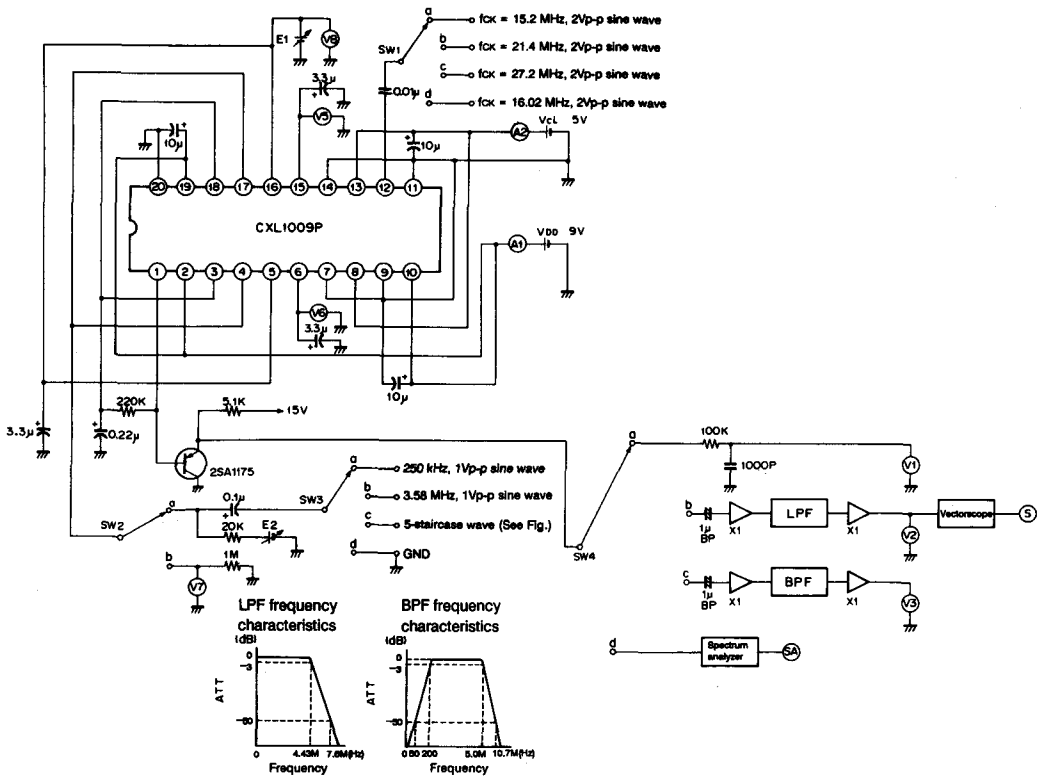
*3. Insertion gain difference
With the insertion gain of clock frequencies of 15.2 MHz, 21.4 MHz and 27.2 MHz, determine maximum value as IGmax [dB] and minimum value as IGmin [dB]. Insertion gain difference ⊿IG is defined as follows.

$$\Delta IG = \frac{10^{(IGmax/20)} - 10^{(IGmin/20)}}{10^{(IGmax/20)} + 10^{(IGmin/20)}} \times 200\ [\%]$$

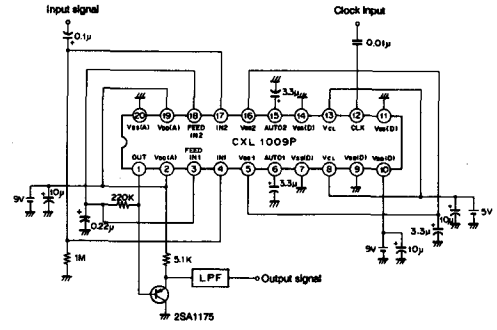
*4. DC output voltage difference
With the DC output voltage of clock frequencies of 15.2 MHz, 21.4MHz and 27.2 MHz, determine maximum value as $V_{O\text{-}DC}max$ and minimum value as $V_{O\text{-}DC}min$. DC output voltage difference ⊿$V_{O\text{-}DC}$ is defined as follows.

$$\Delta V_{O\text{-}DC} = V_{O\text{-}DC}\ max - V_{O\text{-}DC}\ min\ [V]$$

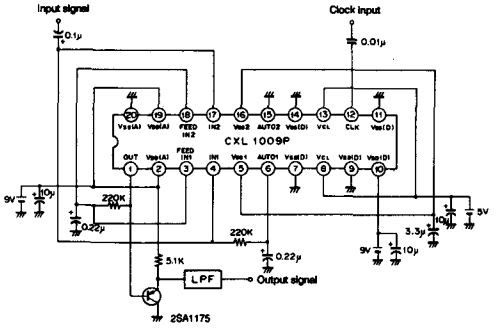
Electrical Characteristics Test Circuit



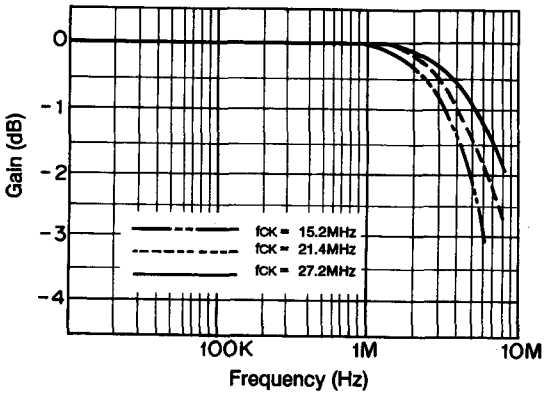
Application Circuit (Video)



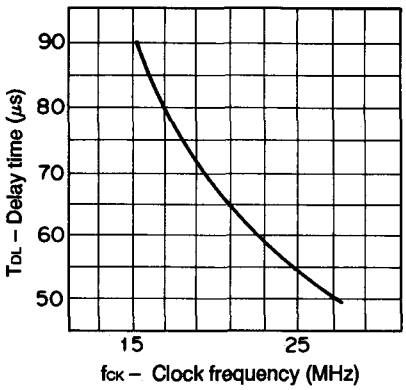
Application Circuit (Audio)



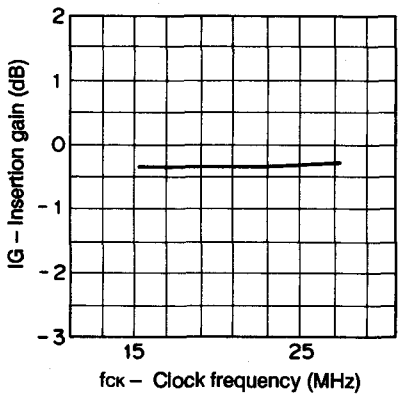
Frequency characteristics



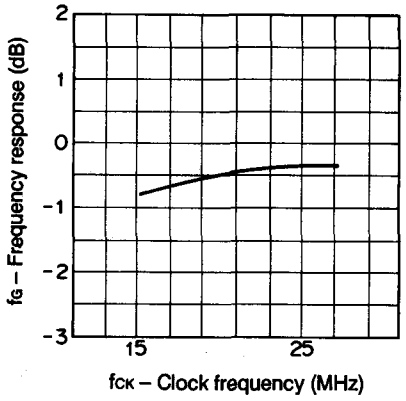
Delay time vs. Clock frequency



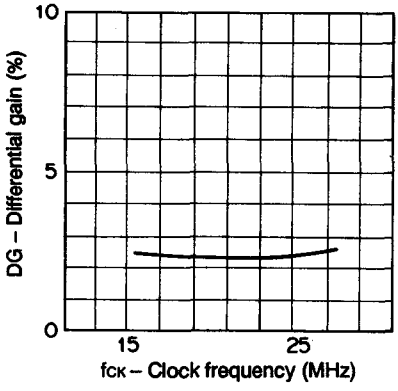
Insertion gain vs. Clock frequency



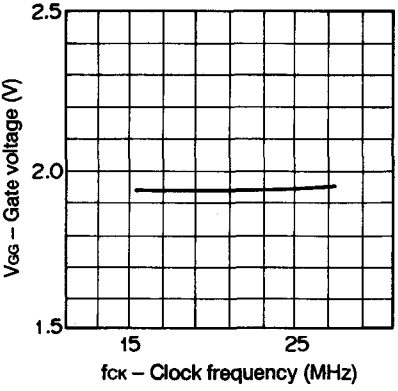
Frequency response vs. Clock frequency



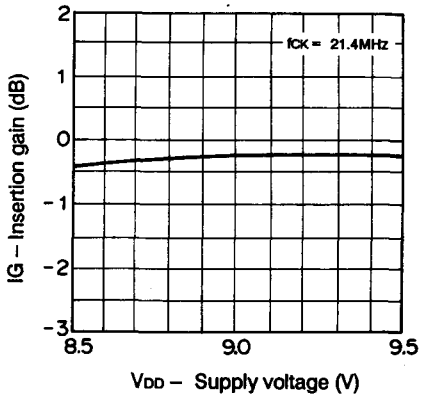
Differential gain vs. Clock frequency



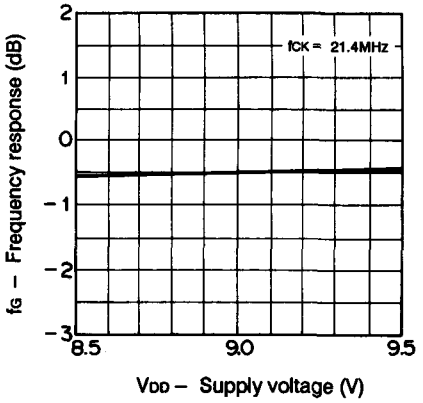
Gate voltage vs. Clock frequency



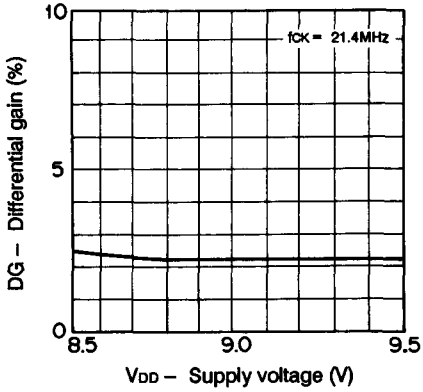
Insertion gain vs. Supply voltage



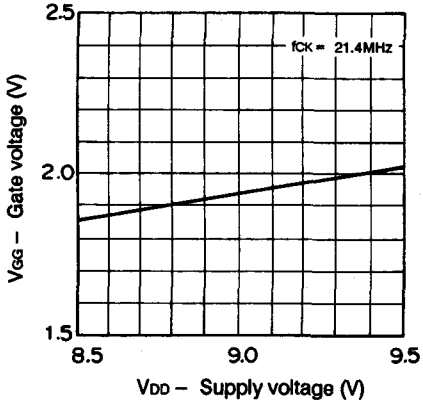
Frequency response vs. Supply voltage



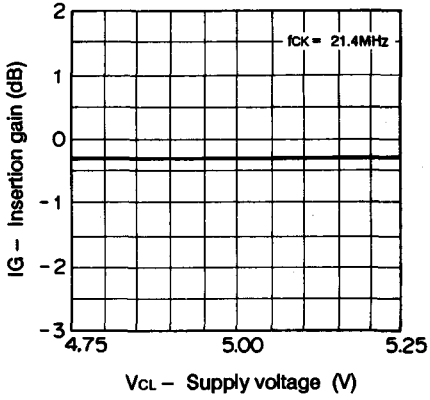
Differential gain vs. Supply voltage



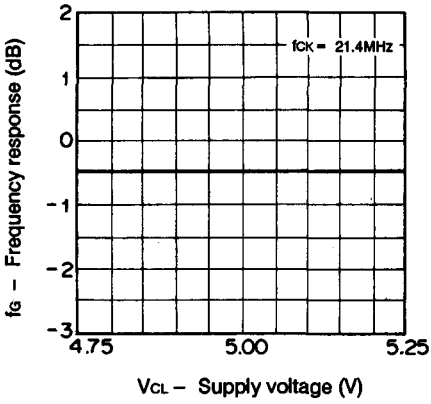
Gate voltage vs. Supply voltage



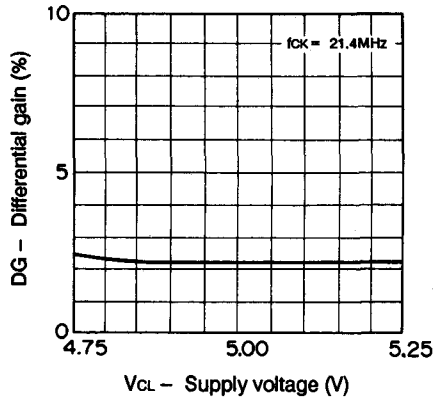
Insertion gain vs. Supply voltage



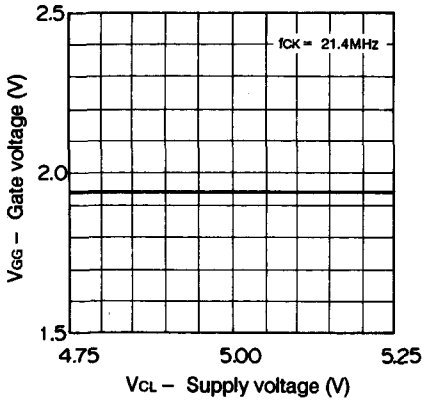
Frequency response vs. Supply voltage



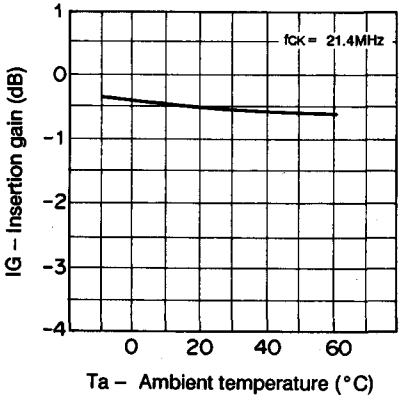
Differential gain vs. Supply voltage



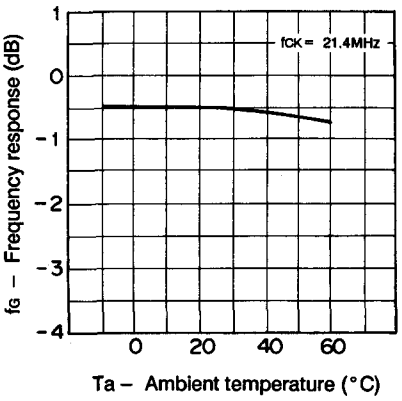
Gate voltage vs. Supply voltage



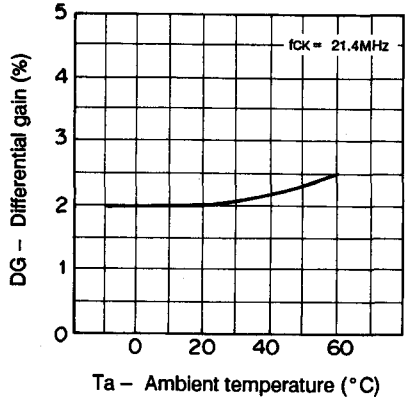
Insert gain vs. Ambient temperature



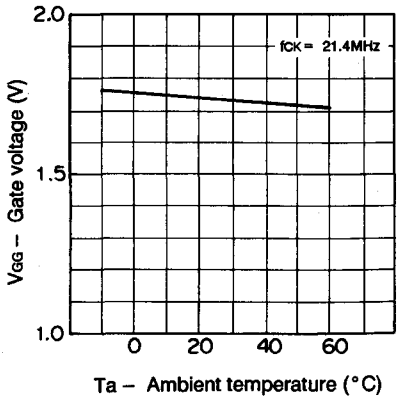
Frequency response vs. Ambient temperature



Differential gain vs. Ambient temperature



Gate voltage vs. Ambient temperature



SONY

CXL1008P/M

CMOS-CCD Signal Processor for Skew Compensation

Description

CXL1008P/M are CMOS-CCD signal processors developed for the varying-speed video signal for home-use 8 mm VTRs.

Features

- Low power consumption 105 mW (Typ.)
- Built-in peripheral circuit
- Adjustment is necessary for one part.

Functions

- 1/2H 359-bit, direct 20-bit CCD register
- Clock driver
- Timing oscillation circuit
- Automatic bias circuit
- Sink chip clamp circuit
- Dummy VD insert circuit
- Sample hold circuit

Structure

CMOS-CCD

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	11	V
	V_{CL}	6	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	CXL1008P 1000	mW
		CXL1008M 500	mW

Recommended Operating Conditions

• Supply voltage	V_{DD}	9V±5	%
	V_{CL}	5V±5	%

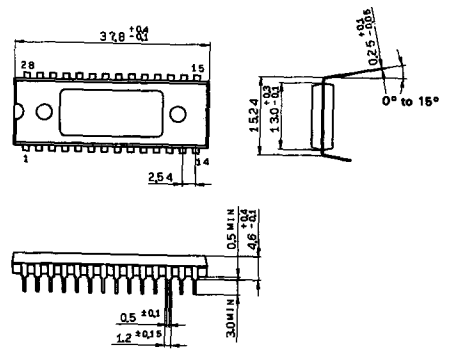
Recommended Clock Conditions

• Clock input amplitude	V_{CLK}	0.15 to 1.0 (0.3 Typ.)	Vp-p
• Clock frequency	f_{CLK}	10.738635	MHz

Package Outline

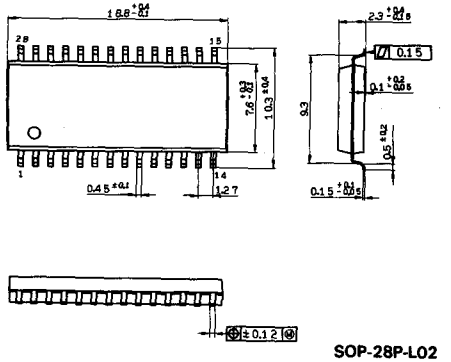
Unit: mm

CXL1008P 28 pin DIP (Plastic)



DIP-28P-03

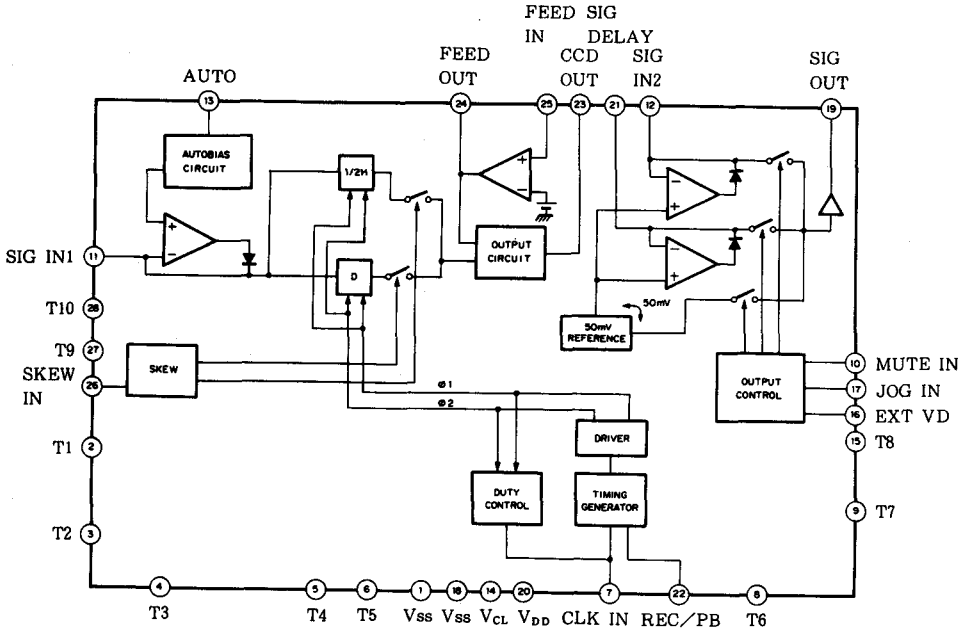
CXL1008M 28 pin SOP (Plastic)



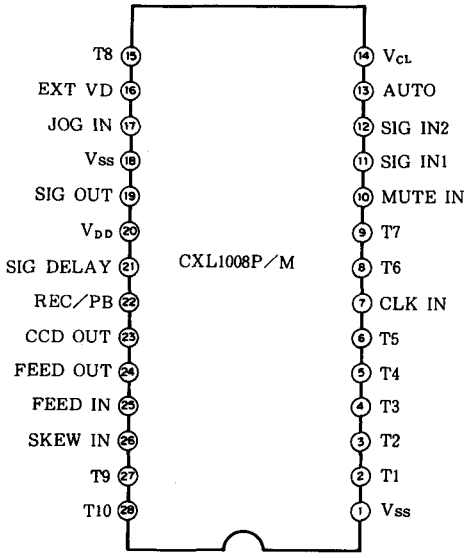
SOP-28P-L02

*60924 – ST

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Condition	Description	Impedance (Ω)
1	Vss			GND	
7	CLK IN	I	0.3Vp-p	Input the sinewave of 3 fsc (10.738635 MHz)	>50k
10	MUTE IN	I	5V when muting, normally 0V	The video signal mute is generated at High level. See the Logic Table of Signal Output Selection State (Table 1).	>100k
11	SIG IN1	I	1.1 Vp-p or less	Signal input pin of CCD DL Enter composite video signal.	>100k
12	SIG IN2	I	2.2 Vp-p or less	Signal input pin of the through side Enter composite video signal.	>100k
13	AUTO	O		The DC level of automatic bias is output.	10k
14	V_{CL}		+5V	Power supply 1	
16	EXT VD	I	When VD is inserted, 5V	Use this pin when VD is inserted to the video signal in the external dummy VD signal input.	>100k
17	JOG IN	I	JOG mode 5V PB/REC mode 0V	JOG/NORMAL PB selection pin See the Logic Table of Signal Output Selection State (Table 1).	>100k
18	Vss			GND	
19	SIG OUT	O		Final output	0.6 to 1.5k
20	V_{DD}		+9V	Power supply 2	
21	SIG DELAY	I		After the output from pin 23 CCD OUT passes through LPF, input it to the same pin and insert clamp and VD.	>100k
22	REC/PB	I	5V when PB 0V when REC	Operate the clock at High when PB. Stop the clock at Low when REC.	>100k
23	CCD OUT	O		Direct output from CCD DL	0.6 to 1.5k
24	FEED OUT	O		Feedback DC output	10k
25	FEED IN	I		Smoothing capacitor connection pin of the bias commutation loop on the output circuit	>100k
26	SKEW IN	I		Select Direct DL and 1/2H DL signals when High and Low, respectively. See the CCD/DL mode selection logic table (Table 2).	>100k

Note) T1 through T10 test pins must be connected as shown in the example of the application circuit because of the IC internal circuit.

Precautions

Countermeasures for electrostatics are necessary because some pins have low electrostatic strength (particularly Pin 26: SKEW IN).

Electrical Characteristics

(See the Electrical Characteristics Test Circuit)

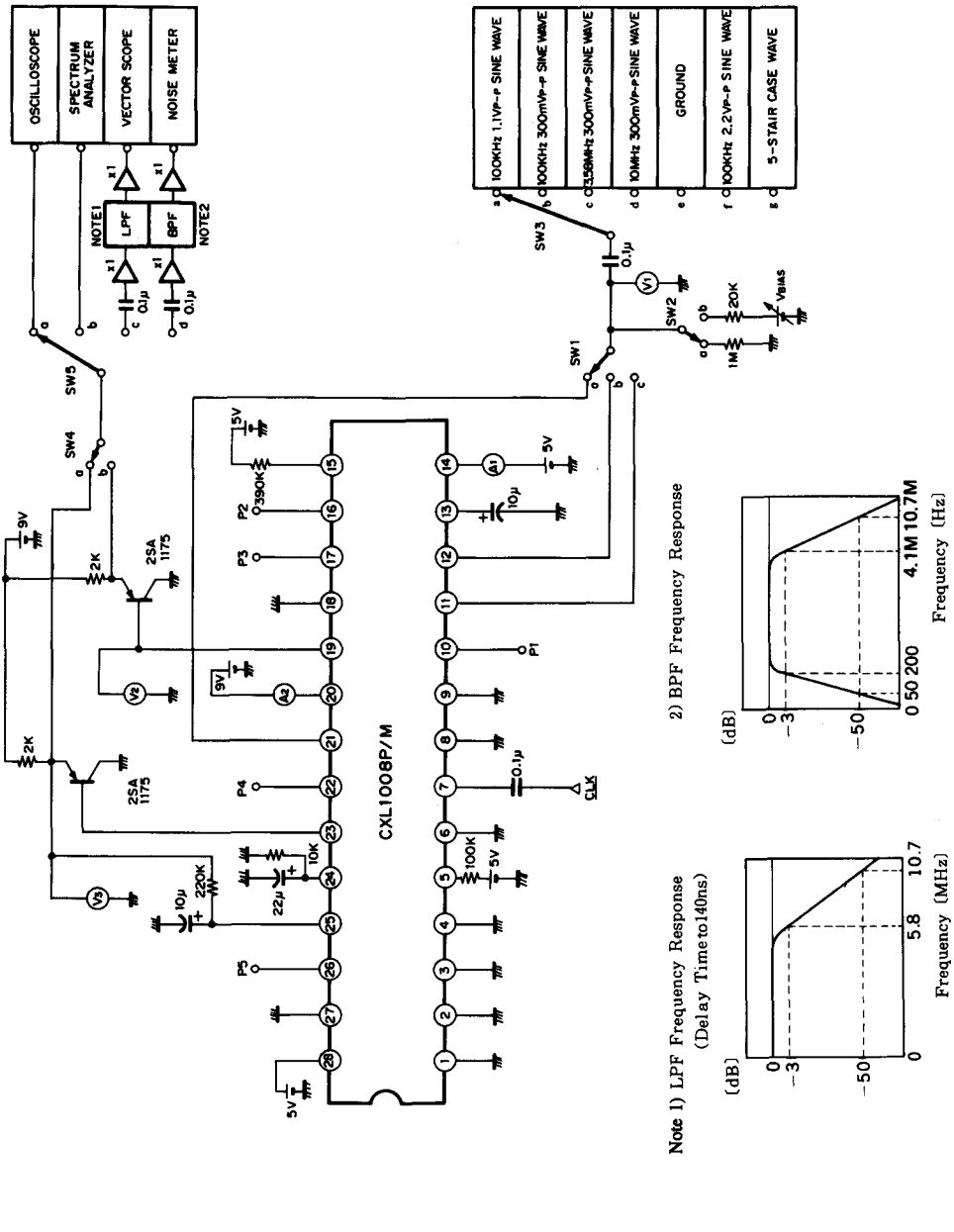
Ta = 25℃, V_{DD} = 9.0V, V_{CL} = 5.0V, f_{CLK} = 10.7MHz, V_{CLK} = 0.3Vp-p Sinewave

Items	Symbol	Test Conditions	Switch Conditions					Control Pin Conditions *1, *2					Min.	Typ.	Max.	Unit	Note
			1	2	3	4	5	P1	P2	P3	P4	P5					
Power current	I_{DD}	PB. JOG	c	a	a						H			7	12	mA	1
	I_{CL}		c	a	a						H			8	10	mA	1
Clock input level	CLK										H		0.15	0.3	1.0	V	
Signal input pin voltage	Vdi1		c	a	e						H		4.0	5.0	6.0	V	2
	Vdi2		b	a	e								4.0	4.2	4.4	V	2
	Vdi3		a	a	e								4.0	4.2	4.4	V	2
Signal output pin voltage	Vdo1		c	a	e						H		1.7	2.0	2.4	V	3
	Vdo2		b	a	e			L	L	L			1.5	2.0	2.5	V	3
CCD signal output voltage difference	Δ Dab	Direct↔1/2H	c	a	e	a	a				H	H↔L	−55	0	55	mV	4
Signal insert gain	IG_{CCD}		c	b	a	a	a				H		− 3.0	0	3.0	dB	5
	IG_{In2}		b	b	f	b	a	L	L	L			− 1.2	− 0.8	0	dB	5
	IG_{DL}		a	b	f	b	a	L	L	H			− 1.2	− 0.8	0	dB	5
CCD output signal gain difference	Δ Gab	Direct↔1/2H	c	b	a	a	a				H	H↔L	− 1.3	0	1.3	%	6
Frequency characteristics	f_{CCD}	3.58MHz/100kHz	c	b	b↔c	a	b				H		−3	−2	0	dB	7
	f_{In2}	10MHz/100kHz	b	b	b↔d	b	b	L	L	L			− 0.5	0	—	dB	8
	f_{DL}	10MHz/100kHz	a	b	b↔d	b	b	L	L	H			− 0.5	0	—	dB	8
Frequency characteristics difference	Δ fab	Direct↔1/2H at 3.58MHz	c	b	b↔c	a	b				H	H↔L	− 0.2	0	0.2	dB	9
Differential gain	DG_{CCD}	1.1 Vp-p input	c	b	g	a	c				H		0	3	10	%	10
	DG_{In2}	2.2 Vp-p input	b	b	g	b	c	L	L	L			0	2	4	%	10
	DG_{DL}	2.2 Vp-p input	a	b	g	b	c	L	L	H			0	2	4	%	10

Test Items	Symbol	Test Conditions	Switch Conditions					Control Pin Conditions *1, *2					Min.	Typ.	Max.	Unit	Note
			1	2	3	4	5	P1	P2	P3	P4	P5					
Differential phase	DP_{CCD}	1.1 Vp-p input	c	b	g	a	c				H		0	3	5	deg	10
	DP_{In2}	2.2 Vp-p input	b	b	g	b	c	L	L	L			0	3	5	deg	10
	DP_{DL}	2.2 Vp-p input	a	b	g	b	c	L	L	H			0	3	5	deg	10
Allowable input amplitude	V_{IN1-AC}		c		g								—	—	1.1	Vp-p	
	V_{IN2-AC}		a/b		g								—	—	2.2	Vp-p	
SN rate	S/N_{CCD}		c	b	a↔e	a	d				H		50	55	—	dB	11
	S/N_{In2}		b	b	f↔e	b	d	L	L	L			50	65	—	dB	11
	S/N_{DL}		a	b	f↔e	b	d	L	L	H			50	65	—	dB	11
VD insert depth	V_{VD}	2 Vp-p video signal from sink chip	a	a	g	b	a	L	⎍	H			0	50	100	mV	12
Logical input	$V_{IN\ H}$												4.0		—	V	
	$V_{IN\ L}$												—		1.0	V	

Note) •1. Control pins correspond to P1 through P5 of the Electrical Characteristics Test Circuit.
•2. Symbols "H" and "L" in control pin conditions represent "$V_{IN\ H}$" and "$V_{IN\ L}$" of logical input.

Electrical Characteristics Test Circuit



Note 1) LPF Frequency Response (Delay Time to 140ns)

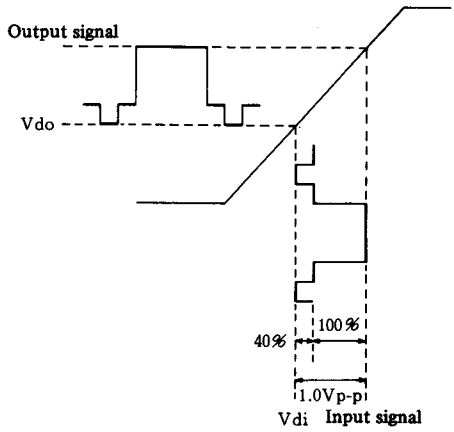
2) BPF Frequency Response

Note)

1. Current value when the clock is in operation in the PB or JOG mode.
   In the REC mode, the clock is stopped (Pin 22 is at low) to save power.

2. With the signal input pin voltage value, the video signal sync tip is clamped.

3. Vdo1 is a CCD OUT output voltage when the SIG IN1 input voltage is Vdi1
   Vdo2 is a SIG OUT output voltage when the SIG IN2 input voltage is Vdi2.
   Vdo1 and Vdo2 represent outputs for the sync tip clamp level when a white level signal is input as shown in the diagram.



4. ΔDab denotes an output voltage difference of CCD OUT when the direct DL and 1/2H DL are switched.

5. IG_{CCD} is a gain when a 1.1 Vp-p 100 kHz sinewave is input to SIG IN1.

$$IG_{CCD} = 20 \log \frac{\text{Output amplitude (Vp-p)}}{1.1\ \text{Vp-p}}$$

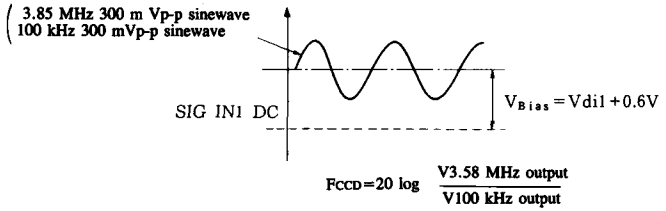
It is measured by giving a Vdi1 + 0.6 bias with V_{Bias}.
IGin2 and IG_{PL} are SIG OUT gains when 2.2 Vp-p 100 kHz sinewave is input to each of SIG IN2 and SIG DELAY pins.

$$IGin2 = 20 \log \frac{\text{Output amplitude (Vp-p)}}{2.2\ \text{Vp-p}}$$

It is measured by giving a Vdi2 + 1.1V bias with V_{Bias}.

6. ΔGab is a gain difference between the direct DL and 1/2H DL.

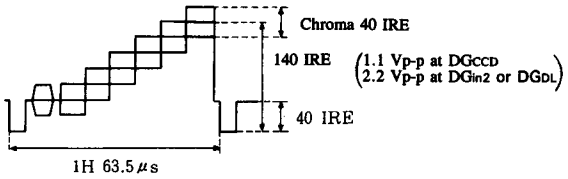
7. It represents a loss at 3.58 MHz compared with 100 kHz.
It is measured by raising the SIG IN1 input pin by 0.6V higher than the sync tip clamp level (Vdi1) with VBias.



8. It represents a loss at 10 MHz compared with 100 kHz.
It is measured by raising the SIG IN2 or SIG DELAY pin by 1.1V higher than the sync tip clamp level (Vdi2 or Vdi3) with VBias.

9. ΔFab is a frequency response difference between the direct DL and 1/2H DL.

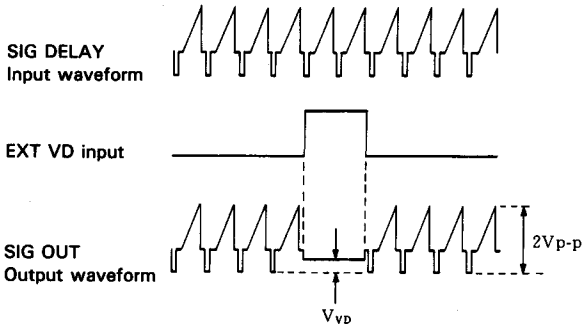
10.



DG is measured with a vectorscope in each mode of the 5-stage waves.

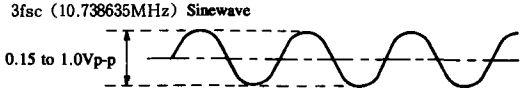
11. Measure S/N of the BPF 100 kHz to 4.2 MHz in the subcarrier trap mode with a video noise meter.

12.



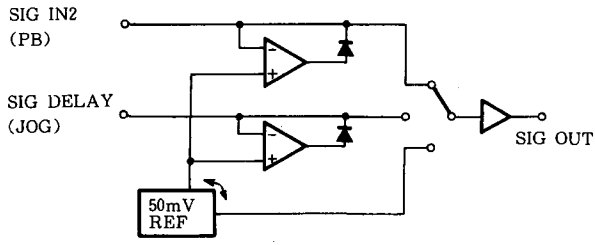
Set a voltage value at VVD when inserting EXT VD to the 2 Vp-p signal output waveform sync tip of SIG OUT.

CLOCK



Function Outline

Output signal selection



The video output signal is selected by selecting the output switch for three signals: Pin 10 (MUTE IN), Pin 17 (JOG IN) and Pin 16 (EXT VD).

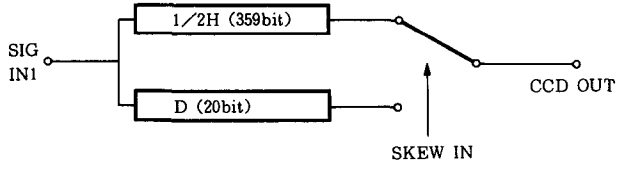
Logic Table of Signal Output Selection State

Input control signal state			Video signal output selection state			
JOG IN	MUTE IN	EXT VD	PB	JOG	VD insert	MUTE
0	0	0	○	×	×	×
0	0	1	○	×	×	×
0	1	0	×	×	×	○
0	1	1	×	×	×	○
1	0	0	×	○	×	×
1	0	1	×	×	○	×
1	1	0	×	×	×	○
1	1	1	×	×	○	○

Table 1

Note) 1. Figures "0" and "1" of the input control signal state are equivalent to "Low" and "High" of logic.
2. Items marked with the symbol "○" in the video signal output selection state are selected.
3. PB = $\overline{\text{JOG IN}}$. $\overline{\text{MUTE IN}}$
JOG = JOG IN . $\overline{\text{MUTE IN}}$. $\overline{\text{EXT VD}}$
VD insert = JOG IN . EXT VD
MUTE = MUTE IN

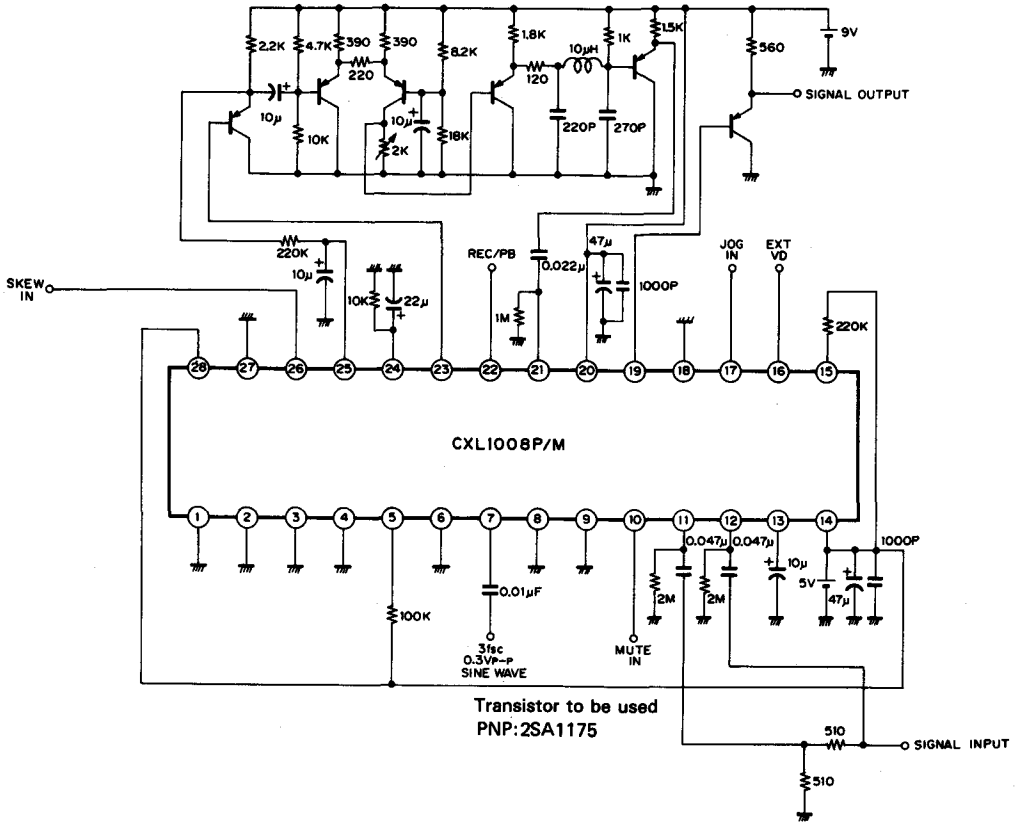
CCD selection



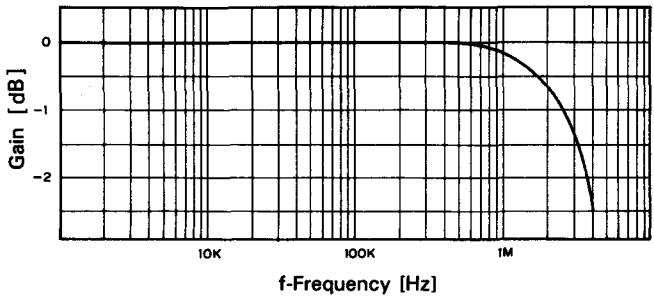
Logic Table of Signal Output Selection State

Control signal	CCD DL mode	
SKEW IN	D	1/2H
0	×	○
1	○	×

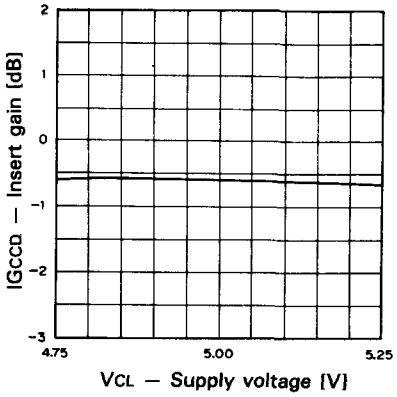
Table 2



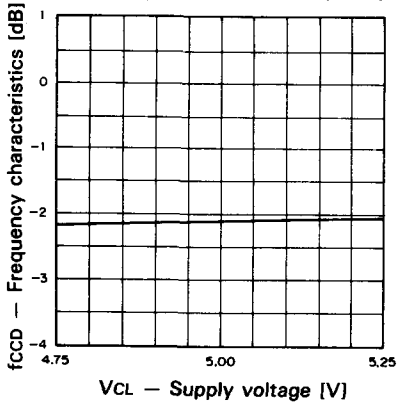
Frequency characteristics (Ta = 25°C)



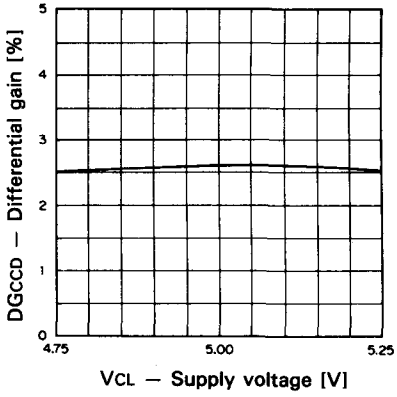
Supply voltage (V_{CL}) vs. Insert gain (IG_{CCD})



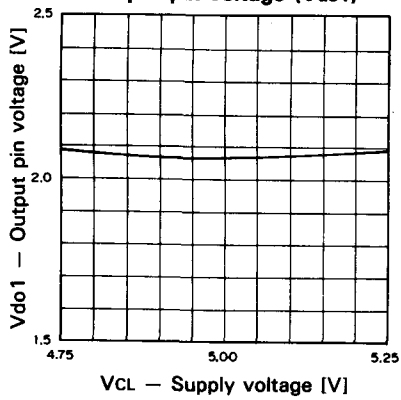
Supply voltage (V_{CL}) vs. Frequency characteristics (f_{CCD})



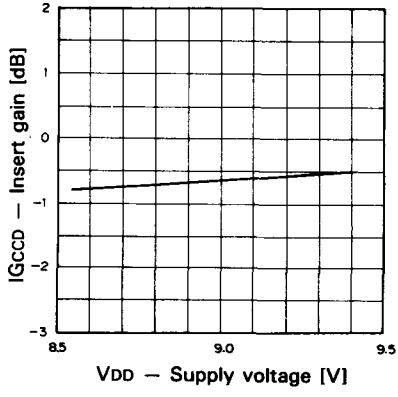
Supply voltage (V_{CL}) vs. Differential gain (DG_{CCD})



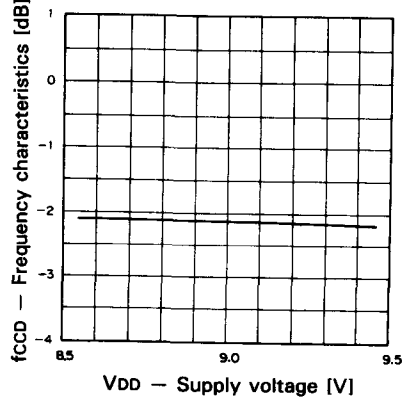
Supply voltage (V_{CL}) vs. Output pin voltage (V_{do1})



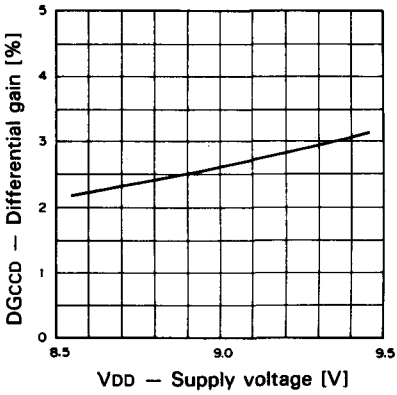
Supply voltage (V_{DD}) vs. Insert gain (IG_{CCD})



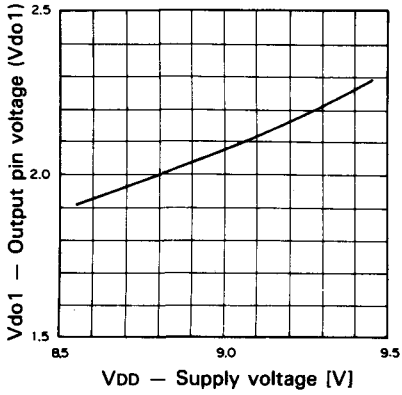
Supply voltage (V_{DD}) vs. Frequency characteristics (f_{CCD})



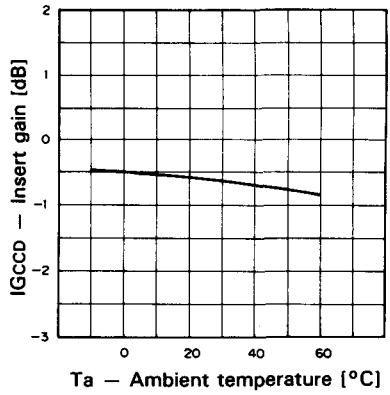
Supply voltage (V_{DD}) vs. Differential gain (DG_{CCD})



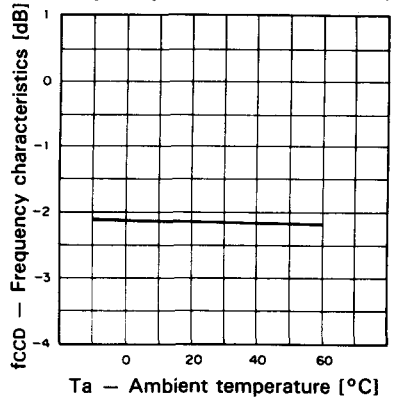
Supply voltage (V_{DD}) vs. Output pin voltage (Vdo1)



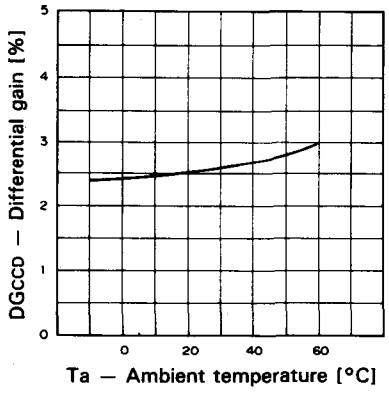
Ambient temperature (Ta) vs. Insert gain (IG_{CCD})



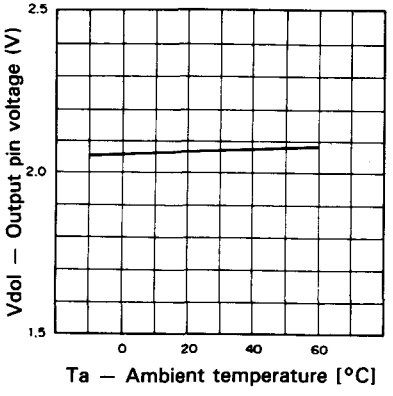
Ambient temperature (Ta) vs. Frequency characteristics (f_{CCD})



Ambient temperature (Ta) vs. Differential gain (DG_{CCD})



Ambient temperature (Ta) vs. Output pin voltage (f_{CCD})(Vdo1)



SONY®

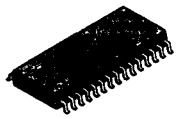
CXL1501M

CMOS-CCD Signal Processor

Description

CXL1501M is a CMOS-CCD signal processor designed for 8-mm VTR video signal processing. In combination with the 8-mm VTR video Y/C signal processing IC CXA1200BQ, this IC configures a comb filter for Y/C separation in recording an image and elimination of crosstalk in playing back.

30pin SOP (Plastic)



Features

- Single power supply 5V
- Low power consumption (225 mW Typ.)
- Built-in peripheral circuits
- Completely adjustment free
- Built-in quadruple progression PLL circuit
- For NTSC signals

Function

- 1-H comb filter output
- Dropout compensation (D.O.C) output
- Delay time matching through-output (THR)
- PLL circuit (quadruple progression)
- Clock driver
- Autobias circuit
- Sync tip clamp circuit
- Sample and hold circuit

Structure

CMOS-CCD

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}		6			V
• Operating temperature	Topr	-10	to	+60		°C
• Storage temperature	Tstg	-55	to	+150		°C
• Allowable power dissipation	P_D		500			mW

Recommended Operating Conditions (Ta=25°C)

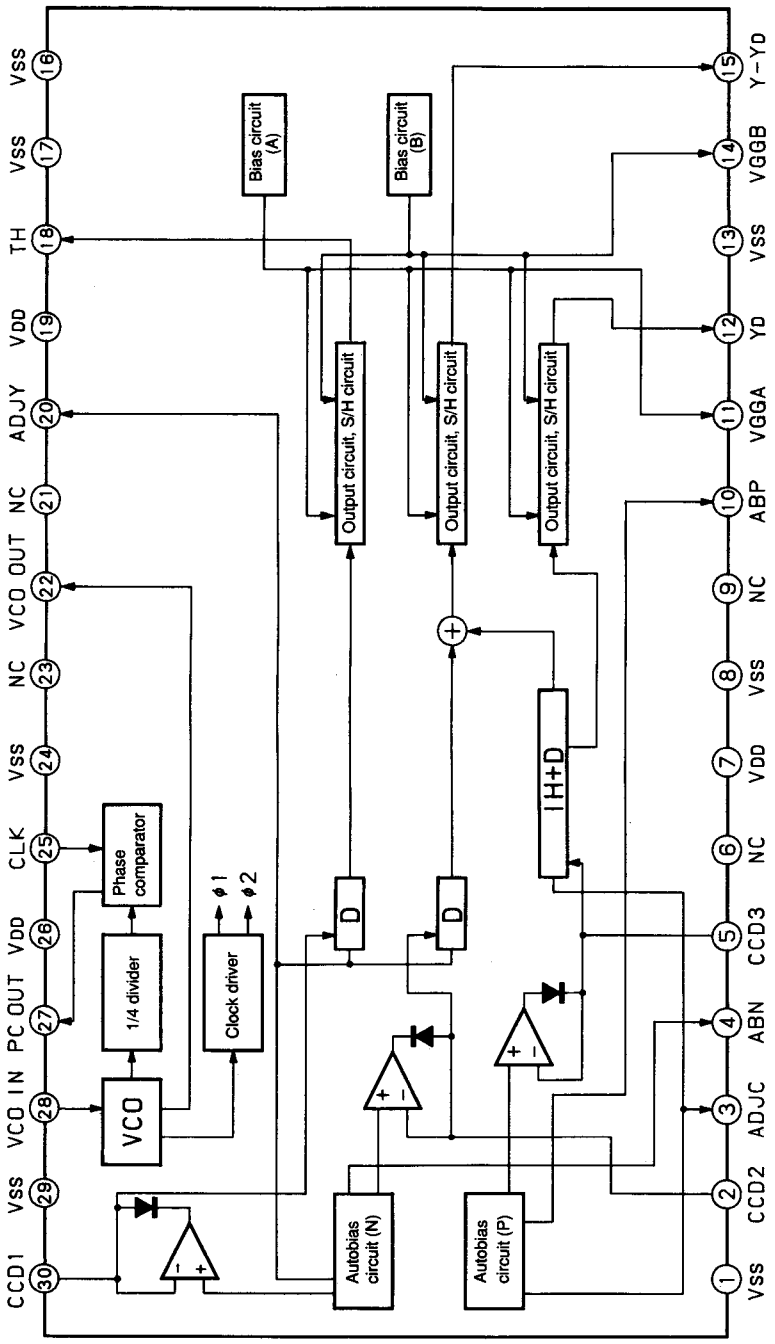
• Supply voltage	V_{DD}		5 ± 5%			V

Recommended Clock Conditions (Ta=25°C)

• Input clock amplitude	V_{CLK}	0.4	to	1.0	Vp-p	(0.5 Vp-p Typ.)
• Clock frequency	f_{CLK}		3.579545		MHz	
• Input clock waveform	sine wave					
• Input Signal Amplitude	V_{SIG}		571		mVp-p	(Max.)

81067A0X-YA

Block Diagram and Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description	Impedance [Ω]
1	Vss	–	GND	
2	CCD2	I	Signal input 2 (Reverse phase signal)	>100K (at no clamp)
3	ADJC	O	Positive CCD bias DC output	600 to 2K
4	ABN	O	Reverse autobias DC output	2K to 20K
5	CCD3	I	Signal input 3 (Positive phase signal)	>100K (at no clamp)
6	NC	–		
7	VDD	–	5V supply (For clock driver)	
8	Vss	–	GND	
9	NC	–		
10	ABP	O	Positive autobias DC output	2K to 20K
11	VGGA	O	Gate bias (A) DC output	2K to 10K
12	YD	O	D.O.C signal output (Reverse phase signal)	40 to 500
13	Vss	–	GND	
14	VGGB	O	Gate bias (B) DC output	2K to 10K
15	Y-YD	O	Comb filter signal output	40 to 500
16	Vss	–	GND	
17	Vss	–	GND	
18	TH	O	THR signal output (Positive phase signal)	40 to 500
19	VDD	–	5V supply (For analog)	
20	ADJY	O	Reverse phase CCD bias DC output	600 to 2K
21	NC	–		
22	VCO OUT	O	VCO output	
23	NC	–		
24	Vss	–	GND	
25	CLK	I	Clock input	4K to 40K
26	VDD	–	5V supply (For digital)	
27	PC OUT	O	Phase comparator output	2K to 5K
28	VCO IN	I	VCO input	>100K
29	Vss	–	GND	
30	CCD1	I	Signal input 1 (Reverse phase signal)	>100K (at no clamp)

Electrical Characteristics

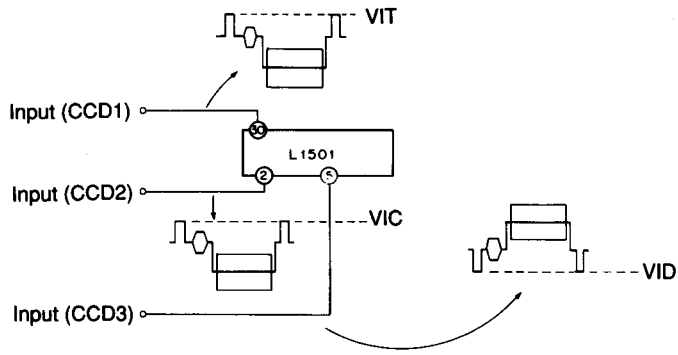
(Ta=25°C, V_{DD}=5V, f_{CLK}=3.579545MHz, V_{CLK}=500mVp-p sine wave)
See the Electrical Characteristics Test Circuit

Item	Symbol	Test condition*1	SW condition 1	2	3	4	5	6	7	8	9	Bias condition*2 (V) V_{BIAS} 1	V_{BIAS} 2	V_{BIAS} 3	Min.	Typ.	Max.	Unit	NOTE
Supply current	IDD		a	a	a	a	a	a	a	–	–	——	——	——	35	45	55	mA	*3
Low frequency gain	GLT	196.678kHz 500mVp-p Sine wave	a	a	a	a	a	a	a	a	b	——	——	——	-5.0	-3.0	-1.0	dB	*4
	GLC		a	a	a	a	a	a	a	b	b								
	GLD		a	a	a	a	a	a	a	c	b								
High frequency gain	GHT	3.579545 MHz 150mVp-p Sine wave	c	a	a	a	b	b	b	a	b	VIT-0.25	VIC-0.25	VID+0.25	-6.5	-4.5	-2.5	dB	*5
	GHC		c	a	a	a	b	b	b	b	b								
	GHD		c	a	a	a	b	b	b	c	b								
Frequency response	fT	196.678kHz ↔3.579545 MHz 150mVp-p Sine wave	b↔c	a	a	a	b	b	b	a	b	VIT-0.25	VIC-0.25	VID+0.25	-2.5	-1.5	-0.5	dB	*6
	fC		b↔c	a	a	a	b	b	b	b	b								
	fD		b↔c	a	a	a	b	b	b	c	b								
Differential gain	DGT	5-staircase wave*7	f	a	a	a	a	a	a	a	c	——	——	——	0	3	7	%	*7
	DGC		f	a	a	a	a	a	a	b	c								
	DGD		f	a	a	a	a	a	a	c	c								
Differential phase	DPT	5-staircase wave*7	f	a	a	a	a	a	a	a	c	——	——	——	0	3	7	degree	*7
	DPC		f	a	a	a	a	a	a	b	c								
	DPD		f	a	a	a	a	a	a	c	c								
S/H pulse coupling	VPT	No-signal input	–	b	b	b	b	b	b	a	a	VIT	VIC	VID+0.5	—	—	350	mVp-p	*8
	VPC		–	b	b	b	b	b	b	b	a								
	VPD		–	b	b	b	b	b	b	c	a								
SN ratio	SNT	No-signal input*9	–	b	b	b	a	a	a	a	d	——	——	——	—	-56	-52	dB	*9
	SNC		–	b	b	b	a	a	a	b	d								
	SND		–	b	b	b	a	a	a	c	d								
Chroma comb depth min. gain	C.CD	3.579545MHz 200mVp-p sine wave 3.587412 MHz 200mVp-p sine wave	d↔e	a	a	a	b	b	b	b	b	*10	*10	*10	—	—	-27	dB	*10

Note)

*1. Adjust the output amplitude of the inversion and the non inversion amplifiers in the signal input part of Fig. 1 to an equal value, as well as the phase difference to a precise 180°.
Also set the clock and input signal frequency accurately.

*2. VIT, VIC and VID are defined as follows:
VIT, VIC and VID are input signal clamp levels, clamping the Video signal sync tip level. They are the pin voltages at no-input signal for pins 30, 2 and 5, respectively.



Testing of VIT, VIC and VID is executed with a voltmeter under the following SW conditions:

Item	SW conditions											Test point
	1	2	3	4	5	6	7	8	9	10	11	
VIT	–	b	b	b	a	a	a	–	–	–	–	V1
VIC	–	b	b	b	a	a	a	–	–	–	–	V2
VID	–	b	b	b	a	a	a	–	–	–	–	V3

As VIT, VIC and VID differ with each IC, they are to be tested respectively.

*3. This is the IC supply current value during clock and signal input.

*4. GLT, GLC and GLD are output gains of pins TH, Y-YD and YD when a 500 mVp-p, 196.678 kHz sinewave is simultaneously fed to pins CCD1, CCD2 and CCD3, respectively.

(Example of calculation)

$$GLT = 20 \log \frac{\text{TH pin output voltage [mVp-p]}}{500\ [\text{mVp-p}]} \quad [\text{dB}]$$

*5. GHT, GHC and GHD are output gains of pins TH, Y-YD and YD when a 150 mVp-p, 3.579545 MHz sinewave is simultaneously fed to pins CCD1, CCD2 and CCD3 respectively.
Bias at input ($V_{BIAS}1$, $V_{BIAS}2$ and $V_{BIAS}3$) is tested respectively at YIT + 0.25V, VIC -0.25V and VID + 0.25V.

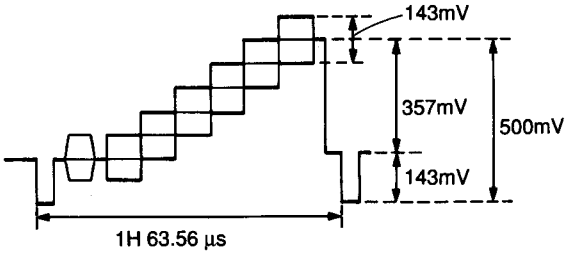
(Example of calculation)

$$GHT = 20 \log \frac{\text{TH pin output voltage [mVp-p]}}{\text{150 [mVp-p]}} \text{ [dB]}$$

*6. Indicates the dissipation at 3.579545 MHz in relation to 196.678 kHz. From the output voltage at pins TH, Y-YD and YD when a 150 mVp-p, 196.678 kHz sinewave is simultaneously fed to pins CCD1, CCD2 and CCD3, and from the output voltage at pins TH, Y-YD and YD when a 150 mVp-p, 3.579545MHz sinewave is simultaneously fed to same, calculation is made according to the following formula. The input part bias for $V_{BIAS}1$, $V_{BIAS}2$ and $V_{BIAS}3$ is tested at VIT-0.25V, VIC-0.25V and VID+0.25V, respectively.

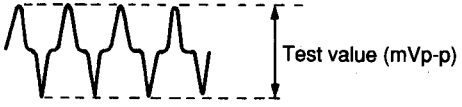
$$fT = 20 \log \frac{\text{TH pin output voltage (3.579545 MHz) [mVp-p]}}{\text{TH pin output voltage 196.678 kHz) [mVp-p]}} \text{ [dB]}$$

*7. The differential gain (DG) and the differential phase (DP), when the 5-staircase wave in the following figure is fed, are tested with a vector scope:



CCD3 pin input waveform (the input waveform to pins CCD1 and CCD2 is the inverted waveform of the figure above.)

*8. The internal clock component to the output signal during no-signal input and the leakage of that high harmonic component are tested. The input part bias is tested at VITv, VICv and VID + 0.5v.



*9. The noise level of output signal at no-input signal is tested with a video noise meter in the Sub Carrier Trap mode at BPF 100 kHz to 4 MHz. Vn [Vrms]

The signal component is determined either by testing the output voltage (the same test system as that of noise level) at input of 357 mVp-p, 196.678 kHz, or by performing calculation from the values of GLT, GLC and GLD in accordance with the following formula. Vs [Vp-p]

(Example of calculation of Vs)

$$Vs\text{-}t = 0.357 \times 10^{\frac{GLT}{20}}$$ (Vs-T: TH output voltage)

(Example of calculation of S/N ratio)

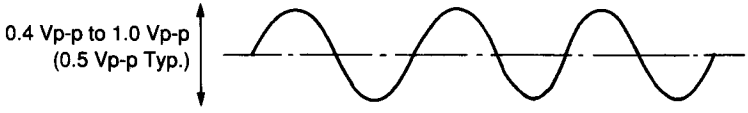
$$SNT = 20 \log \frac{Vn\text{-}T \text{ (noise component) [Vrms]}}{Vs\text{-}T \text{ (signal component) [Vp-p]}} \text{ [dB]}$$

*10. C-CD is calculated in accordance with the following formula from the Y-YD pin output voltage when a 200 mVp-p, 3.579545 MHz sinewave is simultaneously fed to pins CCD1, CCD2 and CCD3 and from the C-CD pin output voltage when a 200 mVp-p, 3.587412 MHz sinewave is simultaneously fed to same. The input part bias is set to VIT-0.30V, VIC-0.30V and VID+0.30V

$$C\text{-}CD = 20 \log \frac{\text{Y-YD pin output voltage (3.587412 MHz)}}{\text{Y-YD pin output voltage (3.579545 MHz)}} \text{ [dB]}$$

CLOCK

fsc (3.579545 MHz) sine wave



Electrical Characteristics Test Circuit

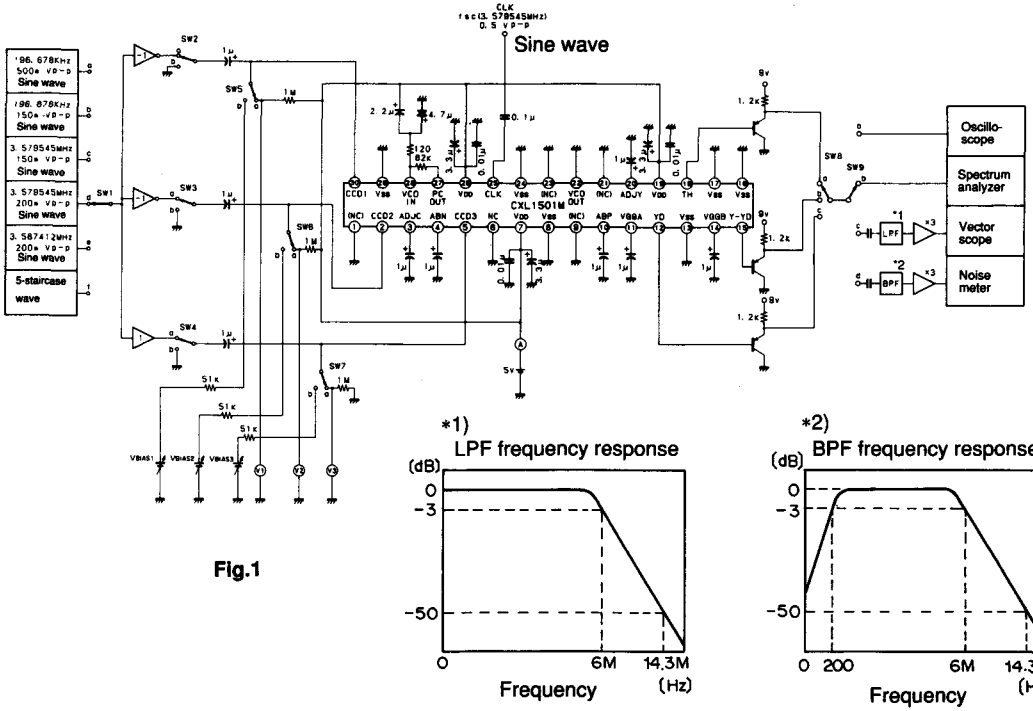
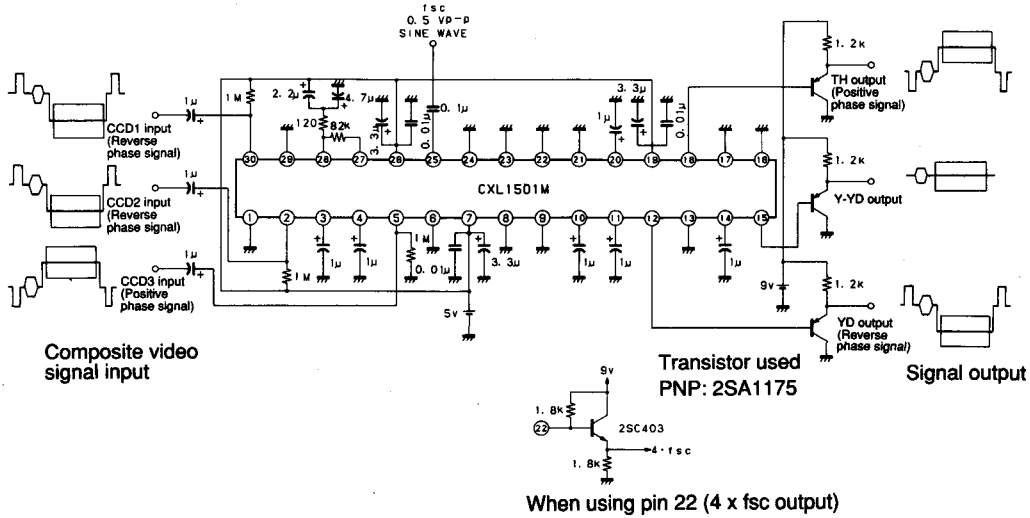
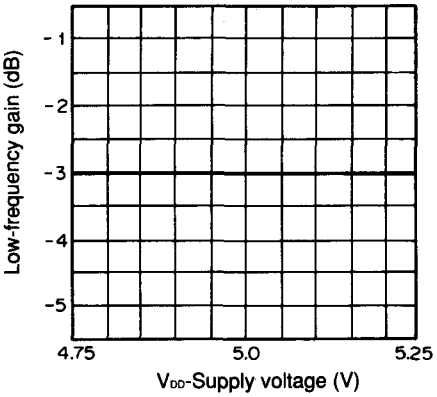


Fig.1

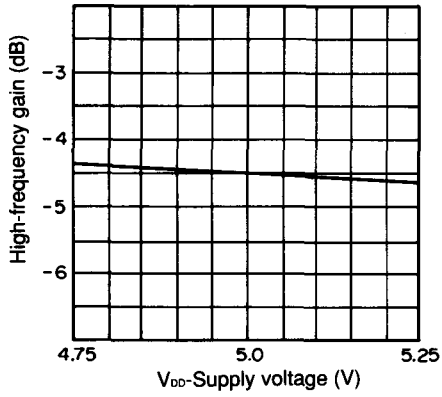
Application Circuit



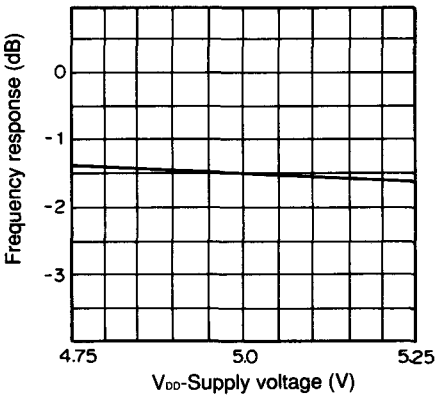
Low-frequency gain vs. Supply voltage



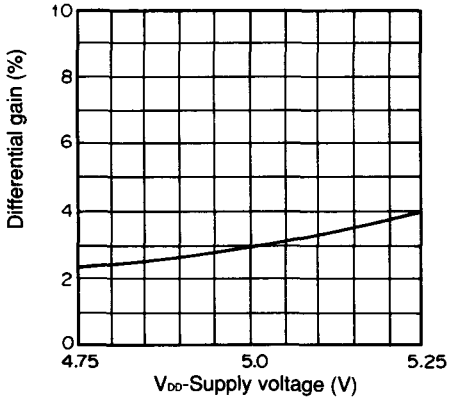
High-frequency gain vs. Supply voltage



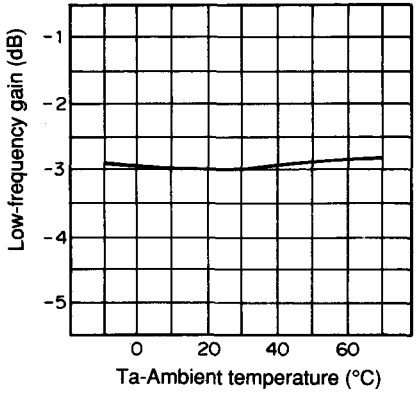
Frequency response vs. Supply voltage



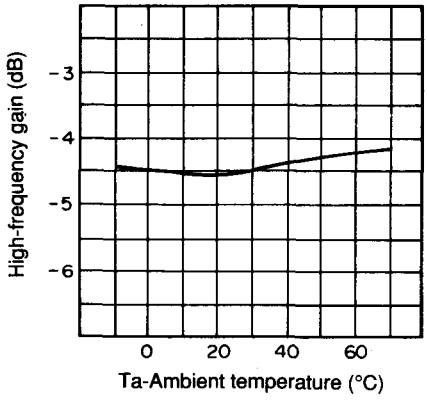
Differential gain vs. Supply voltage



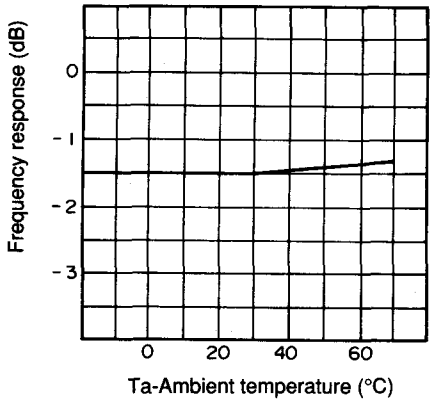
Low-frequency gain vs. Ambient temperature



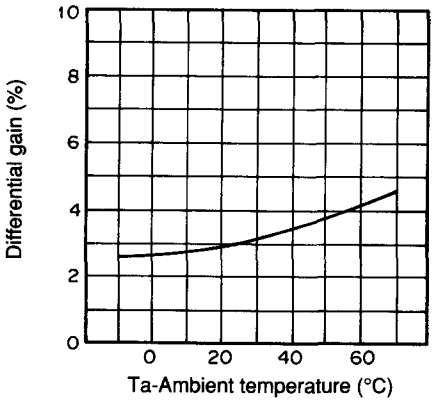
High-frequency gain vs. Ambient temperature



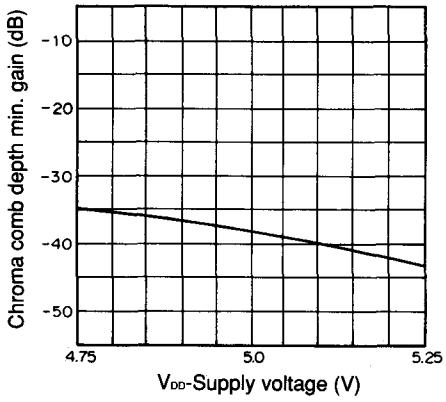
Frequency response vs. Ambient temperature



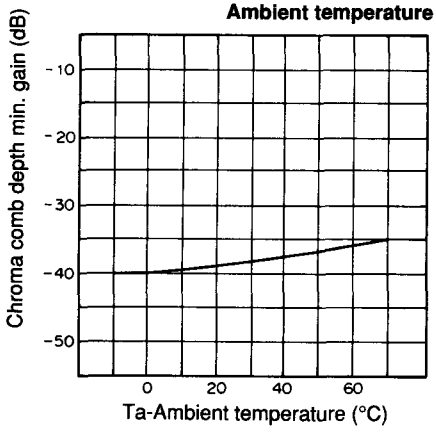
Differential gain vs. Ambient temperature



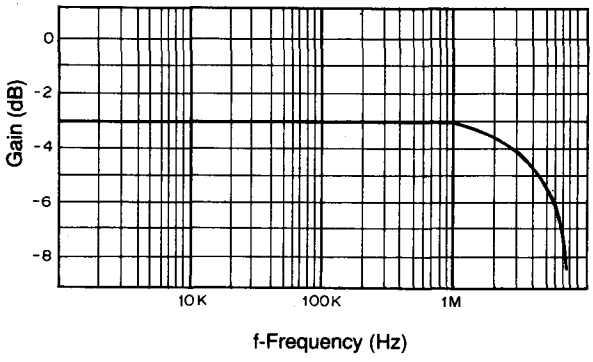
Chroma comb depth min. gain vs. Supply voltage



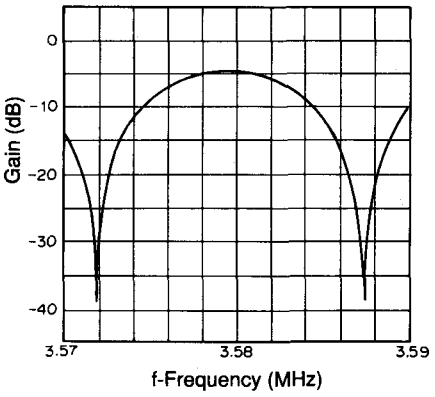
Chroma comb depth min. gain vs. Ambient temperature



Frequency response (TH, YD Output)

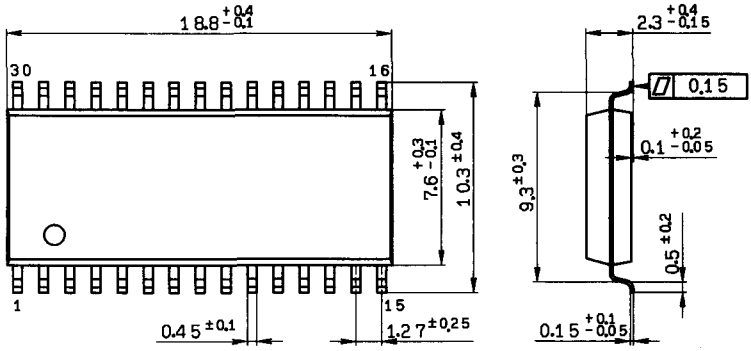


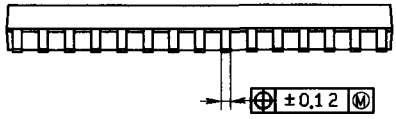
Chroma comb response (Y-YD Output)



Package Outline Unit: mm

30pin SOP (Plastic) 375mil 0.7g





SONY NAME	SOP-30P-L01
EIAJ NAME	*SOP030-P-0375-A
JEDEC CODE	———

SONY

CXL1502M

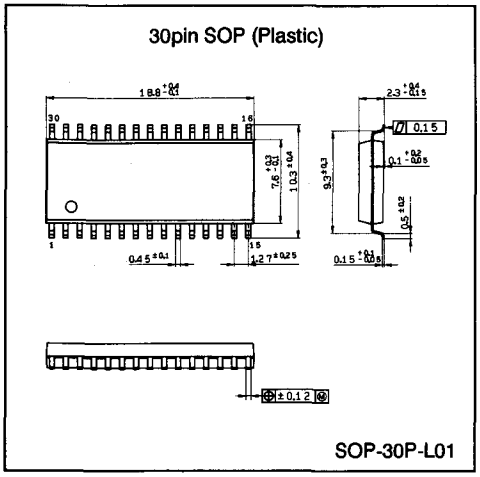
CMOS-CCD Signal Processor

Description

CXL1502M is a CMOS-CCD signal processor designed for 8-mm video signal processing. In combination with the 8-mm video Y/C signal processing IC CXA1200Q, this IC configures a comb filter for Y/C separation in recording an image, elimination of line crawling and crosstalk in playing back.

Package Outline

Unit: mm



Features

- Single power supply 5V
- Low power consumption
- Built-in peripheral circuits
- Completely adjustment free
- Built-in triple progression PLL circuit
- For PAL signals

Function

- 1-H comb filter, 2-H comb filter output
- Dropout compensation
- PLL circuit (triple progression)
- Clock driver
- Autobias circuit
- Sync tip clamp circuit
- Sample and hold circuit
- Delay time matching through-output (THR)

Structure

CMOS-CCD

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}		6			V
• Operating temperature	Topr	−10	to	+60		°C
• Storage temperature	Tstg	−55	to	+150		°C
• Allowable power dissipation	P_D		500			mW

Recommended Operating Conditions (Ta = 25°C)

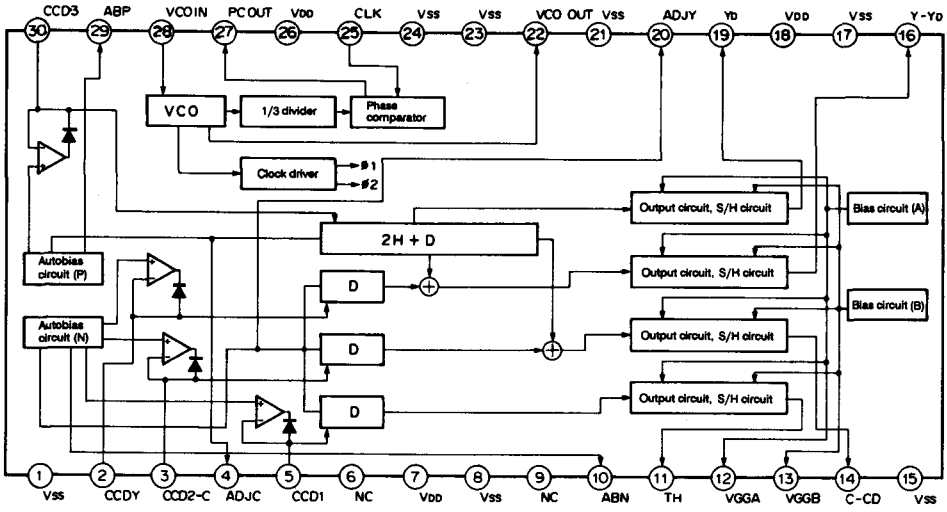
• Supply voltage	V_{DD}		5 ± 5%			V

Recommended Clock Conditions (Ta = 25°C)

• Input clock amplitude	V_{CLK}	0.3	to	1.0	Vp-p	(0.4 Vp-p Typ.)
• Clock frequency	f_{CLK}		4.433619		MHz	
• Input clock waveform	sine wave					
• Input Signal Amplitude	V_{SIG}		575		mVp-p	(Max.)

80334A-YA

Block Diagram



Pin Description

No.	Symbol	I/O	Description	Impedance (Ω)
1	Vss	–	GND	
2	CCDY	I	Signal input 4 (Reverse phase signal)	>100k (at no clamp)
3	CCD2-C	I	Signal input 2 (Reverse phase signal)	>100k (at no clamp)
4	ADJC	O	Positive CCD bias DC output	600 to 2k
5	CCD1	I	Signal input 1 (Reverse phase signal)	>100k (at no clamp)
6	NC	–		
7	VDD	–	5V supply	
8	Vss	–	GND	
9	NC	–		
10	ABN	O	Reverse autobias DC output	2k to 200k
11	TH	O	THR signal output (Positive phase signal)	40 to 500
12	VGGA	O	Gate bias (A) DC output	2k to 10k
13	VGGB	O	Gate bias (B) DC output	2k to 10k
14	C-CD	O	2H comb filter signal output	40 to 500
15	Vss	–	GND	
16	Y-YD	O	1H comb filter signal output	40 to 500
17	Vss	–	GND	
18	VDD	–	5V supply	
19	YD	O	DOC signal output (Reverse phase signal)	40 to 500
20	ADJY	O	Reverse phase CCD bias DC output	600 to 2k
21	Vss	–	GND	
22	VCO OUT	O	VCO output	
23	Vss	–	GND	
24	Vss	–	GND	
25	CLK	I	Clock input	4k to 40k
26	VDD	–	5V supply	
27	PC OUT	O	Phase comparator	2k to 5k
28	VCO IN	I	VCO input	>100k
29	ABP	O	Positive autobias DC output	2k to 200k
30	CCD3	I	Signal input 3 (Positive phase signal)	>100k (at no clamp)

Electrical Characteristics

(See the Electrical Characteristics Test Circuits)

Ta = 25°C, V_{DD} = 5V, f_{CLK} = 4,433619MHz, V_{CLK} = 400mVpp

Item	Symbol	Test conditions	SW conditions 1	2	3	4	5	6	7	8	9	10	11	Bias conditions (Note 1) V BIAS 1	V BIAS 2	V BIAS 3	V BIAS 4	Min.	Typ.	Max.	Unit	Note
Supply current	IDD	–	a	a	a	a	a	a	a	a	a	-	-	–	–	–	–	50	60	70	mA	2
Low frequency gain	GLC	Vin: 203.126 KHz 500mVpp	a	a	a	a	a	a	a	a	a	c	b	–	–	–	–	-5.0	-3.0	-1.0	dB	3
	GLY		a	a	a	a	a	a	a	a	a	b	b									
	GLD		a	a	a	a	a	a	a	a	a	a	b									
	GLT		a	a	a	a	a	a	a	a	a	d	b									
High frequency gain	GHC	Vin: 4.437525 MHz 150mVpp	c	a	a	a	a	b	b	b	b	c	b	VID +0.25	VIY −0.25	VIC −0.25	VIT −0.25	-7.0	-5.0	-3.0	dB	4
	GHY		c	a	a	a	a	b	b	b	b	b	b									
	GHD		c	a	a	a	a	b	b	b	b	a	b									
	GHT		c	a	a	a	a	b	b	b	b	d	b									
Frequency response	fc	Vin: 150mVpp 203.126KHz / 4.437525MHz	b/c	a	a	a	a	b	b	b	b	c	b	VID +0.25	VIY −0.25	VIC −0.25	VIT −0.25	-3.0	-2.0	-1.0	dB	5
	fY		b/c	a	a	a	a	b	b	b	b	b	b									
	fD		b/c	a	a	a	a	b	b	b	b	a	b									
	fT		b/c	a	a	a	a	b	b	b	b	d	b									
Differential gain	DGC	Vin: 5-staircase wave	h	a	a	a	a	a	a	a	a	c	c	–	–	–	–	0	3	7	deg	6
	DGY		h	a	a	a	a	a	a	a	a	b	c									
	DGD		h	a	a	a	a	a	a	a	a	a	c									
	DGT		h	a	a	a	a	a	a	a	a	d	c									
Differential phase	DPC	Vin: 5-staircase wave	h	a	a	a	a	a	a	a	a	c	c	–	–	–	–	0	3	7	deg	6
	DPY		h	a	a	a	a	a	a	a	a	b	c									
	DPD		h	a	a	a	a	a	a	a	a	a	c									
	DPT		h	a	a	a	a	a	a	a	a	d	c									
SN ratio	SNC	No-signal input	-	b	b	b	b	a	a	a	a	c	d	–	–	–	–	–	-56	-52	deg	7
	SNY		-	b	b	b	b	a	a	a	a	b	d									
	SND		-	b	b	b	b	a	a	a	a	a	d									
	SNT		-	b	b	b	b	a	a	a	a	d	d									
S/H pulse coupling	VPC	No-signal input	-	b	b	b	b	b	a	a	a	c	a	VID +0.5	–	–	–	–	–	350	mVpp	8
	VPY		-	b	b	b	b	b	a	a	a	b	a									
	VPD		-	b	b	b	b	b	a	a	a	a	a									
	VPT		-	b	b	b	b	b	a	a	a	d	a									
Chroma comb depth min. gain	CCD	Vin: 200mVpp 4.437525MHz/ 4.441432MHz	d/e	a	a	a	a	b	b	b	b	c	b	VID +0.3	VIY −0.3	VIC −0.3	VIT −0.3	–	–	-24	dB	9
Y-comb depth min. gain	YCD	Vin: 200mVpp 2.000011MHz/ 1.992198MHz	f/g	a	a	a	a	b	b	b	b	b	b	VID +0.3	VIY −0.3	VIC −0.3	VIT −0.3	–	–	-15	dB	10

Electrical Characteristics Test Circuit

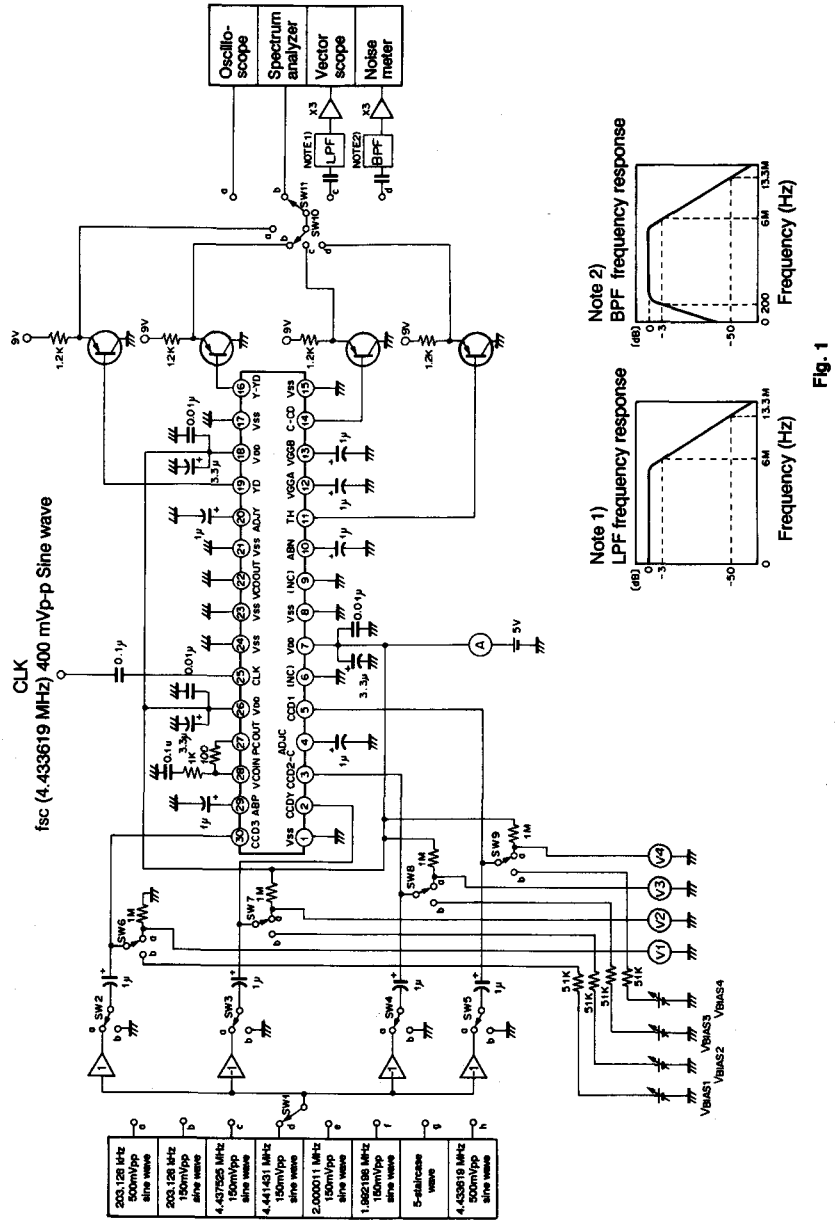
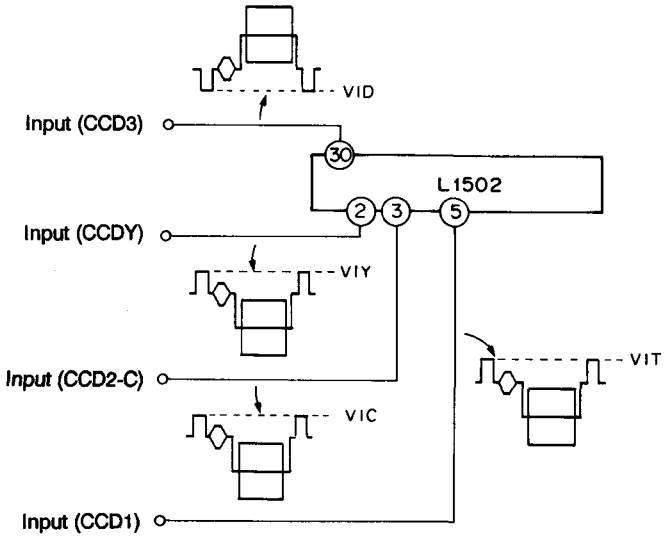


Fig. 1

Note)

1. VIC, VIY, VID and VIT are defined as follows:
   VIC, VIY, VID and VIT are input signal clamp levels, clamping the Video signal sync tip level. They are the pin voltages at no-input signal for pins 3, 2, 30 and 5, respectively.



Testing of VIC, VIY, VID and VIT is executed with a voltmeter under the following SW conditions:

Item	SW conditions											Test point
	1	2	3	4	5	6	7	8	9	10	11	
VIC	–	b	b	b	b	a	a	a	a	–	–	V3
VIY	–	b	b	b	b	a	a	a	a	–	–	V2
VID	–	b	b	b	b	a	a	a	a	–	–	V1
VIT	–	b	b	b	b	a	a	a	a	–	–	V4

2. This is the IC supply current value during clock and signal input.

3. GLC, GLY, GLD and GLT are output gains of pins C-CD, Y-YD, YD and TH when a 500 mVp-p, 203.126 kHz sinewave is simultaneously fed to pins CCD2-C, CCDY, CCD3 and CCD1, respectively.

   (Example of calculation)

$$GLC = 20 \log \frac{\text{C-CD pin output voltage [mVp-p]}}{500 \text{ [mVp-p]}} \text{ [dB]}$$

4. GHC, GHY, GHD and GHT are output gains of pins C-CD, Y-YD, YD and TH when a 150 mVp-p, 4.437525 MHz sinewave is simultaneously fed to pins CCD2-C, CCDY, CCD3 and CCD1, respectively. Bias at input ($V_{BIAS}1$, $V_{BIAS}2$, $V_{BIAS}3$ and $V_{BIAS}4$) is tested respectively at VID + 0.25V, VIY – 0.25V, VIC – 0.25V and VIT – 0.25V.

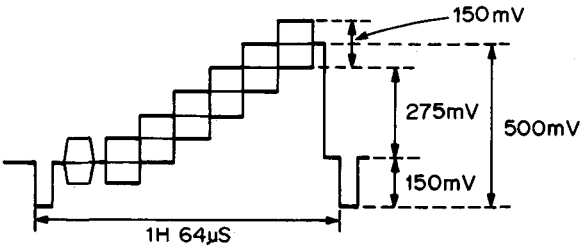
   (Example of calculation)

$$GHC = 20 \log \frac{\text{C-CD pin output voltage [mVp-p]}}{150 \text{ [mVp-p]}} \text{ [dB]}$$

5. Indicates the dissipation at 4.4357525 MHz in relation to 203.126 kHz. From the output voltage at pins TH, C-CD, Y-YD and YD when a 150 mVp-p, 203.126 kHz sinewave is simultaneously fed to pins CCD1, CCD2-C, CCDY and CCD3, and from the output voltage at pins TH, C-CD, Y-YD and YD when a 150 mVp-p, 4.437525 MHz sinewave is simultaneously fed to same, calculation is made according to the following formula. The input part bias for $V_{BIAS}1$, $V_{BIAS}2$, $V_{BIAS}3$ and $V_{BIAS}4$ is tested at VID + 0.25V, VIY – 0.25V, VIY – 0.25V, VIC – 0.25V and VIT – 0.25V, respectively.

$$fT = 20 \log \frac{\text{TH pin output voltage (4.437525 MHz) [mVp-p]}}{\text{TH pin output voltage (203.126kHz) [mVp-p]}} \text{ [dB]}$$

6. The differential gain (DG) and the differential phase (DP), when the 5-staircase wave in the following figure is fed, are tested with a vector scope:



   CCD3 pin input waveform (the input waveform to pins CCD1, CCD2-C and CCDY is the inverted waveform of the figure above.)

7. The noise level of output signal at no-input signal is tested with a video noise meter in the Sub Carrier Trap mode at BPF 100 kHz to 5 MHz. Vn [Vrms]

   The signal component is determined either by testing the outpt voltage (the same test system as that of noise level) at input of 350 mVp-p, 203.126 KHz, or by performing calculation from the values of GLT, GLC, GLY and GLD in accordance with the following formula. Vs [Vp-p]

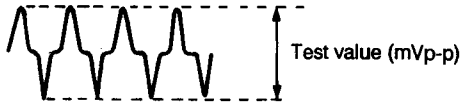
   (Example of calculation of Vs)

$$V_{S\text{-}T} = 0.35 \times 10^{\frac{GLT}{20}}$$ ($V_{S\text{-}T}$: TH output voltage)

   (Example of calculation of S/N ratio)

$$SNT = 20 \log \frac{V_{N\text{-}T} \text{ (noise component) [Vrms]}}{V_{S\text{-}T} \text{ (signal component) [Vp-p]}} \text{ [dB]}$$

8. The internal clock component to the output signal during no-signal input and the leakage of that high harmonic component are tested. The input part bias for V_{BIAS1} is tested at VID + 0.5v.

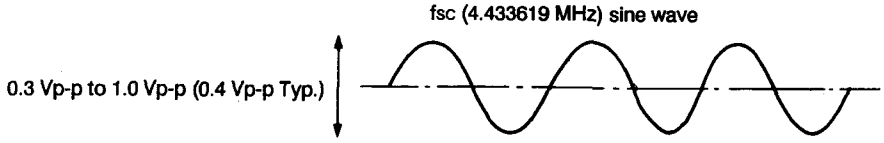


9. CCD is calculated in accordance with the following formula from the C-CD pin output voltage when a 200 mVp-p, 4.437525 MHz sinewave is simultaneously fed to pins CCD1, CCD2-C, CCDY and CCD3 and from the C-CD pin output voltage when a 200 mVp-p, 4.441431 MHz sinewave is simultaneously fed to same. The input part bias for V_{BIAS1}, V_{BIAS2}, V_{BIAS3} and V_{BIAS4} is set to V_{ID} + 0.3V, VIY − 0.3V, VIC − 0.3V and VIT − 0.3V, respectively.

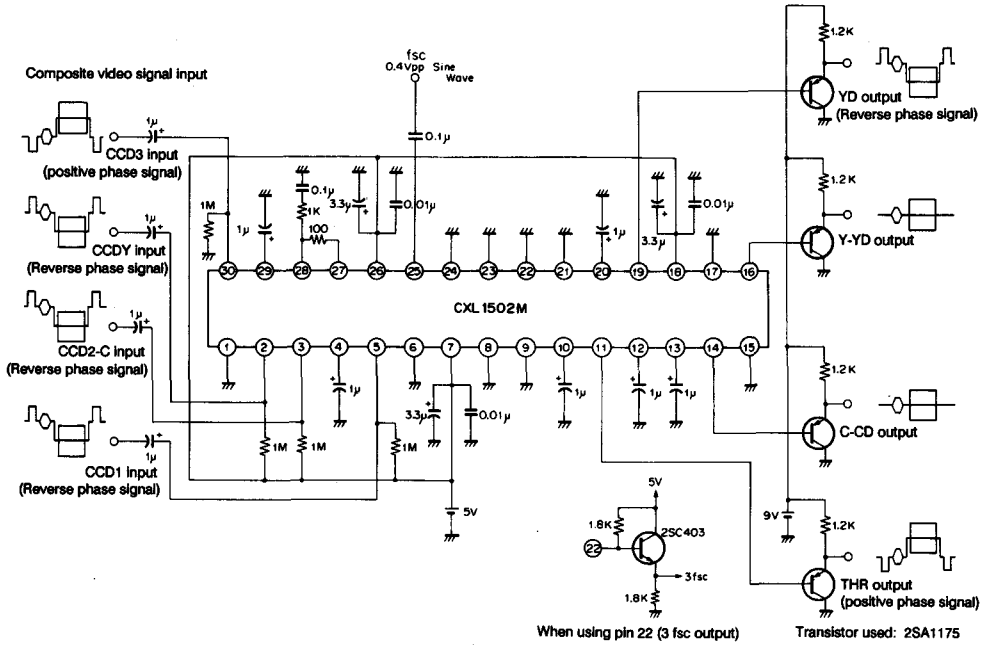
$$CCD = 20 \log \frac{\text{C-CD pin output voltage (4.441431 MHz)}}{\text{C-CD pin output voltage (4.437525 MHz)}} \text{ [dB]}$$

10. YCD is calculated in accordance with the following formula from the Y-YD pin output voltage when a 200mVp-p, 2.000011 MHz sinewave is simultaneously fed to pins CCD1, CCD2-C, CCDY and CCD3 and from the Y-YD pin output voltage when a 200 mVp-p, 1.992198 MHz sinewave is simultaneously fed to same. The input part bias is set to the same conditions as in testing CCD.

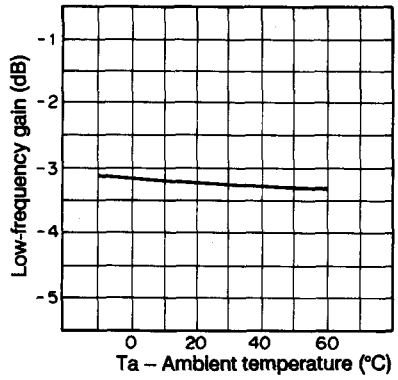
$$YCD = 20 \log \frac{\text{Y-YD pin output voltage (2.000011 MHz)}}{\text{Y-YD pin output voltage (1.992198 MHz)}} \text{ [dB]}$$



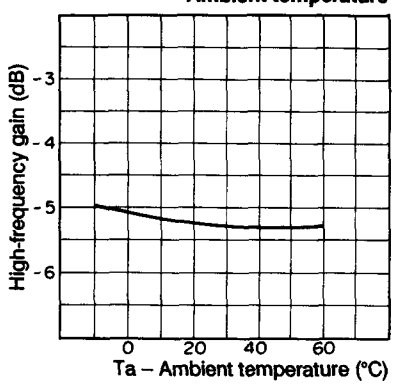
Application Circuit



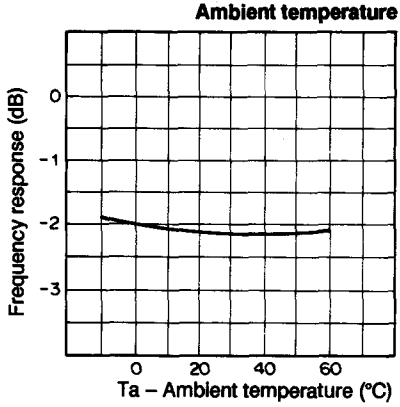
Low-frequency gain vs. Ambient temperature



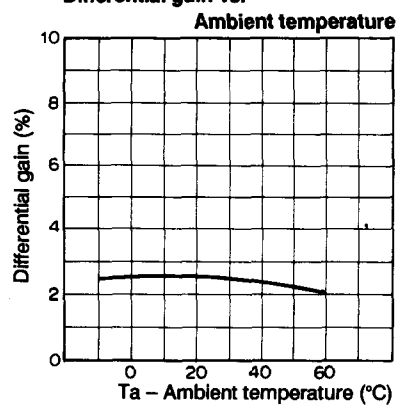
High-frequency gain vs. Ambient temperature



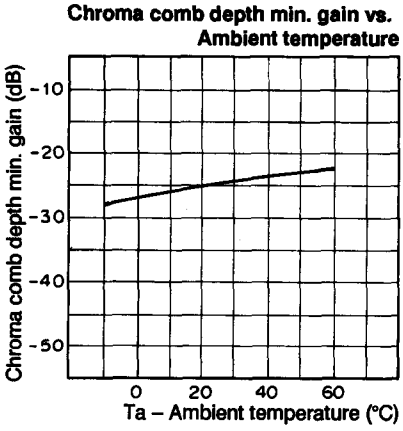
Frequency response vs. Ambient temperature



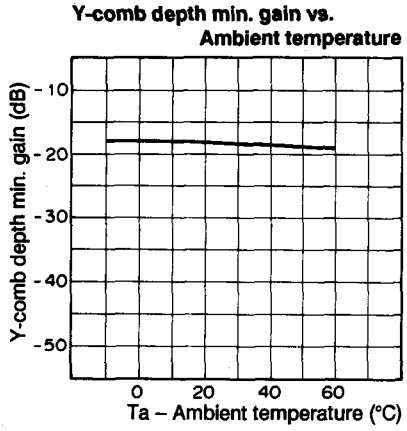
Differential gain vs. Ambient temperature



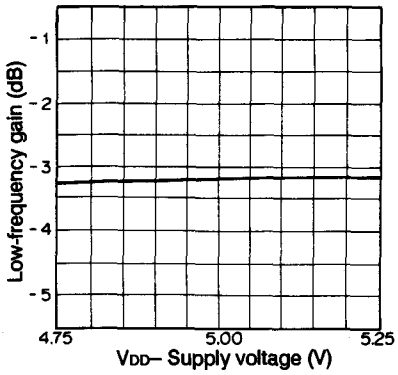
Chroma comb depth min. gain vs. Ambient temperature



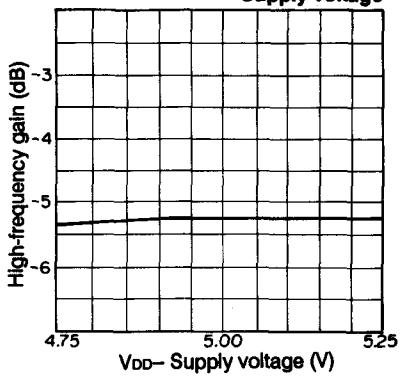
Y-comb depth min. gain vs. Ambient temperature



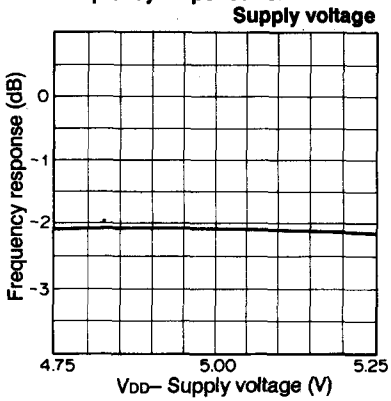
Low-frequency gain vs. Supply voltage



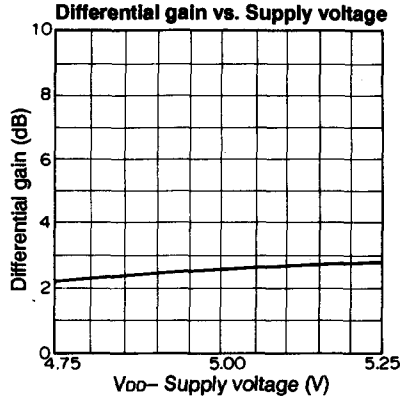
High-frequency gain vs. Supply voltage



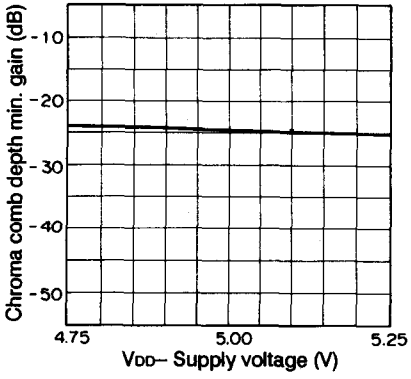
Frequency response vs. Supply voltage



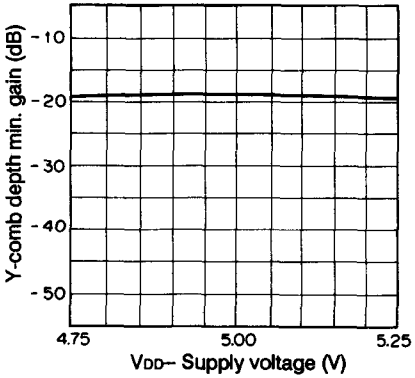
Differential gain vs. Supply voltage



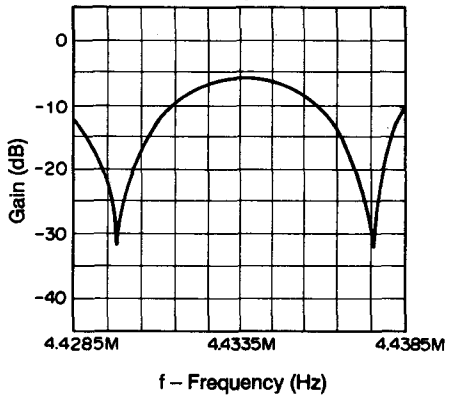
Chroma comb depth min. gain vs. Supply voltage



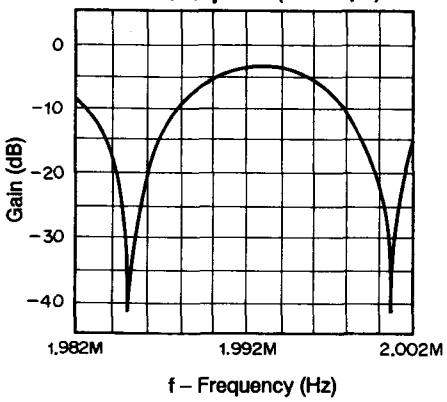
Y-comb depth min. gain vs. Supply voltage



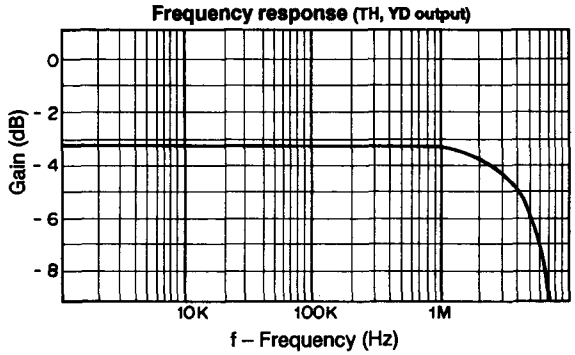
Chroma comb response (C-CD output)



Y-comb response (Y-YD output)



Frequency response (TH, YD output)



SONY

CXL1506M

CMOS-CCD 1H/2H Delay Line for PAL

Description

CXL1506M is a CMOS-CCD delay line developed for video signal processing. Usage in conjunction with an external low pass filter provide 1H and 2H delay signals simultaneously (For PAL signals).

16 pin SOP (Plastic)

Features

- Single power supply (5V)
- Low power consumption
- Built-in peripheral circuits
- Built-in tripling PLL circuit
- For PAL signals
- 1 input and 2 outputs
  (Outputs for both 1H and 2H delays)

Functions

- 847-bit (1H) and 1698-bit (2H) CCD register
- Clock driver
- Autobias circuit
- Sync tip clamp circuit
- Sample and hold circuit
- Tripling PLL circuit

Structure

CMOS-CCD

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	+6	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	400	mW

Recommended Operating Voltage (Ta = 25°C)

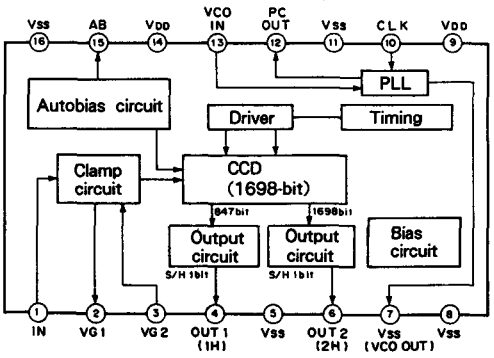
	V_{DD}	5V ± 5	%

Recommended Clock Conditions (Ta = 25°C)

• Input clock amplitude	V_{CLK}	0.2 to 1.0Vp-p (0.4Vp-p Typ.)	
• Input clock frequency	f_{CLK}	4.433619	MHz
• Input clock waveform	sine wave		

Input Signal Amplitude V_{SIG} 575 (MAX.) mVp-p (at internal clamp condition)

Block Diagram



E89X22A07 – ST

Pin Description

No.	Symbol	I/O	Description	Impedance (Ω)
1	IN	I	Signal input (Non-inverted signal)	>10kΩ (at no clamp)
2	VG1	O	Gate bias 1 DC output	
Note) 3	VG2	I	Gate bias 2 DC input	
4	OUT1	O	1H signal output (Inverted signal)	40 to 500 Ω
5	Vss	—	GND	
6	OUT2	O	2H signal output (Inverted signal)	40 to 500 Ω
7	Vss (VCOOUT)	(O)	GND or VCO output (3fsc)	
8	Vss	—	GND	
9	V_{DD}	—	Power supply (5V)	
10	CLK	I	Clock input (fsc)	>10kΩ
11	Vss	—	GND	
12	PC OUT	O	Phase comparator output	
13	VCO IN	I	VCO input	
14	V_{DD}	—	Power supply (5V)	
15	AB	O	Autobias DC output	600 to 200kΩ
16	Vss	—	GND	

Note) Description of Pin 3 (VG2)
Control of input signal clamp condition
0V····Sync chip clamp condition
5V····Center bias condition
The input signal is biased to approx. 2.1V by means of the IC internal resistance (approx. 10kΩ). In this mode the input signal is limited to the APL 50% and the maximum input signal amplitude is at 200mVp-p.

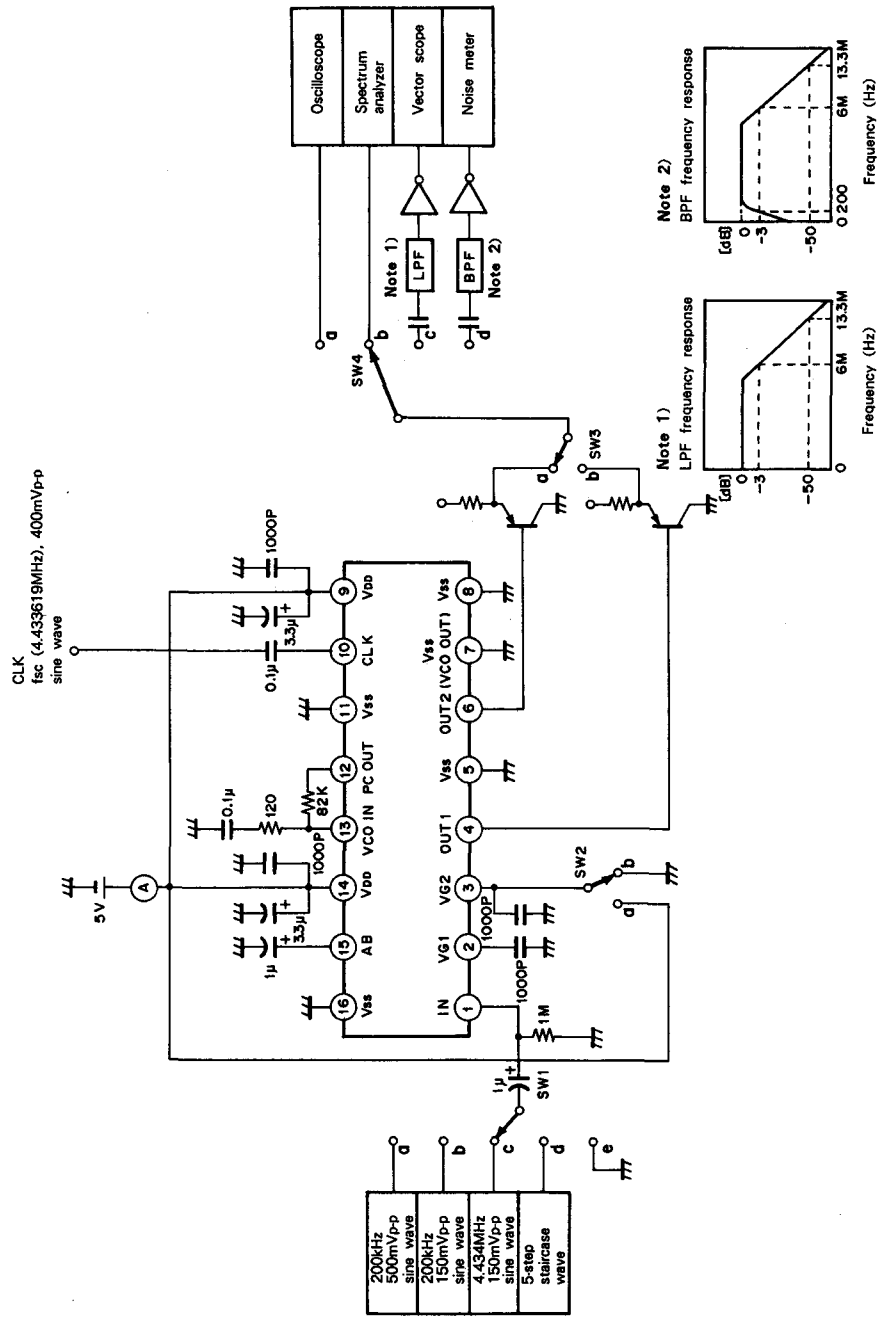
Electrical Characteristics

($Ta = 25°C$, $V_{DD} = 5V$, $f_{CLK} = 4.433619MHz$, $V_{CLK} = 400mVp\text{-}p$ sine wave)

See Electrical Characteristics Test Circuit

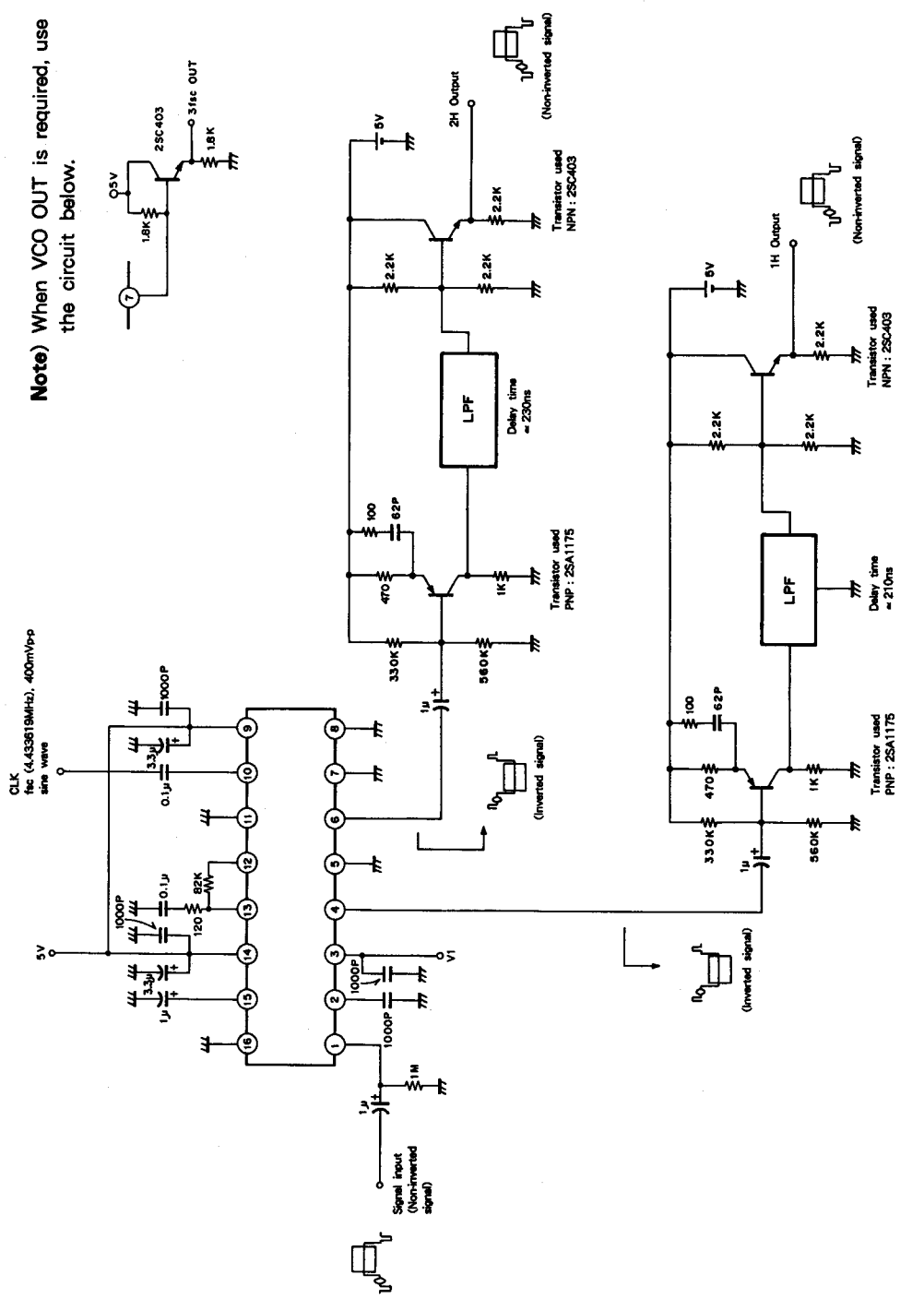
Item	Symbol	Test conditions (NOTE 1)	SW conditions 1	2	3	4	Min.	Typ.	Max.	Unit	NOTE
Supply current	I_{DD}	—	a	b	a	a	17	27	37	mA	2
Low frequency gain	GL1	200kHz 500mVp-p sine wave	a	b	a	b	−2	0	2	dB	3
	GL2		a	b	b	b	−2	0	2		
Frequency response	fR1	200kHz↔4.434MHz 150mVp-p sine wave	b↔c	a	a	b	−2.7	−1.7	−0.7	dB	4
	fR2		b↔c	a	b	b	−2.8	−1.8	−0.8		
Differential gain	DG1	5 staircase wave	d	b	a	c	—	5	7	%	5
	DG2		d	b	b	c	—	5	7		
Differential phase	DP1	5 staircase wave	d	b	a	c	—	5	7	degree	5
	DP2		d	b	b	c	—	5	7		
SN ratio	SN1	No signal input	e	b	a	d	52	56	—	dB	6
	SN2		e	b	b	d	52	56	—		
S/H pulse feed through	CP1	No signal input	e	b	a	a	—	—	350	mVp-p	7
	CP2		e	b	b	a	—	—	350		

Electrical Characteristics Test Circuit



Application Circuit

Note) When VCO OUT is required, use the circuit below.



NOTE)

1) By switching SW2, input condition turns out as follows.

SW2 condition	Input condition
a	Center bias condition (approx. 2.1V) Approx. 2.1V bias is applied internally to the input signal
b	Sync chip and clamp conditions

2) This is the supply current value during IC operation. Here the signal is input.

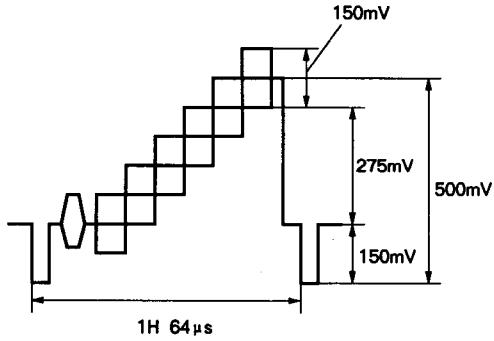
3) GL is the output gain of pin OUT when a 500mVp-p, 200kHz sine wave is fed to pin IN.

$$GL = 20\log \frac{\text{pin OUT output voltage [mVp-p]}}{\text{500 [mVp-p]}} \text{ [dB]}$$

4) Indicates the dissipation at 4.434MHz in relation to 200kHz. From the output voltage at pin OUT when a 150mVp-p, 200kHz sine wave is fed to pin IN, and from the output voltage at pin OUT when a 150mVp-p, 4.434MHz sine wave is fed to same, calculation is made according to the following formula.

$$fR = 20\log \frac{\text{pin OUT output voltage (4.434MHz) [mVp-p]}}{\text{pin OUT output voltage (200kHz) [mVp-p]}} \text{ [dB]}$$

5) The differential gain (DG) and the differential phase (DP), when the 5-step staircase wave in the following figure is fed, are tested with a vector scope :



6) The noise level of the output signal at no-input signal is tested with a video noise meter in the Sub Carrier Trap mode at BPF 100kHz to 5MHz. (Vn [Vrms])
The signal component is determined either by testing the output voltage (the same testing system as for noise level) at the input of 350mVp-p, 200kHz, or by utilizing values from GL to calculate according to the following formula. (Vs [Vp-p])

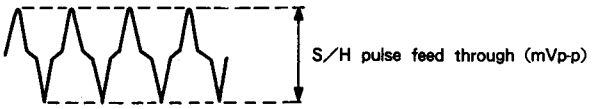
(Example of Vs calculation)

$$Vs = 0.35 \times 10^{\frac{GL}{20}}$$

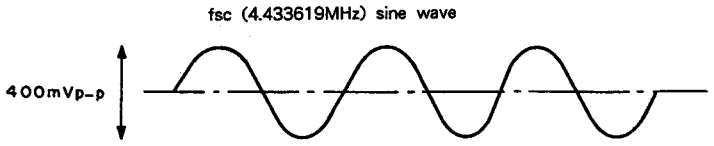
(Example of SN ratio calculation)

$$SN = 20\log \frac{Vn \text{ (noise component) [Vrms]}}{Vs \text{ (signal component) [Vp-p]}} [dB]$$

7) The internal clock component to the output signal during no-signal input and the leakage of that high harmonic component are tested.

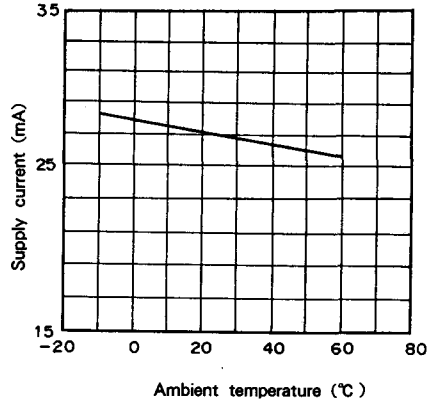


CLOCK

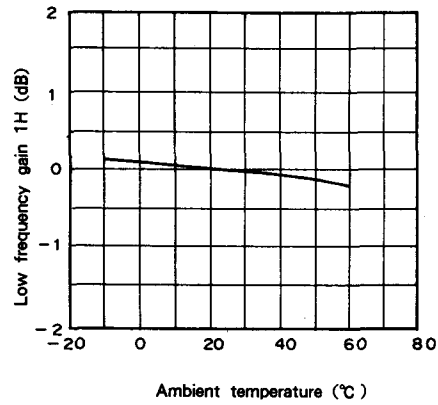


Example of Representative Characteristics

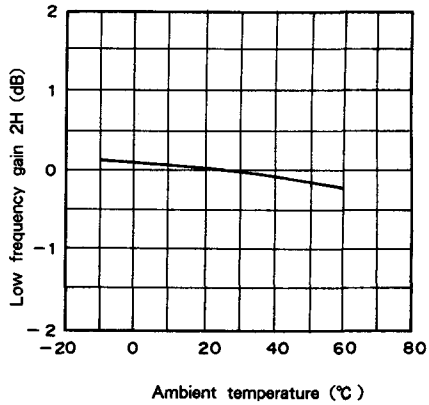
Supply current vs. Ambient temperature



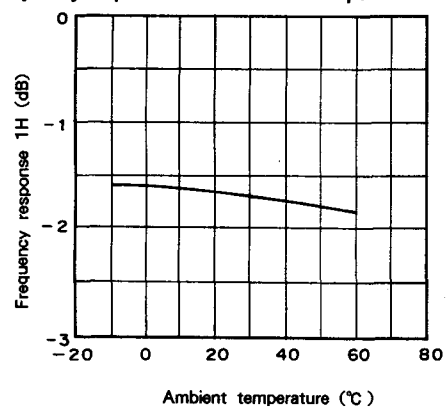
Low frequency gain (1H) vs. Ambient temperature



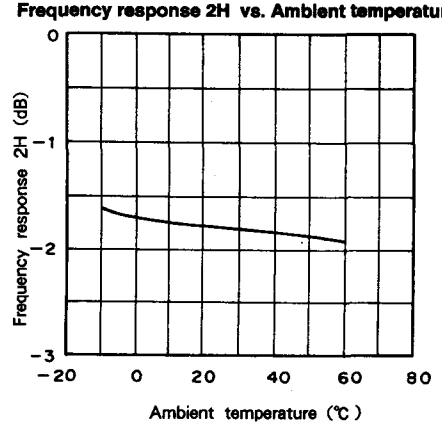
Low frequency gain (2H) vs. Ambient temperature



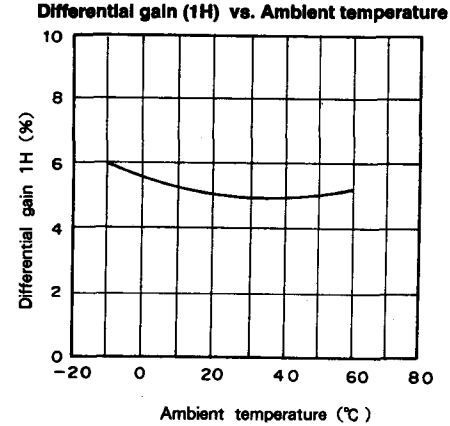
Frequency response 1H vs. Ambient temperature



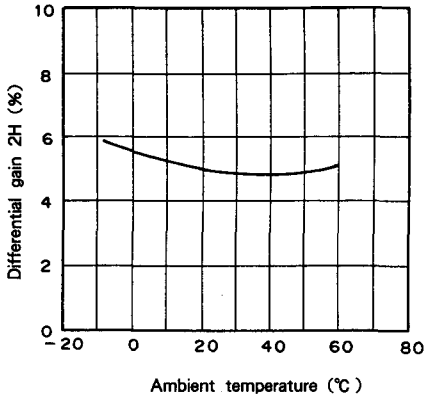
Frequency response 2H vs. Ambient temperature



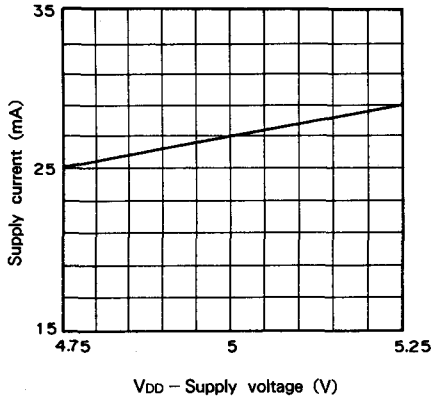
Differential gain (1H) vs. Ambient temperature



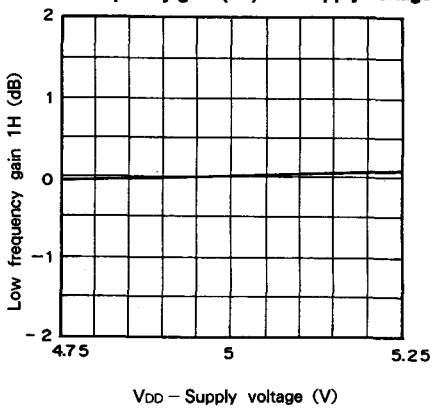
Differential gain (2H) vs. Ambient temperature



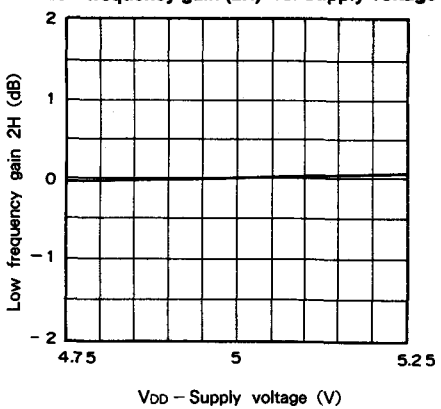
Supply current vs. Supply voltage



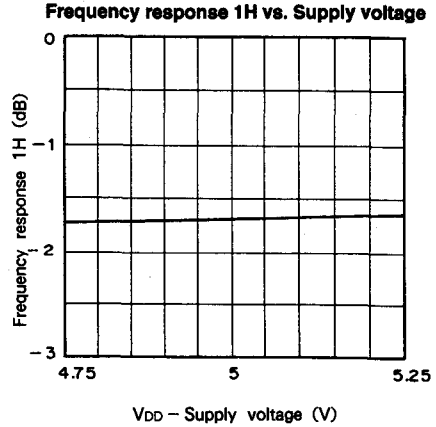
Low frequency gain (1H) vs. Supply voltage



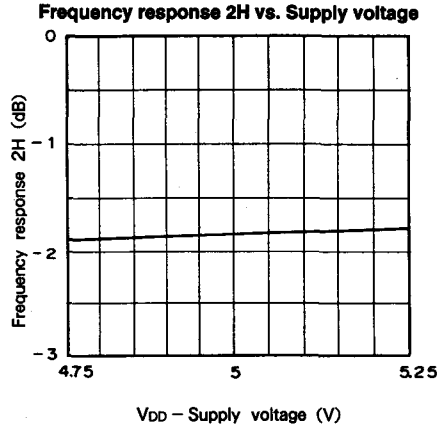
Low frequency gain (2H) vs. Supply voltage



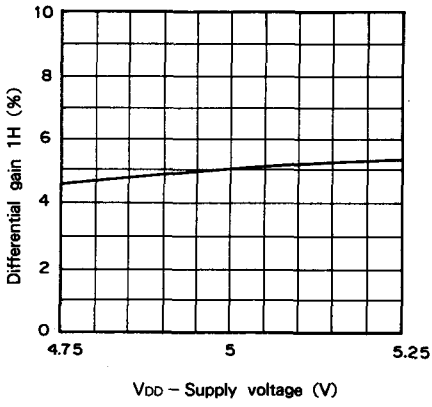
Frequency response 1H vs. Supply voltage



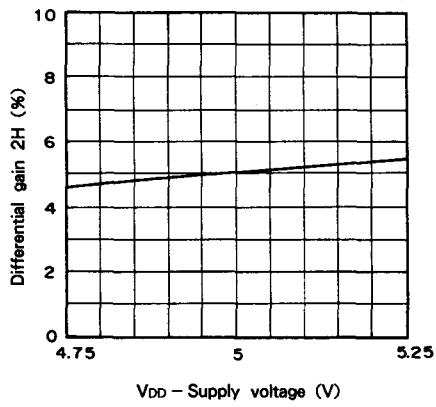
Frequency response 2H vs. Supply voltage



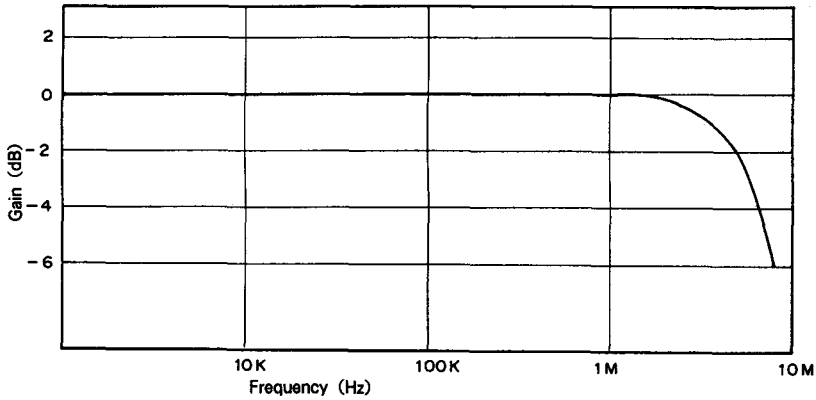
Differential gain (1H) vs. Supply voltage



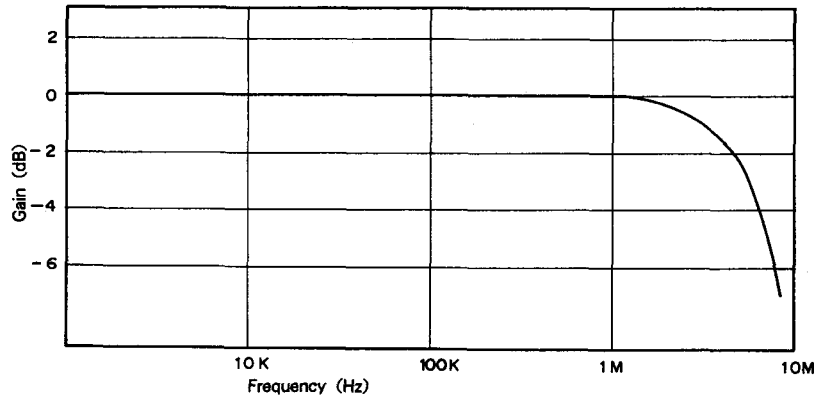
Differential gain (2H) vs. Supply voltage



Frequency response (1H output)



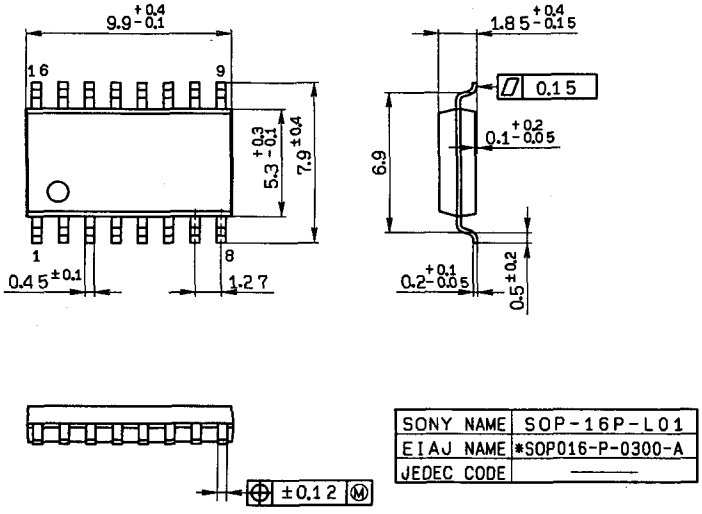
Frequency response (2H output)



Note) 1H and 2H shown in brackets indicate 1H and 2H outputs.

Package Outline Unit : mm

16pin SOP (Plastic) 300mil 0.2g



SONY NAME	SOP-16P-L01
EIAJ NAME	*SOP016-P-0300-A
JEDEC CODE	———

CCD Linear Sensor

7) CCD Linear Sensor

Type	Applications	Functions	Page
ILX501	Facsimile, Copy machine	5000-pixel, B/W linear sensor	903
ILX503	Facsimile, Image scanner	2048-Pixel, B/W linear sensor	913
ILX505		2592-Pixel, B/W linear sensor	923

SONY

ILX501

5000-pixel CCD Linear Sensor (B/W)

Description

The ILX501 is a reduction type CCD linear sensor developed for high resolution facsimiles and copiers. This sensor reads A3 size documents at a density of 400 DPI (Dot Per Inch). A built-in timing generator and clock-drivers ensure direct drive at 5V logic for easy use.

Features

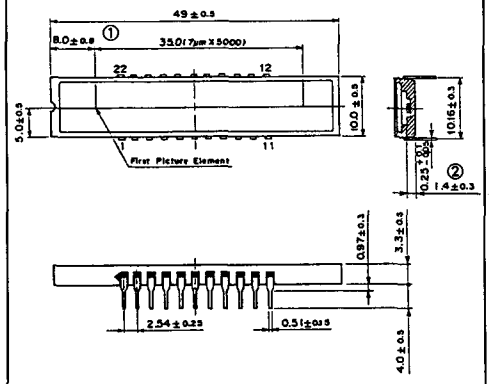
- Number of effective pixels : 5000 pixels
- Pixel size : 7 μm × 7 μm (7 μm pitch)
- Built in timing generator and clock-drivers
- Ultra low lag
- Maximum clock frequency : 12.5MHz

Absolute Maximum Ratings

• Supply voltage	V_{DD1}	11	V
	V_{DD2}	6	V
• Operation guarantee operating temperature		−10 to +55	°C
• Storage temperature		−30 to +80	°C

Package Outline

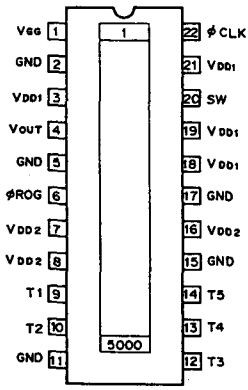
Unit : mm



Note

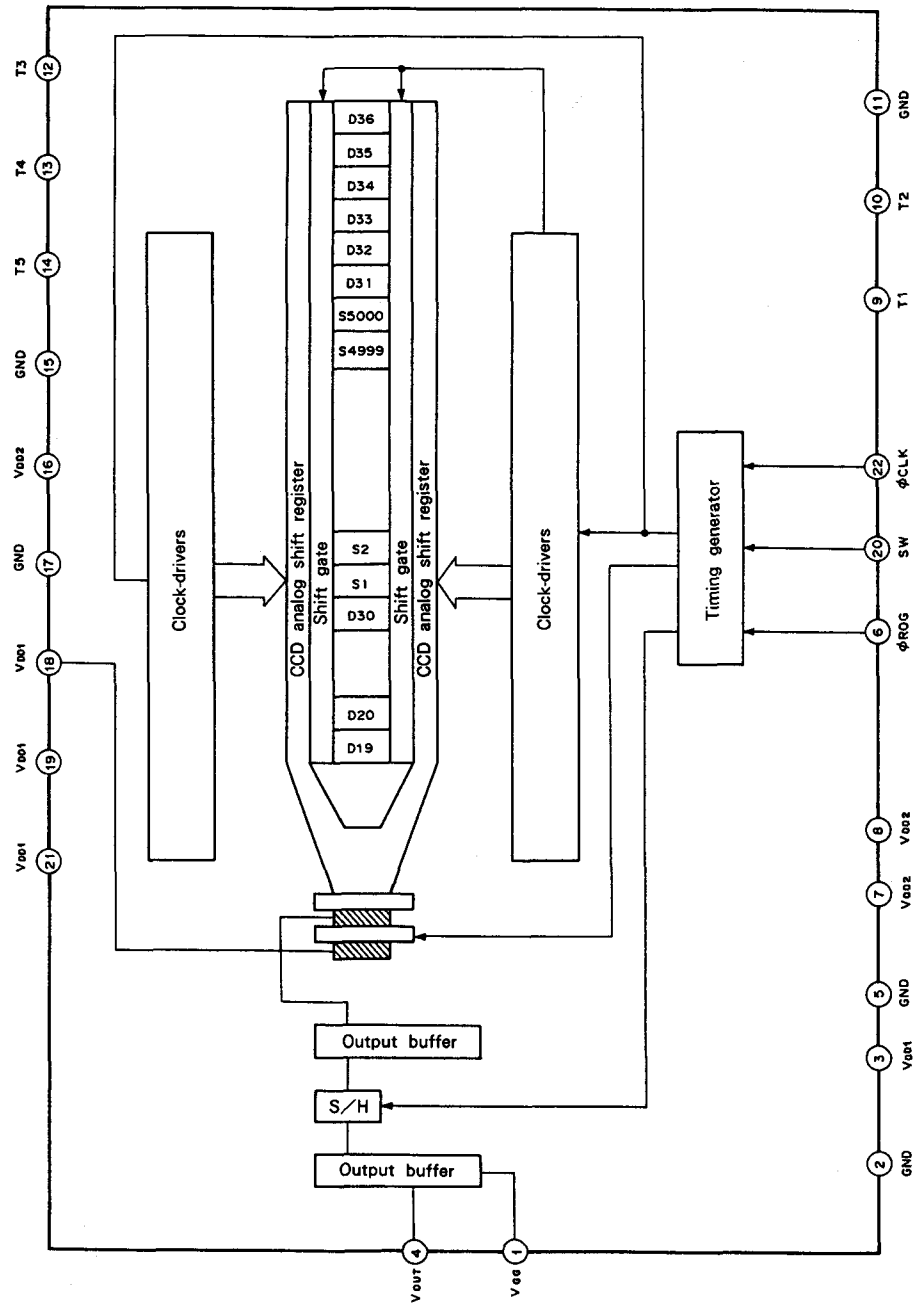
1) ①The distance from the package pin side to the first pixel.
2) ②The distance from the package bottom side to the surface of the sensor.
3) Glass thickness t = 0.8
   (Index of refraction = 1.5)

Pin Configuration (Top View)



E89X01 – ST

Internal Structure



Pin Description

Pin No.	Symbol	Description
1	V_{GG}	Output circuit gate bias
2	GND	GND
3	V_{DD1}	9V power supply
4	V_{OUT}	Signal output
5	GND	GND
6	ϕ ROG	Clock pulse
7	V_{DD2}	5V power supply
8	V_{DD2}	5V power supply
9	T1	Test pin
10	T2	Test pin
11	GND	GND
12	T3	Test pin
13	T4	Test pin
14	T5	Test pin
15	GND	GND
16	V_{DD2}	5V power supply
17	GND	GND
18	V_{DD1}	9V power supply
19	V_{DD1}	9V power supply
20	SW	Switch (with S/H→V_{DD1} (without S/H→GND)
21	V_{DD1}	9V power supply
22	ϕ CLK	Clock pulse

Recommended Voltage

Item	Min.	Typ.	Max.	Unit
V_{DD1}	8.5	9.0	9.5	V
V_{DD2}	4.75	5.0	5.25	V

Electrooptical Characteristics

($Ta = 25°C$, $V_{DD1} = 9V$, $V_{DD2} = 5V$, Light source = 3200K, IR cut filter, CM-500S (t = 1.0mm))

Item	Symbol	Min.	Typ.	Max.	Unit	φ CLK frequency	Remarks
Sensitivity	R	0.8	1.1	1.35	V/lxsec	6MHz	Note 2
Sensitivity nonuniformity	PRNU	—	8	20	%	6MHz	Note 3
Saturation output voltage	V_{SAT}	0.8	—	—	V	6MHz	Note 4
Even and odd black level DC difference	ΔV	—	25	80	mV	6MHz	Note 5
Dark voltage average	V_{DRK}	—	—	5	mV	1MHz	Note 6
Dark signal nonuniformity	DSNU	—	—	5	mV	1MHz	Note 7
9V supply current	I_{VDD1}	—	8	12.5	mA	6MHz	—
5V supply current	I_{VDD2}	—	36	50	mA	6MHz	—
Total transfer efficiency	TTE	90	95	—	%	6MHz	—

Note

1) In accordance with the given electrooptical characteristics, the even black level is defined as the mean value of D8, D10, D12, D14 and D16. The odd black level is defined as the mean value of D7, D9, D11, D13 and D15.

2) For the sensitivity test light is applied with a uniform intensity of illumination.

3) PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 2.

$$PRNU = \frac{V_{MAX} - V_{MIN}}{V_{AVE}} \times 100 \ (\%)$$

Where the 5000 pixels are divided into blocks of 100, even and odd pixels, respectively. The maximum output of each block is set to V_{MAX}, the minimum output to V_{MIN} and the average output to V_{AVE}.

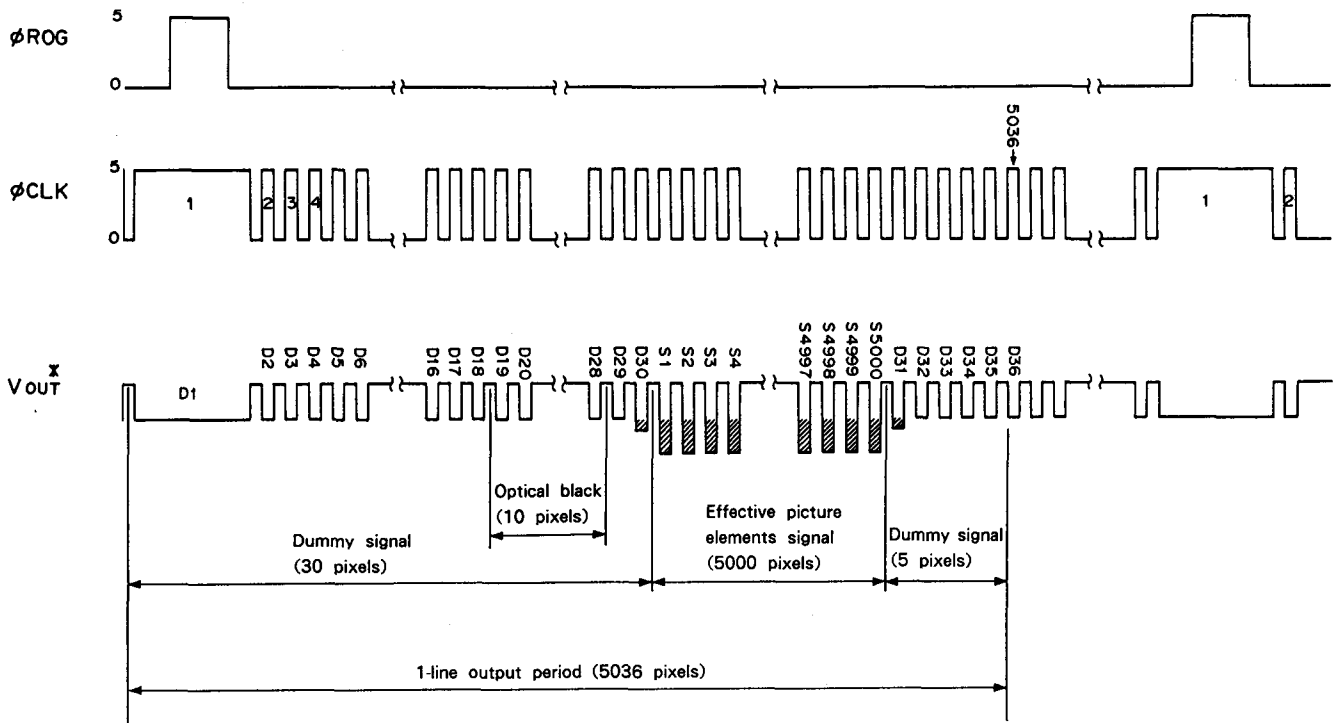
4) Use below the minimum value of the saturation output voltage.

5) Indicates the DC difference in value between odd black level and even black level when φ CLK = 6MHz.

6) Optical signal accumulated time τ int stands at 10msec.

7) The difference between the maximum and mean values of the dark output voltage is calculated for even and odd respectively. The larger value is defined as the dark signal nonuniformity.
Optical signal accumulated time τ int stands at 10msec.

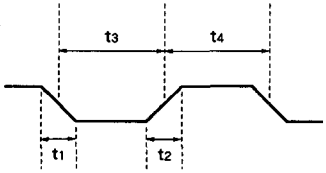
Clock Timing Diagram



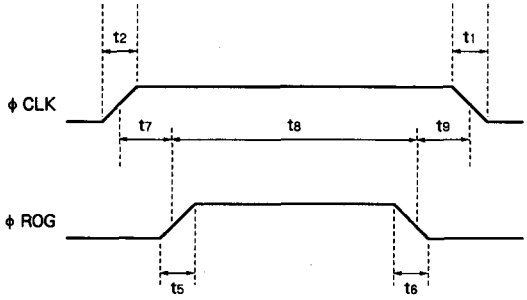
*When signal output without S/H (Pin 20→GND)

Input Clock Waveform Condition

φ CLK Timing

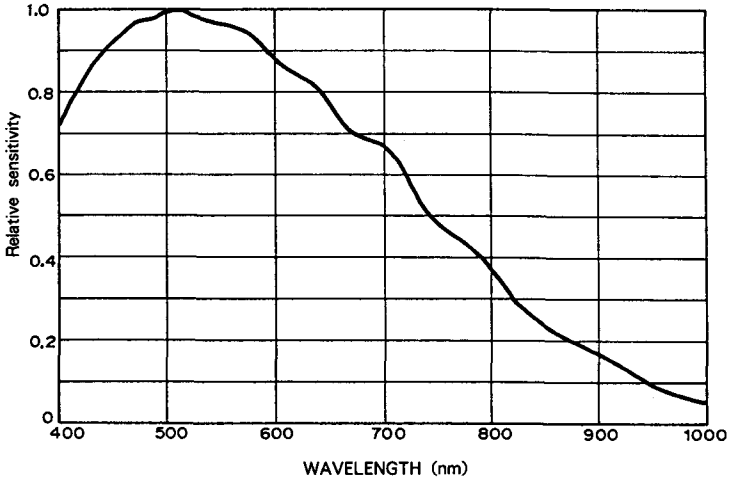


φ CLK, φ ROG Timing

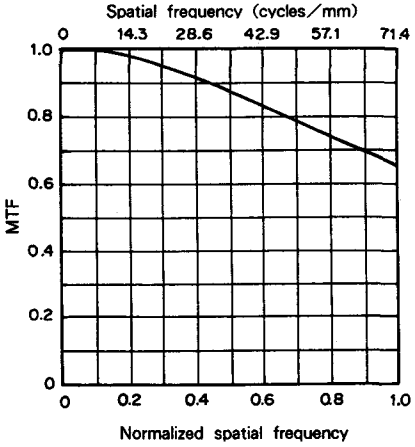


Item		Symbol	Min.	Typ.	Max.	Unit
φ CLK, φ ROG pulse rise/fall time		t_1, t_2, t_5, t_6	—	5	10	nsec
φ ROG pulse period		t_8	800	1000	—	nsec
φ CLK, φ ROG pulse timing		t_7, t_9	100	200	—	nsec
φ CLK pulse duty (t_3/ ($t_3 + t_4$) × 100)		—	40	50	60	%
φ CLK, φ ROG pulse voltage	High level	V φ CLK V φ ROG	4.5	5.0	5.5	V
	Low level		0	—	0.5	V

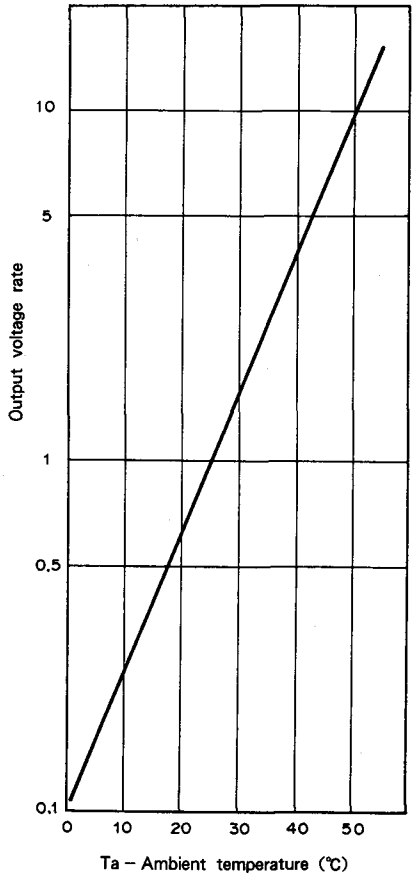
Spectral sensitivity characteristics (Standard characteristics)



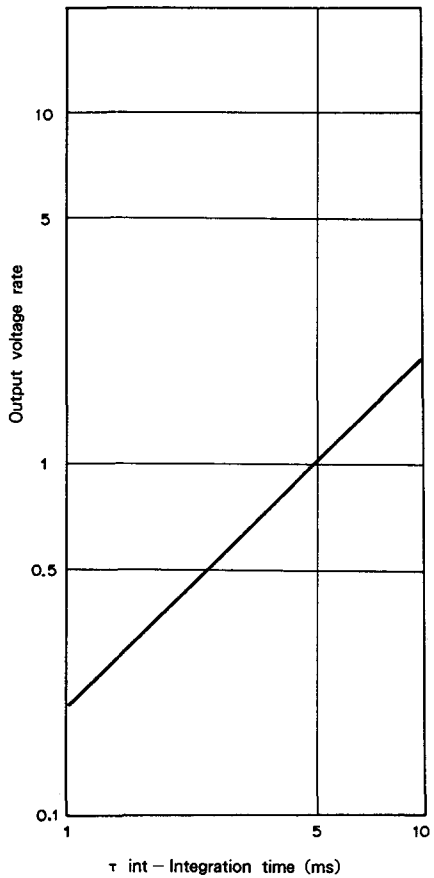
Modulation Transfer Function of main scanning direction (Standard characteristics)



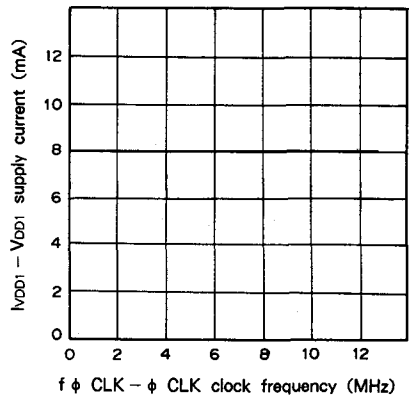
Dark signal output temperature characteristics (Standard characteristics)



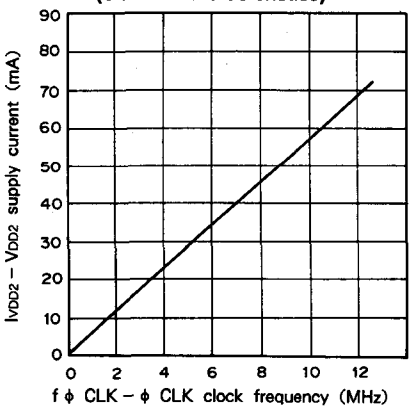
Integration time output voltage characteristics (Standard characteristics)



Operational frequency characteristics of the V_{DD1} supply current (Standard characteristics)

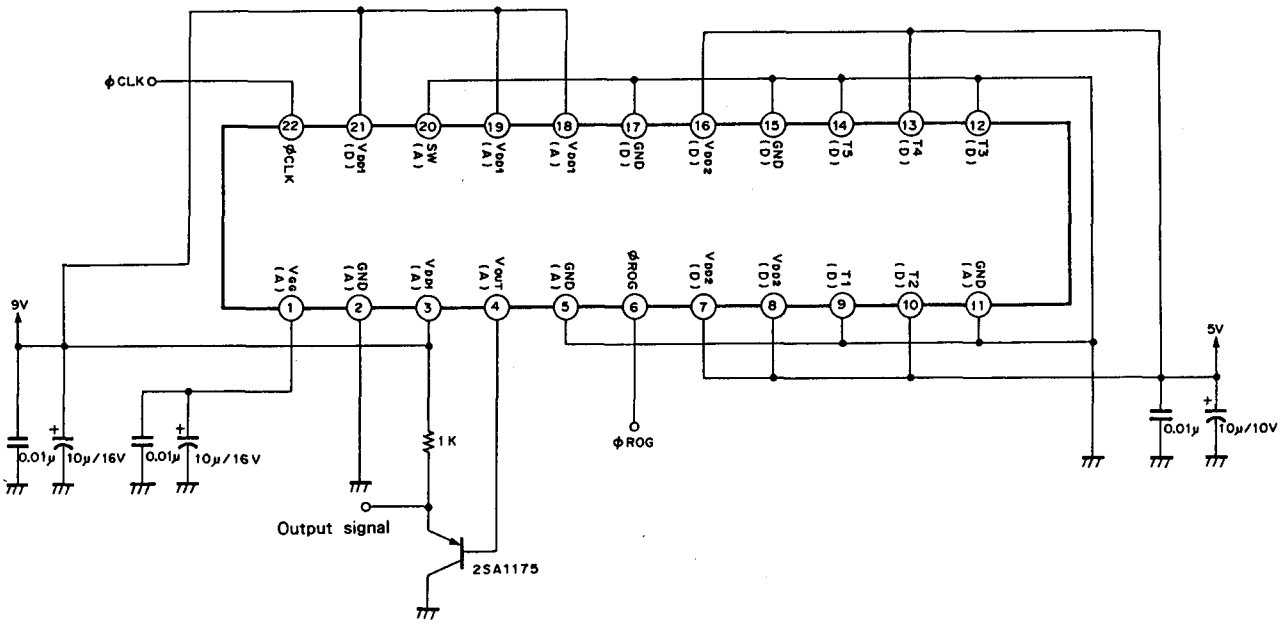


Operational frequency characteristics of the V_{DD2} supply current (Standard characteristics)



Application Circuit

At signal output without S/H



*1 When signal output with S/H, fall Pin 20 to 9V.

*2 When noise effect to the output signal is large connect (A) to analog supply, (D) to digital supply and enlarge the decoupling capacitor values.

Notes on Handling

1) Static charge prevention
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensor.
   e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Regulation for raising and lowering the power supply voltage.
When raising the supply voltage, first raise V_{DD1} (9V) and then V_{DD2} (5V). Similarly, lower V_{DD2} (5V) first and then V_{DD1} (9V).

3) Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an imaging device do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

4) Dust and dirt protection
   a) Operate in clean environments
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

SONY

ILX503

2048-pixel CCD Linear Sensor (B/W)

Description

The ILX503 is a reduction type CCD linear sensor designed for facsimile, image scanner and OCR use. This sensor reads B4 size documents at a density of 200 DPI (Dot Per Inch). A built-in timing generator and clock-drivers ensure direct drive at 5V logic for easy use.

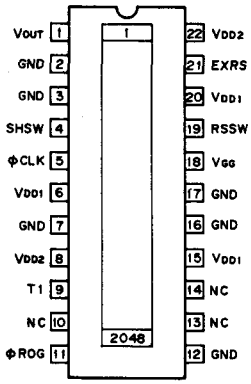
Features

- Number of effective pixels: 2048 pixels
- Pixel size: 14 μm × 14 μm (14 μm pitch)
- Built in timing generator and clock-drivers
- Ultra low lag
- Maximum clock frequency: 5MHz

Absolute Maximum Ratings

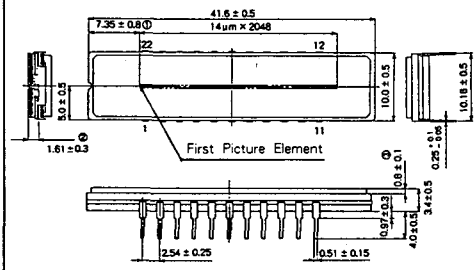
• Supply voltage	V_{DD1}	11	V
	V_{DD2}	6	V
• Operation guarantee operating temperature		−10 to +55	°C
• Storage temperature		−30 to +80	°C

Pin Configuration (Top View)



Package Outline

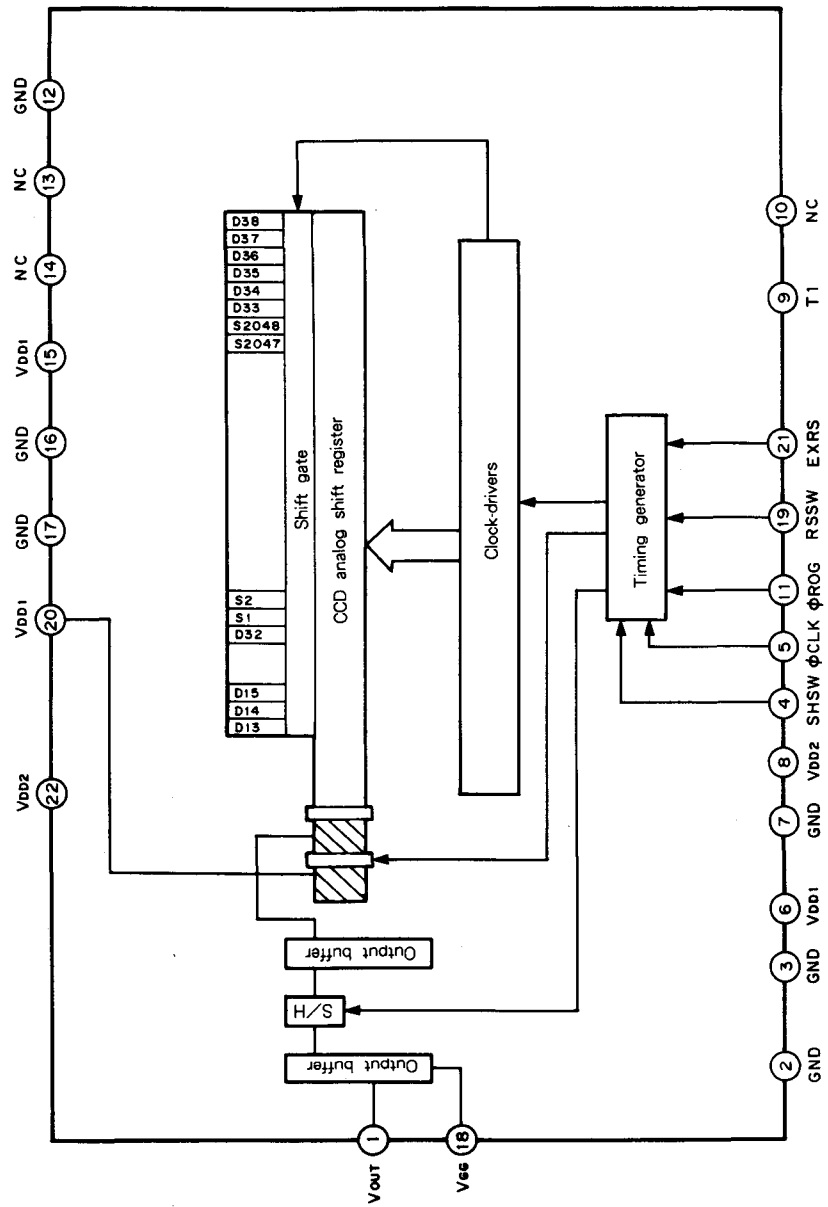
Unit : mm



Note

1) ① The distance from the package pin side to the first pixel.
2) ② The distance from the package bottom side to the surface of the sensor.
3) Glass thickness t=0.8 (Index of refraction=1.5)

Internal Structure



Pin Description

Pin No.	Symbol	Description
1	V_{OUT}	Signal output
2	GND	GND
3	GND	GND
4	SHSW	Switch (with S/H → GND / without S/H → V_{DD2})
5	ϕ CLK	Clock pulse
6	V_{DD1}	9V power supply
7	GND	GND
8	V_{DD2}	5V power supply
9	T1	Test pin (V_{DD2})
10	NC	
11	ϕ ROG	Clock pulse
12	GND	GND
13	NC	
14	NC	
15	V_{DD1}	9V power supply
16	GND	GND
17	GND	GND
18	V_{GG}	Output circuit gate bias
19	RSSW	RS pulse external, internal selection (External RS → V_{DD2}, Internal RS → GND)
20	V_{DD1}	9V power supply
21	EXRS	RS input pin during external RS pulse usage
22	V_{DD2}	5V power supply

Recommended Voltage

Item	Min.	Typ.	Max.	Unit
V_{DD1}	8.5	9.0	9.5	V
V_{DD2}	4.75	5.0	5.25	V

Note) Rules for raising and lowering power supply voltage.
To raise power supply voltage, first raise V_{DD1} (9V) and then V_{DD2} (5V).
To lower voltage, first lower V_{DD2} (5V) and then V_{DD1} (9V).

Electrooptical Characteristics

(Ta=25 °C , V_{DD1}=9V, V_{DD2}=5V, Light source=3200K, IR cut filter, CM-500S (t=1.0mm))

Item	Symbol	Min.	Typ.	Max.	Unit	φ CLK frequency	Remarks
Sensitivity	R	22.5	30.0	37.5	V/(lx • s)	1MHz	Note 1
Sensitivity nonuniformity	PRNU	0	8.0	20	%	1MHz	Note 2
Saturation output voltage	V_{SAT}	1.0	2.5	—	V	1MHz	Note 3
Dark voltage average	V_{DRK}	0	0.5	5.0	mV	1MHz	Note 4
Dark signal nonuniformity	DSNU	0	0.5	5.0	mV	1MHz	Note 4
9V supply current	I_{VDD1}	—	8.0	14.0	mA	1MHz	—
5V supply current	I_{VDD2}	—	3.0	6.0	mA	1MHz	—
Total transfer efficiency	TTE	92.0	97.0	100	%	1MHz	—

Note

1) For the sensitivity test light is applied with a uniform intensity of illumination.

2) PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 1.

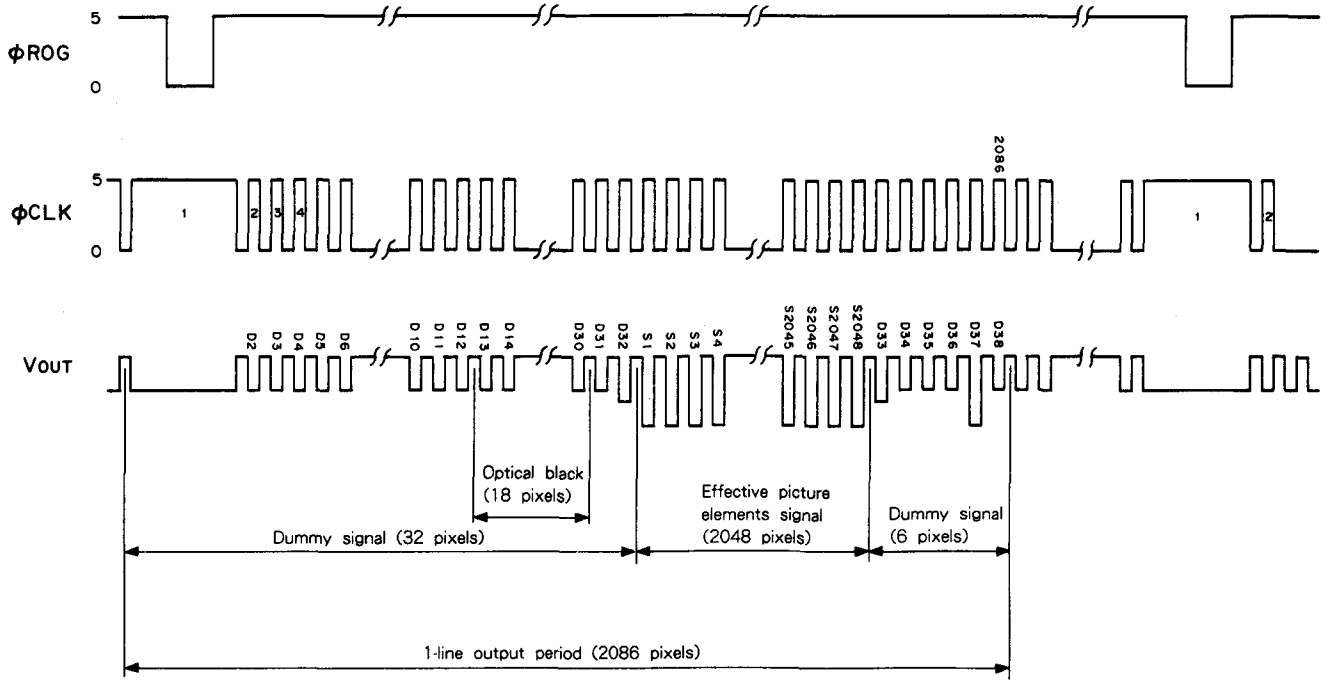
$$PRNU=\frac{V_{MAX}-V_{MIN}}{V_{AVE}} \times 100\ (\%)$$

Where the 2048 pixels are divided into blocks of 100. The maximum output of each block is set to V_{MAX}, the minimum output to V_{MIN} and the average output to V_{AVE}.

3) Use below the minimum value of the saturation output voltage.

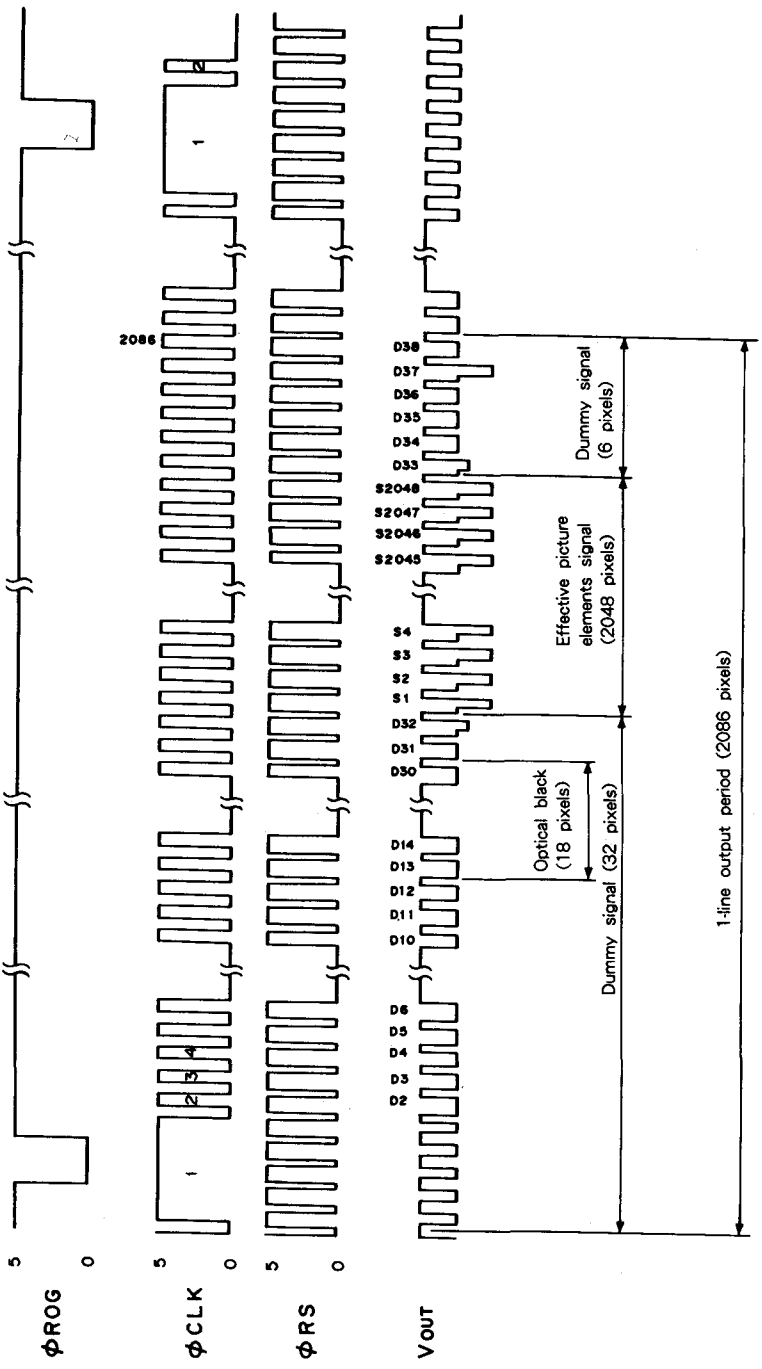
4) Optical signal accumulated time τ int stands at 10ms.

Clock Timing Diagram (For Internal RS mode)

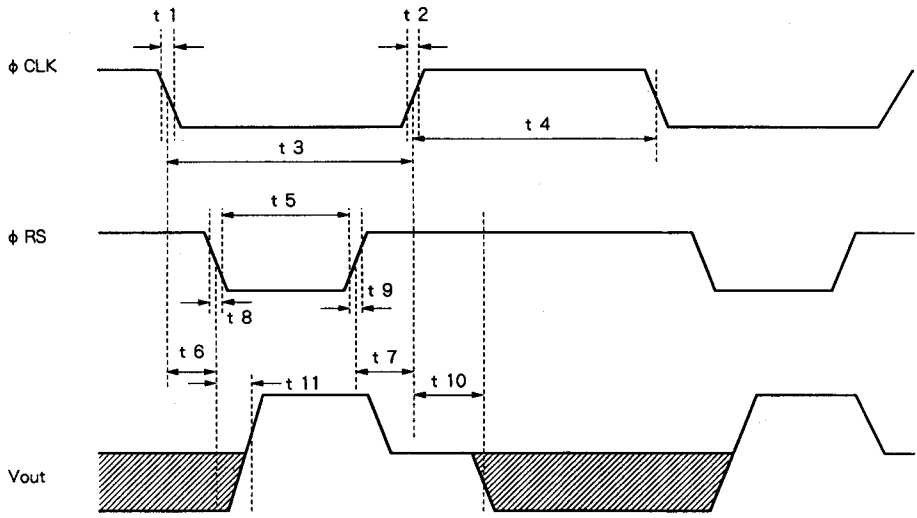


* When signal output without S/H (Pin 4 → V_{DD2})

Clock Timing Diagram (For External RS mode)



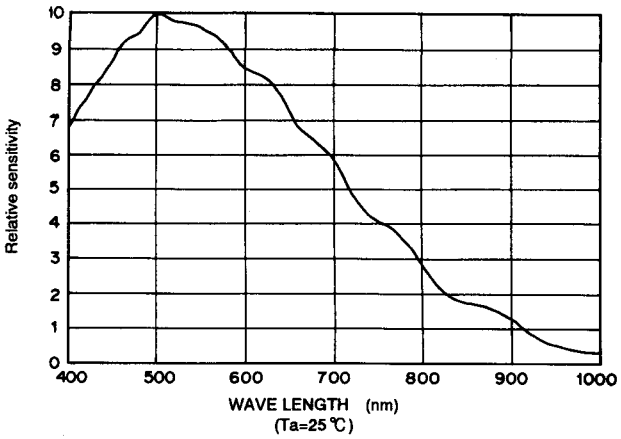
φ CLK, φ RS, Vout Timing



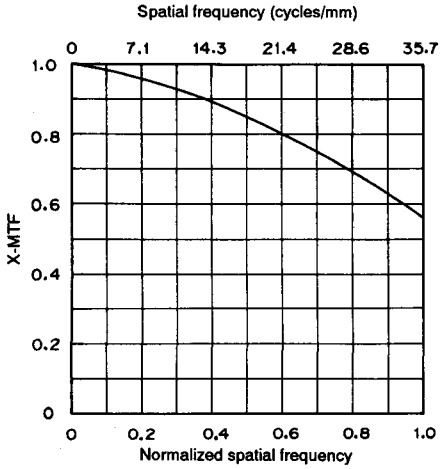
Item	Symbol	Min.	Typ.	Max.	Unit
φ CLK, φ RS pulse rise/fall time	t1, t2, t8, t9	—	10	50	ns
φ CLK pulse duty (Note 1)	—	40	50	60	%
φ CLK–RS pulse timing	t6	0	100	—	ns
φ CLK–RS pulse timing	t7	50	100	—	ns
φ RS pulse period	t5	50	100	—	ns
φ CLK–Vout	t10	50	80	110	ns
φ RS–Vout	t11	30	50	70	ns

Note 1) 100×t 3/(t 3+t 4)

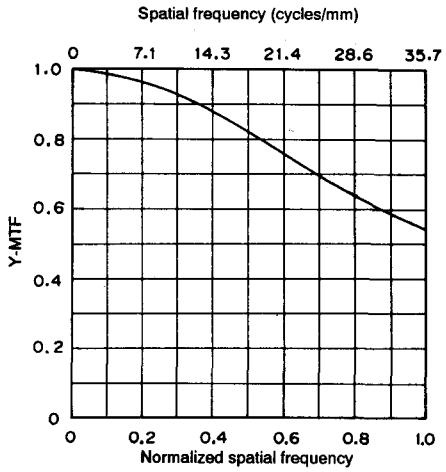
Spectral sensitivity characteristics
(Standard characteristics)



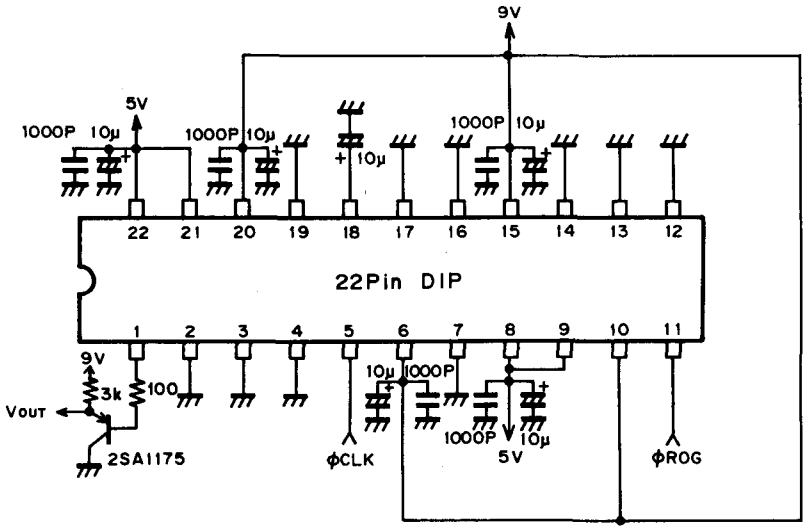
MTF of main scanning direction
(Standard characteristics)



MTF of sub scanning direction
(Standard characteristics)



Application Circuit



* Wen signal output without S/H, fall Pin 4 to V_{DD2}.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Handling

1) Static charge prevention
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensor.
   e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Regulation for raising and lowering the power supply voltage.
When raising the supply voltage, first raise V_{DD1} (9V) and then V_{DD2} (5V). Similarly, lower V_{DD2} (5V) first and then V_{DD1} (9V).

3) Soldering
   a) Make sure the package temperature does not exceed 80 °C .
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an imaging device do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

4) Dust and dirt protection
   a) Operate in clean environments
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

SONY

ILX505

2592-pixel CCD Linear Sensor (B/W)

Preliminary

Description

The ILX505 is a reduction type CCD linear sensor designed for facsimile, image scanner and OCR use. This sensor reads A3 size documents at a density of 200 DPI (Dot Per Inch). A built-in timing generator and clock-drivers ensure direct drive at 5V logic for easy use.

Features

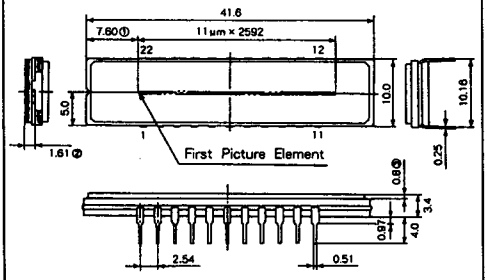
- Number of effective pixels: 2592 pixels
- Pixel size: 11 μm × 11 μm (11 μm pitch)
- Built in timing generator and clock-drivers
- Ultra low lag
- High sensitivity
- Maximum clock frequency: 5MHz

Absolute Maximum Ratings

• Supply voltage	V_{DD1}	11	V
	V_{DD2}	6	V
• Operation guarantee operating temperature		−10 to +55	°C
• Storage temperature		−30 to +80	°C

Package Outline

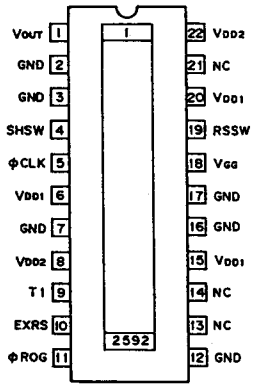
Unit : mm



Note

1) ①The distance from the package pin side to the first pixel.
2) ②The distance from the package bottom side to the surface of the sensor.
3) Glass thickness t=0.8 (Index of refraction=1.5)

Pin Configuration (Top View)



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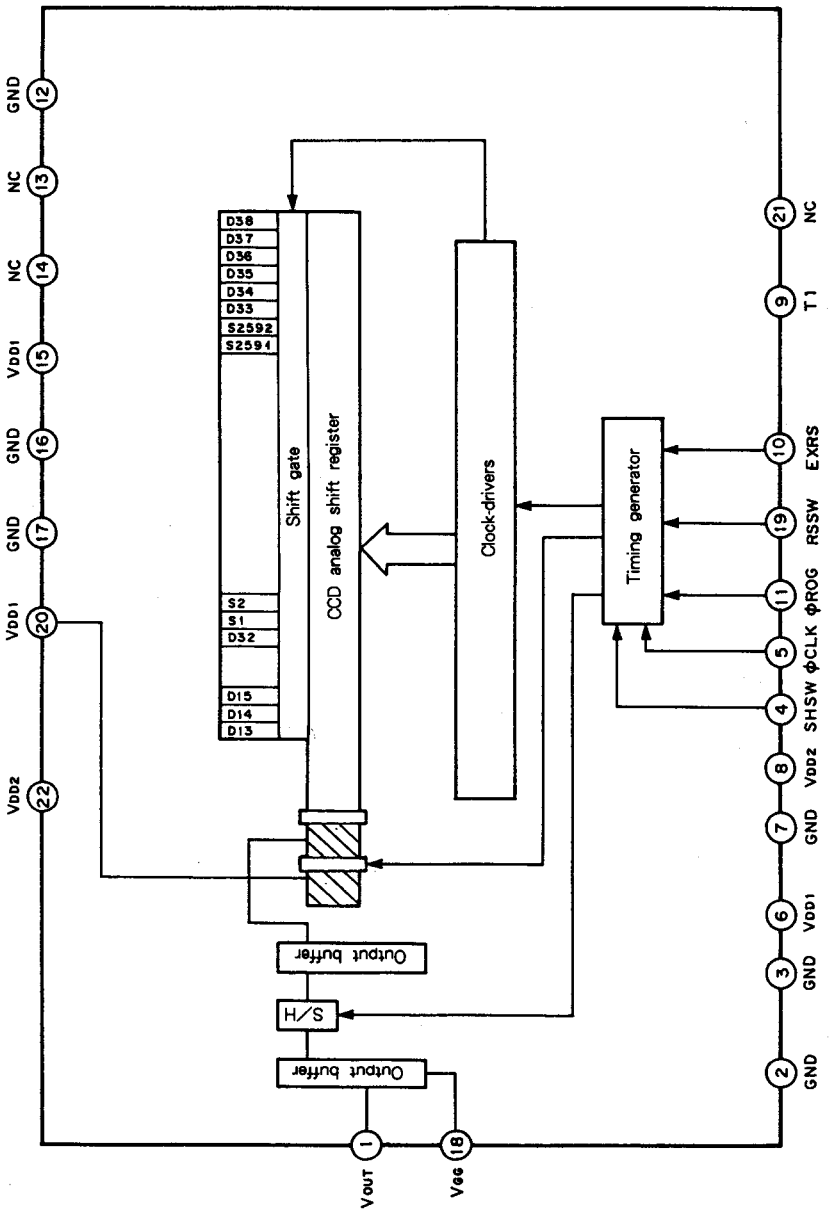
Internal Structure



Pin Description

Pin No.	Symbol	Description
1	V_{OUT}	Signal output
2	GND	GND
3	GND	GND
4	SHSW	Switch (with S/H → GND / without S/H → V_{DD2})
5	ϕ CLK	Clock pulse
6	V_{DD1}	9V power supply
7	GND	GND
8	V_{DD2}	5V power supply
9	T1	Test pin
10	EXRS	External RS pulse input. Must be connected to V_{DD2} when the internal RS pulse is used.
11	ϕ ROG	Clock pulse
12	GND	GND
13	NC	NC
14	NC	NC
15	V_{DD1}	9V power supply
16	GND	GND
17	GND	GND
18	V_{GG}	Output circuit gate bias
19	RSSW	Reset pulse switchover pin
20	V_{DD1}	9V power supply
21	NC	NC
22	V_{DD2}	5V power supply

Mode Description

Mode in Use	19 pin RSSW	10 pin EXRS
Internal RS	GND	V_{DD2}
External RS	V_{DD2}	ϕRS

Note) When the external RS mode is in use, operation of the internal S/H is not guaranteed. Pin 4 must be connected to 5V DC power supply.

Recommended Voltage

Item	Min.	Typ.	Max.	Unit
V_{DD1}	8.5	9.0	9.5	V
V_{DD2}	4.75	5.0	5.25	V

Note) Rules for raising and lowering power supply voltage.
To raise power supply voltage, first raise V_{DD1} (9V) and then V_{DD2} (5V).
To lower voltage, first lower V_{DD2} (5V) and then V_{DD1} (9V).

Electrooptical Characteristics

(Ta=25℃, V_{DD1}=9V, V_{DD2}=5V, Light source=3200K, IR cut filter, CM-500S (t=1.0mm))
Operational mode: Internal RS mode (Pin 19=GND, Pin 10=V_{DD2})

Item	Symbol	Min.	Typ.	Max.	Unit	ϕ CLK frequency	Remarks
Sensitivity	R	—	21.0	—	V/lx.sec	1MHz	Note 1
Sensitivity nonuniformity	PRNU	—	8.0	—	%	1MHz	Note 2
Saturation output voltage	V_{SAT}	—	1.5	—	V	1MHz	
Dark voltage average	V_{DRK}	—	2.0	—	mV	1MHz	Note 3
Dark signal nonuniformity	DSNU	—	2.0	—	mV	1MHz	Note 3
9V supply current	I_{VDD1}	—	14.0	—	mA	1MHz	—
5V supply current	I_{VDD2}	—	5.0	—	mA	1MHz	—
Total transfer efficiency	TTE	—	97.0	—	%	1MHz	—

Note

1) For the sensitivity test light is applied with a uniform intensity of illumination.

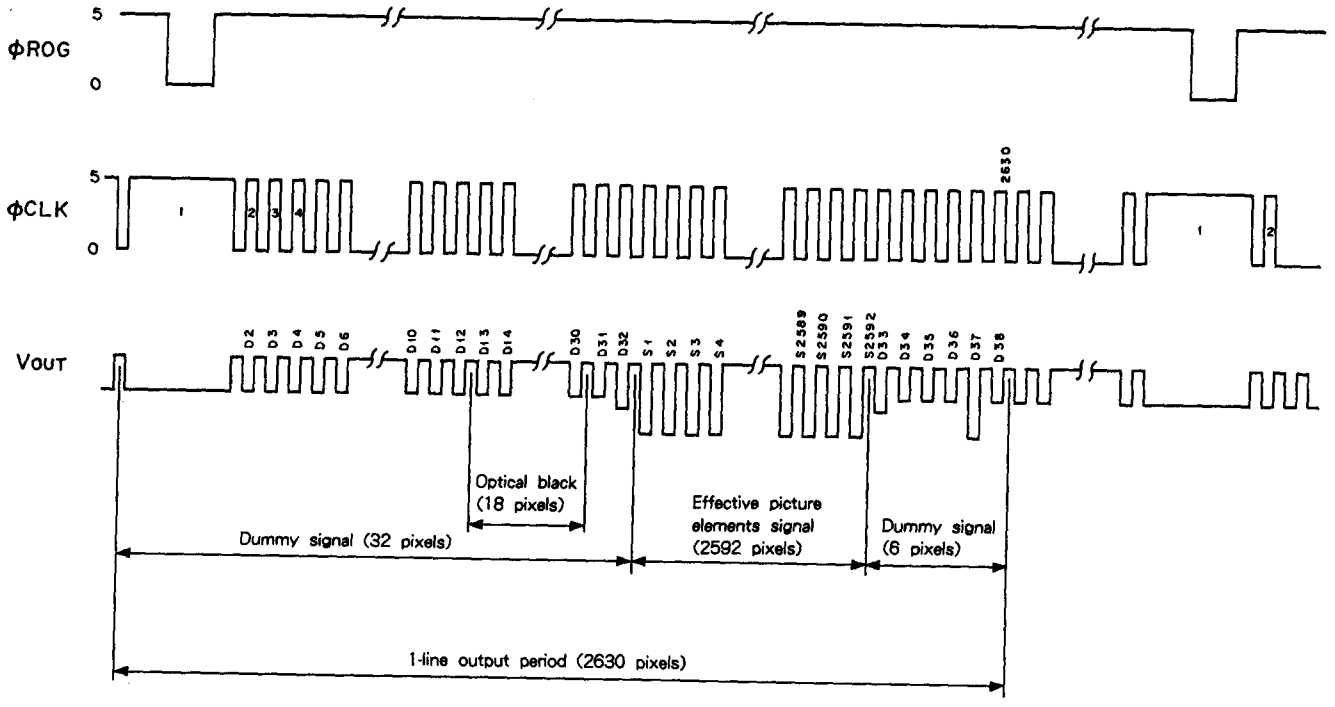
2) PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 1.

$$PRNU=\frac{V_{MAX}-V_{MIN}}{V_{AVE}} \times 100\ (\%)$$

Where the 2592 pixels are divided into blocks of 100. The maximum output of each block is set to V_{MAX}, the minimum output to V_{MIN} and the average output to V_{AVE}.

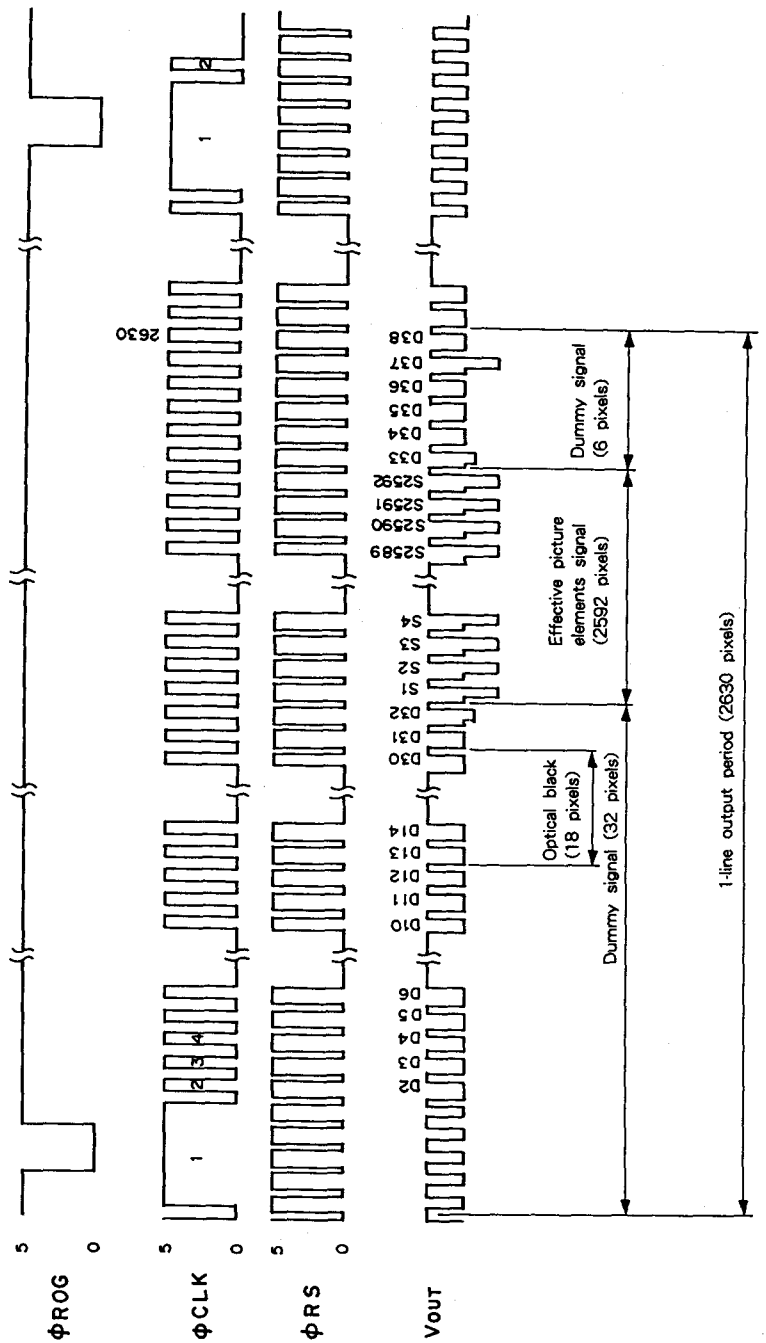
3) Optical signal accumulated time τ int stands at 10msec.

Clock Timing Diagram (For Internal RS mode)

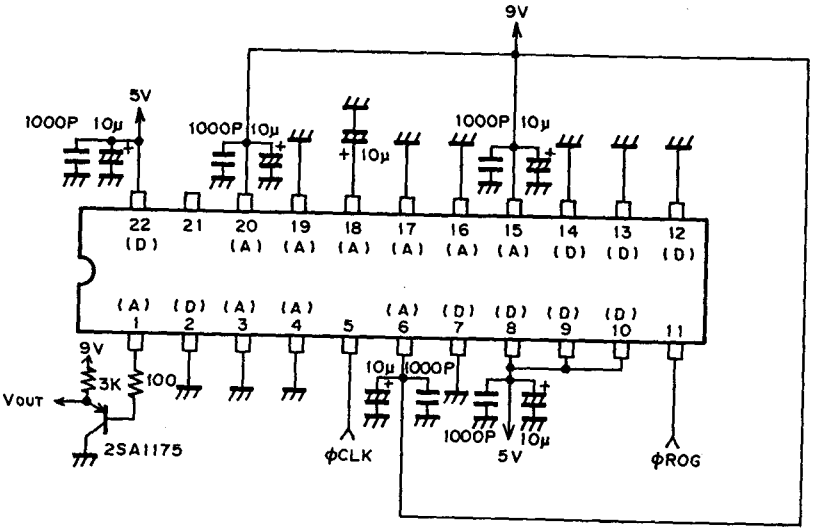


* When signal output without S/H

Clock Timing Diagram (For External RS mode)



Application Circuit



* Internal S/H is in use. Pin 4 must be connected to 5V DC power supply when S/H is not used.
* Internal RS mode is used. For the external RS mode, connect Pin 19 and Pin 4 to 5V DC power supply and input a proper clock pulse into Pin 10.
* When noise influence into output signal is large, connect pins indicated by (A) to the analog power supply and pins indicated by (D) to the digital power supply, and also use a decoupling capacitor of large capacitance.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Handling

1) Static charge prevention
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensor.
   e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Regulation for raising and lowering the power supply voltage.
When raising the supply voltage, first raise V_{DD1} (9V) and then V_{DD2} (5V). Similarly, lower V_{DD2} (5V) first and then V_{DD1} (9V).

3) Soldering
   a) Make sure the package temperature does not exceed 80 °C .
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an imaging device do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

4) Dust and dirt protection
   a) Operate in clean environments
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

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